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# Video Over IP with JPEG2000 Reference Design

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## Summary

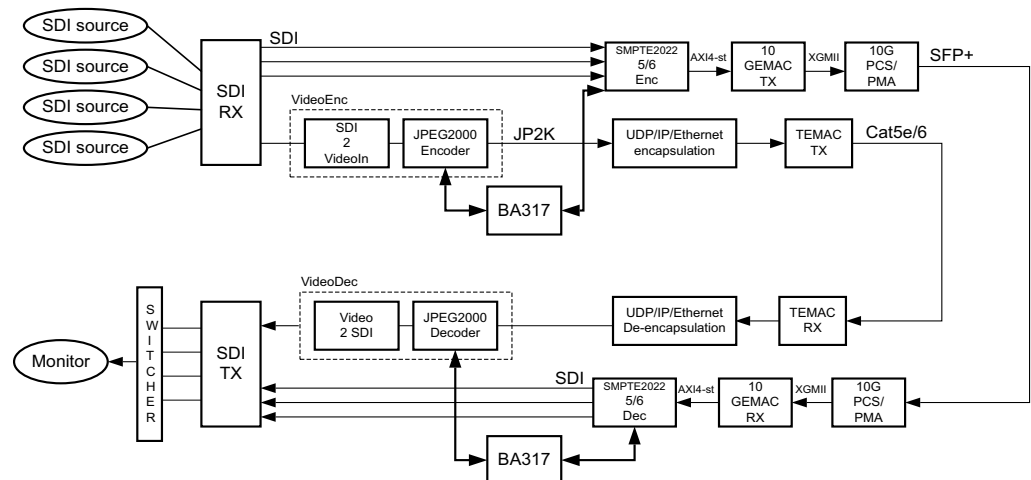
This application note describes the Video over IP reference design [Ref 9] that integrates the Xilinx Society of Motion Picture and Television Engineers (SMPTE) 2022-5/6 LogiCORE™ IP cores [Ref 1] and Barco-Silex JPEG2000 Encoder and Decoder IP Cores [Ref 6][Ref 7] IPs. The design is able to support up to four Standard Definition/High Definition-Serial Digital Interface (SD/HD-SDI) streams.

The entire reference design is composed of two platforms: the transmitter platform and the receiver platform. The transmitter platform design uses four LogiCORE IP triple-rate SDI cores [Ref 4] to receive the incoming SDI video streams. Three of the received SDI streams are multiplexed and encapsulated into fixed-sized datagrams by the SMPTE 2022-5/6 Video over IP transmitter core and sent out through the LogiCORE IP 10 Gb/s Ethernet MAC (10GEMAC) [Ref 5]. The 10 Gb/s link is supported by LogiCORE IP 10 Gb/s PCS/PMA using an SFP+ cable connected to the receiver end. The fourth SDI stream is compressed by the JPEG2000 encoder, encapsulated into fixed sized datagrams, and sent out through the LogiCORE IP Tri-Mode Ethernet MAC (TEMAC) to a standard Cat.5e cable.

On the receiver platform, the Ethernet datagrams of the uncompressed streams are collected at the 10GEMAC. The SMPTE 2022-5/6 Video over IP receiver core filters the datagrams, de-encapsulates and de-multiplexes them into individual streams, and outputs the SDI videos through the triple-rate SDI cores. The Ethernet datagrams of the compressed streams are collected at the Tri-Mode MAC, de-encapsulated and fed to the JPEG2000 decoder. Its output video is converted to SDI and sent to the triple-rate SDI cores. All the Ethernet datagrams are buffered in a DDR3 SDRAM for both the transmitter and receiver.

A MicroBlaze™ processor is included in the design to initialize the cores and read the status.

Figure 1 is a block diagram of the Video Over IP System; it provides a global view of the modules involved.



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Figure 1: Video Over IP System

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The reference design is targeted for the Kintex®-7 FPGA KC705 Evaluation Kit using the Kintex-7 FPGA XC7K325T-2FFG900C FPGA [Ref 2].

## Included Systems

The reference design is created and built using the ISE® Design Suite: System Edition, version 14.2. Part of the design is created using the Xilinx Platform Studio (XPS) tool. The design also includes software built using the Xilinx Software Development Kit (SDK). The software runs on the MicroBlaze processor subsystem and implements control and status functions.

## Introduction

The reference design implements two separate paths:

- Three SDI streams are handled by the SMPTE2022-5/6 and Ten Gigabit Ethernet MAC cores as described in the XAPP896 *SMPTE2022-5/6 High Bit Rate Media Transport Over IP Networks with Forward Error Correction on Kintex-7 FPGAs* application note [Ref 3], which should be consulted for the details on the uncompressed path. The present document only addresses the differences with that application note.
- The fourth SDI stream is routed to the compressed path where the reference design implements the JPEG2000 IPs as modules for broadcast applications that require bridging between broadcast connectivity standards SMPTE SD/HD/3G-SDI and 1GbE networks. The compressed data to be transported are mapped into media datagram payloads. Internet protocol (IP), user datagram protocol (UDP), and real-time transport protocol (RTP) provide standard headers in transporting the media over the IP network. To support the system functions correctly, the bandwidth available in the network always meets or exceeds the bandwidth required by the stream generated by the system. The overhead due to media datagram generation is approximately 4% due to Ethernet, IP, UDP and RTP headers.

The input and output of the complete compressed path are SDI video streams. The system contains two platforms; the encoder core resides in one platform while the decoder core resides in the other. A standard Cat.5e cable connects the two platforms simulating an IP network, as shown in Figure 2.

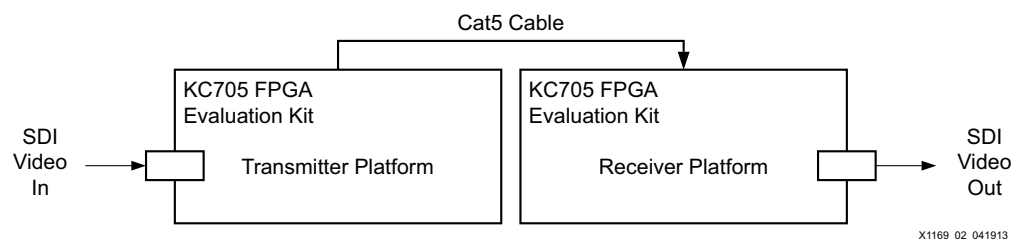


Figure 2: **Video Over IP Compressed Path (complete system)**

The triple-rate SDI core helps the system receive and transmit SDI streams while the Tri-Mode Ethernet MAC transfers the compressed video data in the Ethernet medium (see Figure 3 and Figure 4).

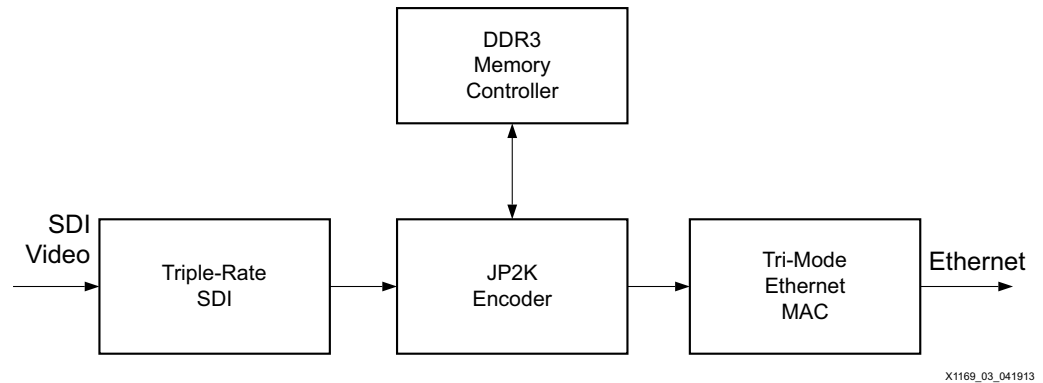


Figure 3: Video Over IP Compressed Path (Transmitter FPGA)

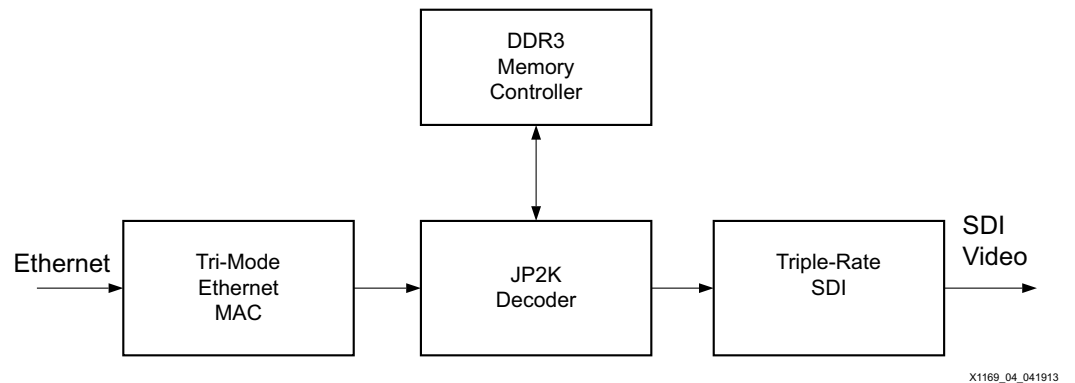
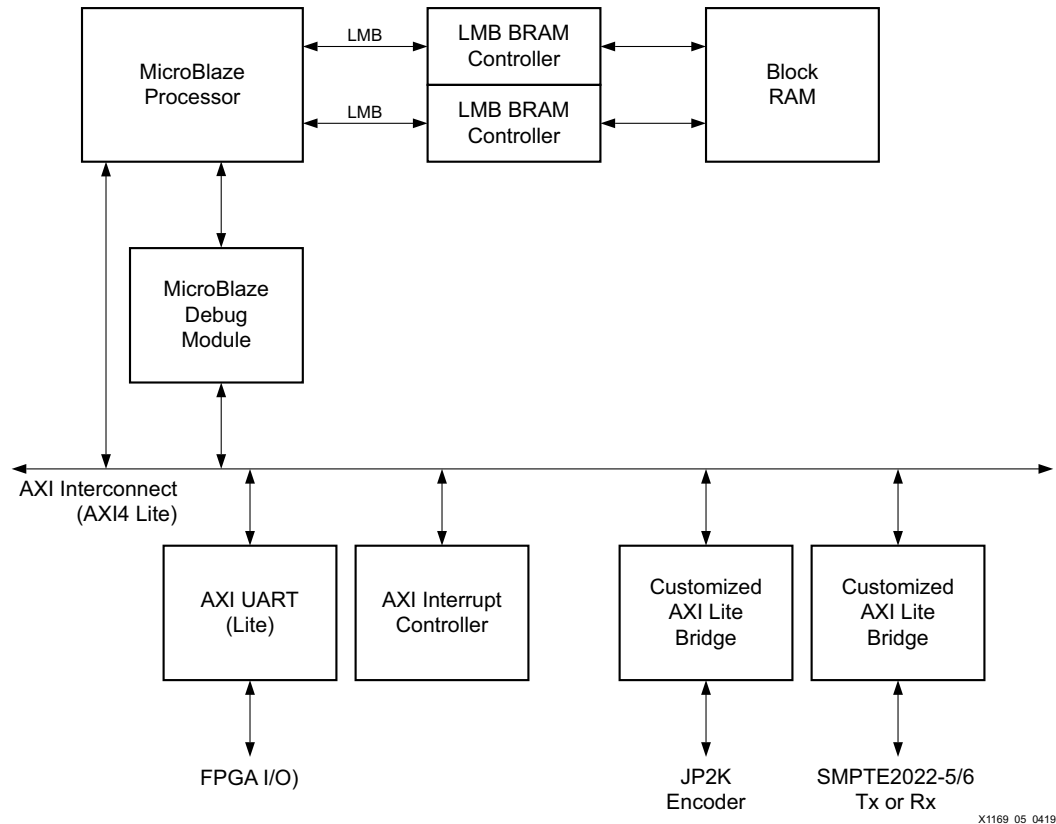


Figure 4: Video Over IP Compressed Path (Receiver FPGA)

## MicroBlaze

The MicroBlaze processor subsystem presented in XAPP896 [Ref 3] has been simplified and adapted. The AXI Memory Interface Generator (MIG) that was instantiated in the subsystem is replaced by the Barco-Silex DDR3 Memory Controller (outside the MicroBlaze processor subsystem), which supports AXI ports (for the SMPTE2022-5/6 cores) and non-AXI ports (for the JPEG2000 cores). The clock generator and processor system reset block have been removed and replaced by dedicated circuitry outside the MicroBlaze processor subsystem. A second AXI4-Lite bridge has been added in the transmitter to configure the JPEG2000 encoder. Figure 5 shows a block diagram of the modified MicroBlaze processor subsystem.



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Figure 5: Microblaze Processor Subsystem Built Using XPS

Table 1 shows the adapted address map of the MicroBlaze processor subsystem.

Table 1: MicroBlaze Processor Subsystem Address Map

Peripheral	Instance	Base Address	High Address
lmb_bram_if_cntlr	microblaze_0_i_bram_ctrl	0x00000000	0x0001FFFF
lmb_bram_if_cntlr	microblaze_0_d_bram_ctrl	0x00000000	0x0001FFFF
Mdm	debug_module_0	0x7E200000	0x7E20FFFF
axi_v6_ddrx	axi_v6_ddrx_0	0xE0000000	0xFFFFFFFF
axi_uartlite	RS232_Uart_1	0x40600000	0x4060FFFF
axilite_bridge	axilite_bridge_0	0x70E00000	0x70e0FFFF
axilite_bridge	axilite_bridge_1	0x79400000	0x7940FFFF

## Hardware Requirements

The hardware requirements for the reference design are:

- Two Kintex-7 KC705 FPGA evaluation kits
- Two Inrevium SDI FPGA Mezzanine Cards (FMC) (TB-FMCH-3GSDI2A)
- Cat.5e cable
- SFP+ cable

## Reference Design Specifics

The reference design includes the following cores:

- AXI Interconnect
- MicroBlaze Processor
- MicroBlaze Debug Module
- Local Memory Bus (LMB)
- LMB Block RAM Controller
- Block RAM
- AXI External Master Connector
- AXI UART (lite)
- Customized AXI4-Lite Bridge (pcore)
- Barco-Silex DDR3 Memory Controller (BA317)
- SMPTE2022-5/6 transmitter and receiver
- Barco-Silex JPEG2000 encoder (BA110) and decoder (BA109)
- Triple-Rate SDI
- 10-Gigabit Ethernet MAC
- Tri-Mode Ethernet MAC

## Hardware System Specifics

This section describes the high-level features of the reference design, including how the main IP blocks are configured. The 10-Gigabit Ethernet MAC, AXI Interconnect (AXI4-Lite) and Software Applications sections found in the XAPP896 [\[Ref 3\]](#) are also valid for the current design and should be referred to for more details.

### SMPTE 2022-5/6 Video Over IP Transmitter and Receiver

The information from the SMPTE2022-5/6 Video over IP Core product page [\[Ref 1\]](#) is valid except the BNC mapping for the uncompressed channels.

*Table 2: BNC Connector Mapping*

Channel	BNC Connector
1	RX2/TX2
2	RX3/TX3
3	RX4/TX4

## Triple-Rate SDI

The Triple-Rate SDI core provides transmitter and receiver interfaces for the SD-SDI and HD-SDI standards. The core is connected to the Kintex-7 FPGA GTX transceiver for serialization and deserialization of the SDI stream. The Triple-Rate SDI receiver uses a 148.5 MHz GTX transceiver reference clock frequency to receive its supported SDI bit rates. The receiver automatically determines the incoming SDI bit rate and configures itself and the GTX transceiver appropriately for that SDI mode. The Triple-Rate SDI transmitter requires two different GTX transceiver reference clock frequencies to support all SDI bit rates. The transmitter in turn controls the GTX transceiver transmitter through the DRP port to configure the GTX transceiver transmitter appropriately for each SDI mode. See the *SMPTE SDI Product Guide v2.0* for more information [\[Ref 4\]](#).

In the reference design, only a 148.5 MHz reference clock is provided, and the 59.94 MHz, 29.97 MHz, and 23.98 MHz bit rates cannot be generated. These are replaced with 60 MHz, 30 MHz, and 25 MHz respectively.

## BA317 DDR3 Memory Controller

The memory controller [\[Ref 8\]](#) has AXI ports for the SMPTE2022-5/6 cores (256-bits wide interface running at 200 MHz) and user ports for the JPEG2000 cores (32, 64 or 128 bits wide running at different frequencies).

## JPEG2000 Encoder

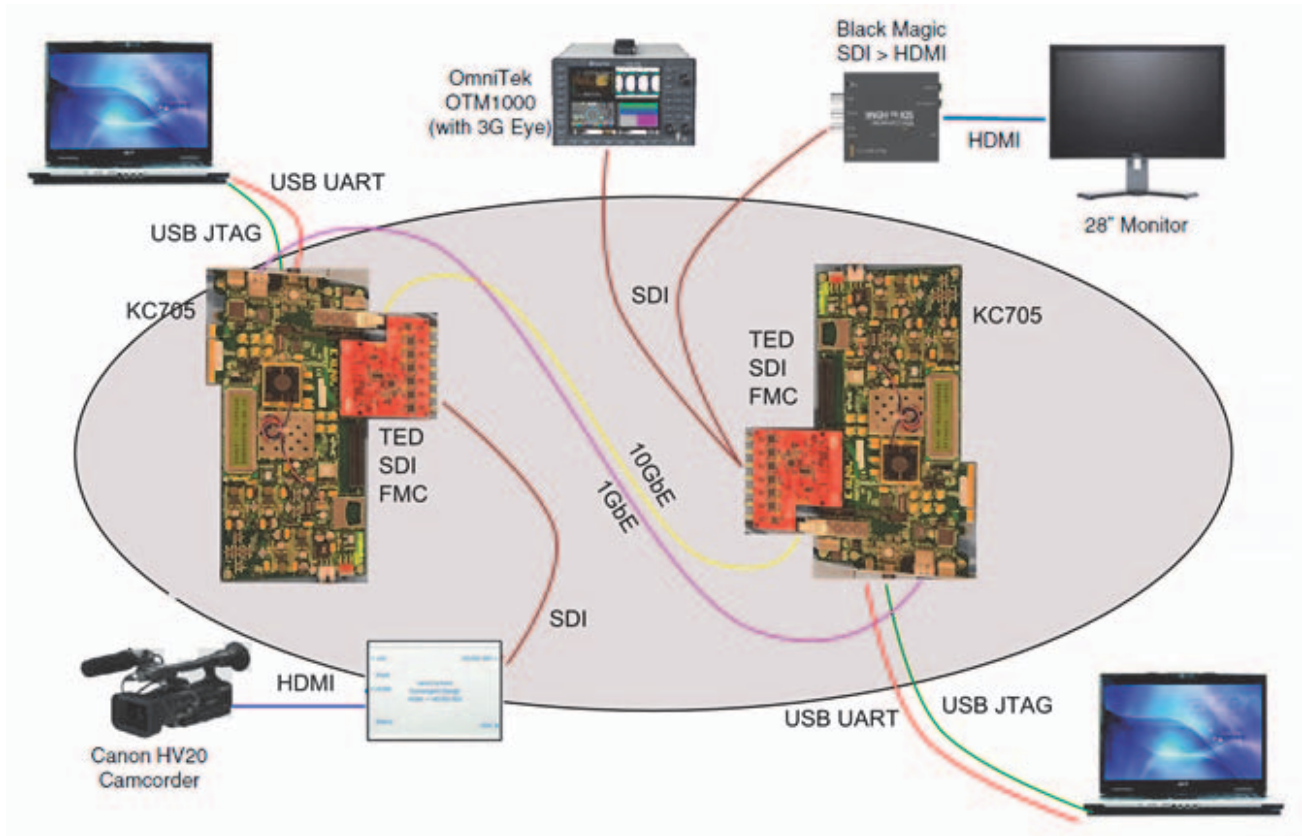
The JPEG2000 Encoder core [\[Ref 6\]](#) compresses a video stream (from the BNC connector TX1) to the JPEG2000 format to be transferred to the 1Gb Ethernet cable. Its input must be a video stream, so the SDI stream coming out of the Triple-Rate SDI core must be converted. Its parameters have been fixed in the VideoEnc netlist, except the bit rate that can be changed dynamically through the software. It has 15 user ports to the Memory controller and uses the fourth quarter of the memory (upper addresses).

## JPEG2000 Decoder

The JPEG2000 Decoder core [\[Ref 7\]](#) decompresses a JPEG2000 stream received from the 1Gb Ethernet cable. Its video output must be converted to SDI and sent to the Triple-Rate SDI core. It has eight ports to the Memory controller and uses the fourth quarter of the memory (upper addresses). The frames coming out of the decoder are stored in DDR and read as required by the SDI bit rate constraints. Some might be dropped and some repeated if necessary. The decoder and video conversion logic are provided as a single netlist (VideoDec).

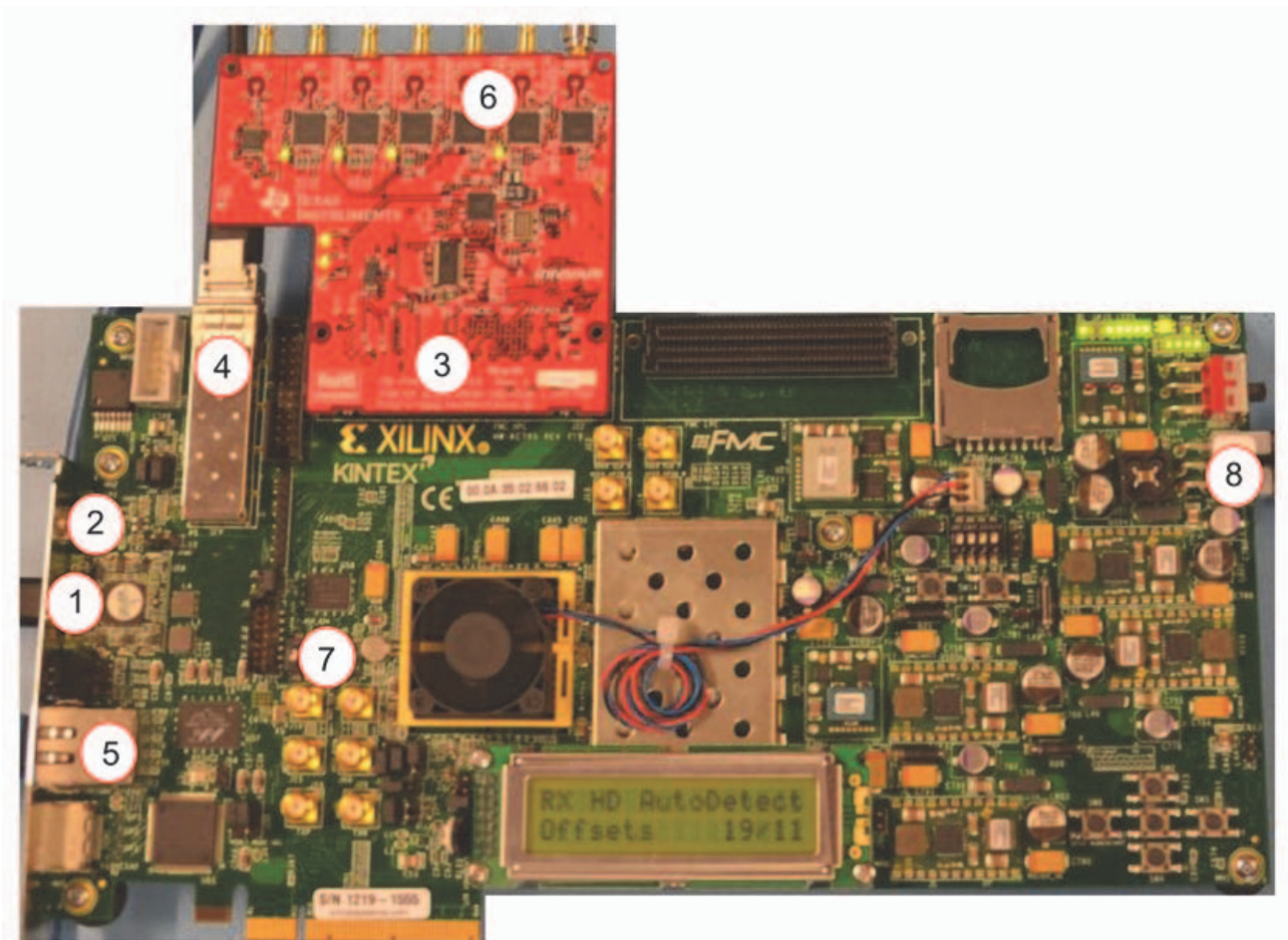
# Executing the Reference Design In Hardware

This section provides instructions to execute the reference design in hardware. This reference design runs on the KC705 and TED SDI FMC boards shown in [Figure 6](#) and [Figure 7](#).



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Figure 6: Video Over IP System Setup



X1169\_07\_041913

**Figure 7: KC705 and TB-FMCH-3GSDI2 Boards**

In these instructions, numbers in parentheses correspond to callout numbers in [Figure 7](#).

1. Connect a USB cable from the host PC to the USB JTAG port (1). Ensure that the appropriate device drivers are installed.
2. Connect a second USB cable from the host PC to the USB UART port (2). Ensure that the USB UART drivers have been installed.
3. Connect the TB-FMCH-3GSDI2 board to the FMC HPC connector of the KC705 board (3).
4. Connect one end of the SFP+ cable (4) to the Video over IP transmitter board, and the other end to the Video over IP receiver board.
5. Connect one end of the Cat.5e cable (5) to the RJ45 connector of the Video over IP transmitter board, and the other end to the RJ45 connector of the Video over IP receiver board.
6. If the KC705 board is the Video over IP receiver, connect the SDI TX ports 1 to 4 (6) to the SDI video monitor; otherwise leave them unconnected.
7. If the KC705 board is the Video over IP transmitter, connect the SDI RX ports 1 to 4 (6) to the SDI video generator; otherwise leave them unconnected.
8. Configure the J17 switch to JTAG mode ("00101") (7).
9. Connect the power supply to the KC705 (8).



10. Switch on the KC705 board.
  11. Start a terminal program (for example, HyperTerminal) on the host PC with these settings:
    - Baud Rate: 115200
    - Data Bits: 8
    - Parity: None
    - Stop Bits: 1
    - Flow Control: None
  12. Program both FPGAs with the bit files, through Impact or the ChipScope™ analyzer for example.
  13. The GPIO LEDs are:
    - led(0) on both boards: DDRInitDone. If lit, it indicates that the DDR controller has calibrated and is operational.
    - led (3-1) on the TX board only: JPEG2000 compression rate. At startup it is "011" as the default rate value (100kB) is the third in the compression rate menu, as shown in [Figure 9](#).
- 

## Results from Running Hardware and Software

The software interface is identical to that presented in XAPP896 [\[Ref 3\]](#), with one additional option to configure the JPEG2000 encoder rate interactively. The software for the receiver board has not been modified. [Figure 8](#) presents HyperTerminal screens of the Video over IP TX output display.

```

Xilinx Inc.
V_SMPTE2022_56_TX Reference Design
Created: April 11, 2012
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VoIP TX Reset
VoIP TX Initializing...
IP Address: 192.168.0.100
MAC Address: 0-0-0-0-0-AA
All VoIP TX channels enabled
VoIP TX Initialization done

Enabling Channel 1
Initializing Channel 1
Dest IP Addr: 192.168.0.50
Source Port: 16
Dest Port: 16
SSRC: 0x12345600
FEC Size: 77x77
FEC: Off
Channel 1 Initialization Done

Enabling Channel 2
Initializing Channel 2
Dest IP Addr: 192.168.0.50
Source Port: 32
Dest Port: 32
SSRC: 0x12345610
FEC Size: 77x77
FEC: Off
Channel 2 Initialization Done

Enabling Channel 3
Initializing Channel 3
Dest IP Addr: 192.168.0.50
Source Port: 48
Dest Port: 48
SSRC: 0x12345620
FEC Size: 77x77
FEC: Off
Channel 3 Initialization Done

-----
-- VoIP TX Main Menu --
-----

Select option
1 = Reset SMPTE Core
2 = Initialize SMPTE Core
3 = Configure SMPTE Channel
4 = Change JPEG2000 rate
q = exit
? = help
-----
```

Figure 8: VoIP\_TX HyperTerminal Output

You can choose one of the five options displayed on the HyperTerminal screen (Figure 8):

1. Reset SMPTE Core
2. Initialize SMPTE Core general space registers
3. Configure SMPTE Channel
4. Change JPEG2000 rate
- q. Exit software application
- ?. Display current menu

The fourth option changes the size of the JP2K compressed stream (in number of bytes per picture), which has a direct influence on the quality of the displayed image at the SDI output of the Receiver — the lowest the compressed size, the lowest the quality of the output.

```
>4
Select rate (bytes per compressed file)
0 = 5 kB
1 = 20 kB
2 = 50 kB
3 = 100 kB
4 = 200 kB
5 = 400 kB
m = Main Menu
-----
>
```

Figure 9: VoIP\_TX Change JPEG2000 rate HyperTerminal Output

You can choose one of the six compressed sizes or go back to the main menu. The third value (101042 bytes per compressed file) is the default one.

## Building Hardware

Before rebuilding the project, ensure that the licenses for the SMPTE 2022-5/6 video over IP transmitter and receiver cores, 10-Gigabit Ethernet PCS/PMA, 10-Gigabit Ethernet MAC and Tri-Mode Ethernet MAC are installed. Run the `buildfpga.sh` shell script (found under `implementation/`) to generate the programming files. The script must be run from that directory.

## Reference Design

Table 3 shows the reference design checklist.

Table 3: Reference Design Checklist

Parameter	Description
<b>General</b>	
Developer names	Jean-François Marbehant and Virginie Brodeoux
Target devices (stepping level, ES, production, speed grades)	Kintex-7 FPGAs
Source code available	Netlists are provided for the BA317 memory controller, the JPEG2000 encoder and decoder and Xilinx LogiCORE IP cores. The rest is provided as source code.
Source code format	VHDL and Verilog
Design uses code/IP from existing Xilinx application note/reference designs, CORE Generator™ tool, or third party	Cores generated from EDK and from CORE Generator system
CORE Generator system	CORE Generator system
<b>Simulation</b>	
Functional simulation performed	N/A
Timing simulation performed	N/A
Test bench used for functional and timing simulations	N/A
Test bench format	N/A
Simulator software/version used	N/A
SPICE/IBIS simulations	N/A
<b>Implementation</b>	
Synthesis software tools/version used	XST 14.2
Implementation software tools/versions used	ISE Design Suite: System Edition 14.2
Static timing analysis performed	Yes
<b>Hardware Verification</b>	
Hardware verified	Yes
Hardware platform used for verification	Kintex-7 FPGA Evaluation Kit

## Design Characteristics

The reference design is implemented in a Kintex-7 FPGA (XC7K325T-2FFG900CFPGA) using the ISE Design Suite: System Edition 14.2. The resources used for the Video over IP TX and RX platforms per the summary report are summarized in [Table 4](#).

*Table 4: Resource Utilization*

Platform	LUTs	I/Os	RAMB36E1s	RAMB18E1s
TX	96,752 out of 203,800 (47%)	184 out of 500 (36%)	285 out of 445 (64%)	149 out of 890 (16%)
RX	75,315 out of 203,800 (36%)	181 out of 500 (36%)	230 out of 445 (51%)	184 out of 890 (20%)

## Conclusion

This application note describes a video over IP network system using various Xilinx IP cores and JPEG2000 cores.

It demonstrates the ability of the SMPTE 2022-5/6 video over IP cores to encapsulate and de-encapsulate multiple SDI streams and transport these streams through a 10 Gb/s Ethernet pipe. The utilization of the Ethernet bandwidth is over 90% with three 3G-SDI videos. The design can perform recovery of a limited number of Ethernet packets when impairment is introduced into the network with the FEC engine turned on. It also demonstrates the possibility to compress those same streams using JPEG2000 and transport them over 1 Gb/s Ethernet cable.

## Reference

This application note uses the following references:

1. [SMPTE2022-5/6 Video Over LogiCORE IP Core product page](#)
2. [Kintex-7 FPGA KC705 Evaluation Kit product page](#)
3. *SMPTE2022-5/6 High Bit Rate Media Transport Over IP Networks with Forward Error Correction on Kintex-7 FPGAs* ([XAPP896, v1.0](#))
4. *SMPTE SDI Product Guide v2.0* ([PG071](#))
5. [10 Gigabit Ethernet Media Access Controller \(10GEMAC\) product page](#)
6. [Barco Silex BA110 JPEG 2000 multichannel HD/DCI encoder product page](#)
7. [Barco Silex BA109 JPEG 2000 multichannel HD/DCI decoder product page](#)
8. [Barco Silex BA317 Multi-port external memory controller product page](#)
9. Link to design files ([zip file](#))

## Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
04/30/2013	1.0	Initial Xilinx release
07/08/2013	1.1	<ul style="list-style-type: none"> <li>Removed and updated some references.</li> <li>Updated Figures 8 and 9.</li> <li>Added link to lounge and design file.</li> <li>Added Step 13 to Executing the Reference Design in Hardware section.</li> </ul>
07/10/2013	1.2	<ul style="list-style-type: none"> <li>Enlarged Figure 9.</li> <li>Replaced text in Building Hardware section with new text.</li> </ul>

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