XAPP1199 (v1.2) September 30, 2015

SMPTE 2022-5/6 High Bit Rate Media Transport Over IP Networks with Forward Error Correction and Seamless Protection Switching on Kintex-7 FPGAs in Vivado Design Suite

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Summary

This application note covers the design considerations of a Video Over IP networks system using the performance features of the LogiCORE™ IP SMPTE 2022-5/6 Video Over IP transmitter and receiver cores. The design focuses on high bit rate, native media transport over 10 Gb/s Ethernet with a built-in forward error correction (FEC) engine and seamless protection switching. The design is able to support up to three SD/HD/3G-SDI streams.

The reference design has two platforms: the transmitter platform and the receiver platform. The transmitter platform design uses three SMPTE SDI cores to receive the incoming SDI video streams. The received SDI streams are multiplexed and encapsulated into fixed-size datagrams by the SMPTE 2022-5/6 Video Over IP transmitter core and sent out through two 10-Gigabit Ethernet MAC cores. The 10 gigabit link is supported by two 10-Gigabit Ethernet PCS/PMA cores using an optical cable connected to the receiver end. On the receiver platform, the Ethernet datagrams are collected at the 10-Gigabit Ethernet MAC. The SMPTE 2022-5/6 Video Over IP receiver core filters the datagrams, de-encapsulates and de-multiplexes the datagrams into individual streams which are output through the SMPTE SDI cores. The Ethernet datagrams are buffered in DDR3 SDRAM for both the transmitter and receiver. The DDR traffic passes through the AXI4 interconnect to the 7 series AXI memory controller. A MicroBlaze™ processor is included in the design to initialize the cores and read the status.

The reference design targets the Xilinx® Kintex®-7 FPGA KC705 evaluation kit, which uses the Kintex-7 XC7K325T-2FFG900 FPGA, Inrevium TB-FMCH-3GSDI2A and Faster Technology FM-S14 Quad SFP/SFP+ transceiver FMC boards. See the Kintex-7 FPGA KC705 Evaluation Kit [Ref 1], Inrevium TB-FMCH-3GSDI2A board [Ref 2] and Faster Technology FM-S14 Quad SFP/SFP+ transceiver FMC [Ref 11] for details.

Included Systems

The reference design was created and built using the Vivado® Design Suite, System Edition 2015.2. The design also includes software built using the Xilinx Software Development Kit (SDK) 2015.2. The software runs on the MicroBlaze processor subsystem and implements control and status functions. Complete project files for Vivado Design Suite and the SDK are provided with this application note to allow examination and rebuilding of the design or to use it as a template for starting a new design.

Introduction

The reference design is built around the SMPTE 2022-5/6 Video Over IP transmitter and receiver cores and leverages additional Xilinx IP cores to form the complete system. The input and output of the system are SDI video streams. The system consists of two platforms. The transmitter and receiver cores each reside in separate platforms. An optical cable connects the two platforms simulating an IP network. See Figure 1.

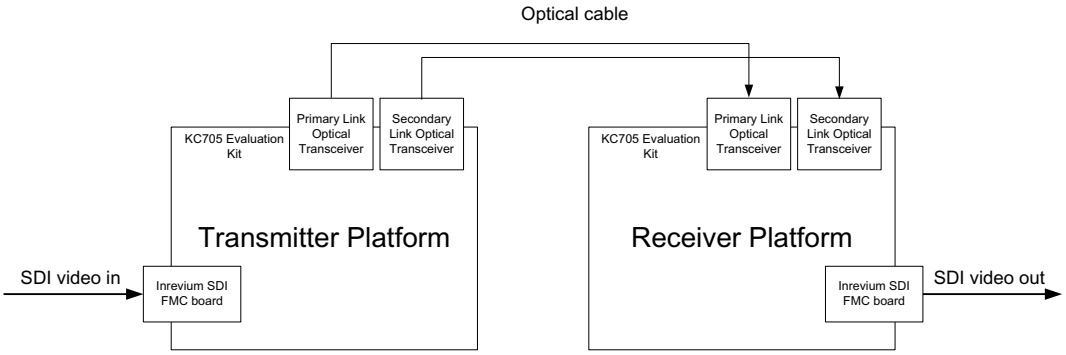

Figure 1: **Top Level Diagram of the Video over IP**

The SMPTE SDI core allows the video over IP cores to receive and transmit SDI streams while the 10-Gigabit Ethernet MAC and 10-Gigabit Ethernet PCS/PMA enable the video over IP cores to transfer SDI data in the Ethernet medium. See Figure 2 and Figure 3.

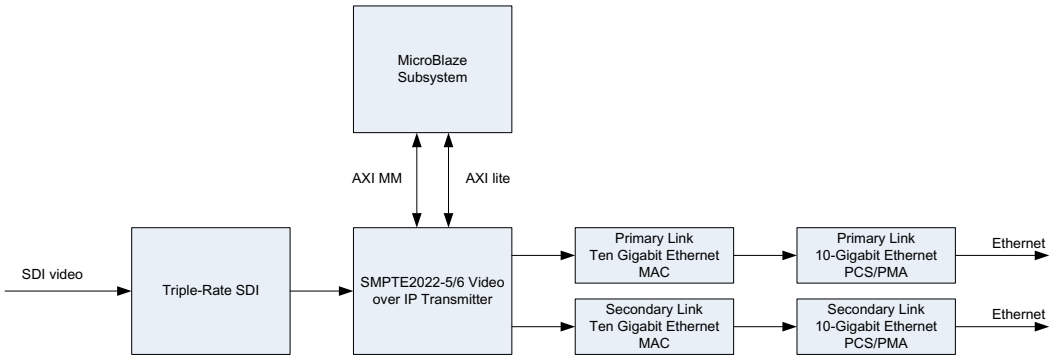

Figure 2: **Block Diagram of the Video over IP Transmitter FPGA**

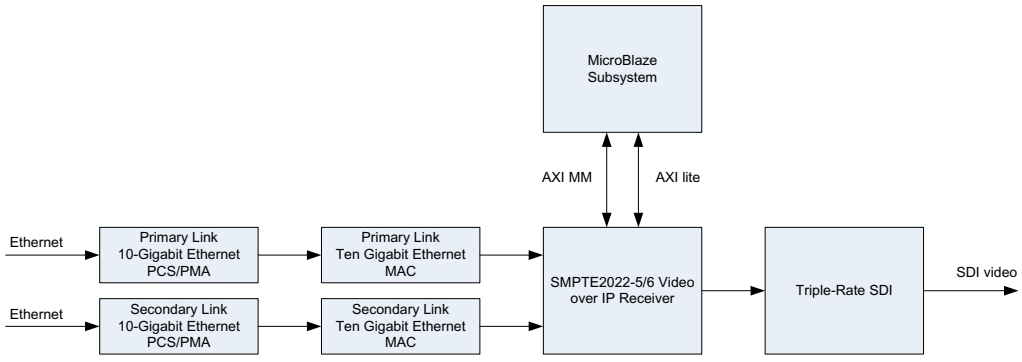

Figure 3: **Block Diagram of the Video over IP Receiver FPGA**

Other than managing the SDI streams, encapsulation and de-encapsulation, the transmitter and receiver cores include forward error correction (FEC) and seamless protection switching features. FEC protects the video stream during the transport of high-quality video over IP networks. With FEC, the transmitter adds systematically generated redundant data to its video. This redundancy allows the receiver to detect and correct a limited number of packet errors occurring anywhere in the video without the need to query the transmitter for additional video data. These errors, in the form of lost video packets, result from several causes ranging from thermal noise to storage system defects and transmission noise introduced by the environment. FEC gives the receiver the ability to correct these errors without needing a reverse channel to request retransmission of data. Seamless protection switching allows transmission and reception of two identical streams over potentially diverse path to add more reliability to the system. The receiver handles the seamless switching datagram by datagram

without impacting the content or the stream. This feature can be enabled using the core registers.

High-level control of the system is provided by a simplified MicroBlaze embedded processor subsystem containing I/O peripherals and processor support IP cores. A clock generator block and a processor system reset block supply clock and reset signals for the system, respectively. An AXI4 interconnect and an AXI4 memory interface generator (MIG) are instantiated in the subsystem allowing the video over IP cores access to the DDR3 SDRAM. See Figure 4 and Table 1 for a block diagram of the MicroBlaze processor subsystem and its address map.

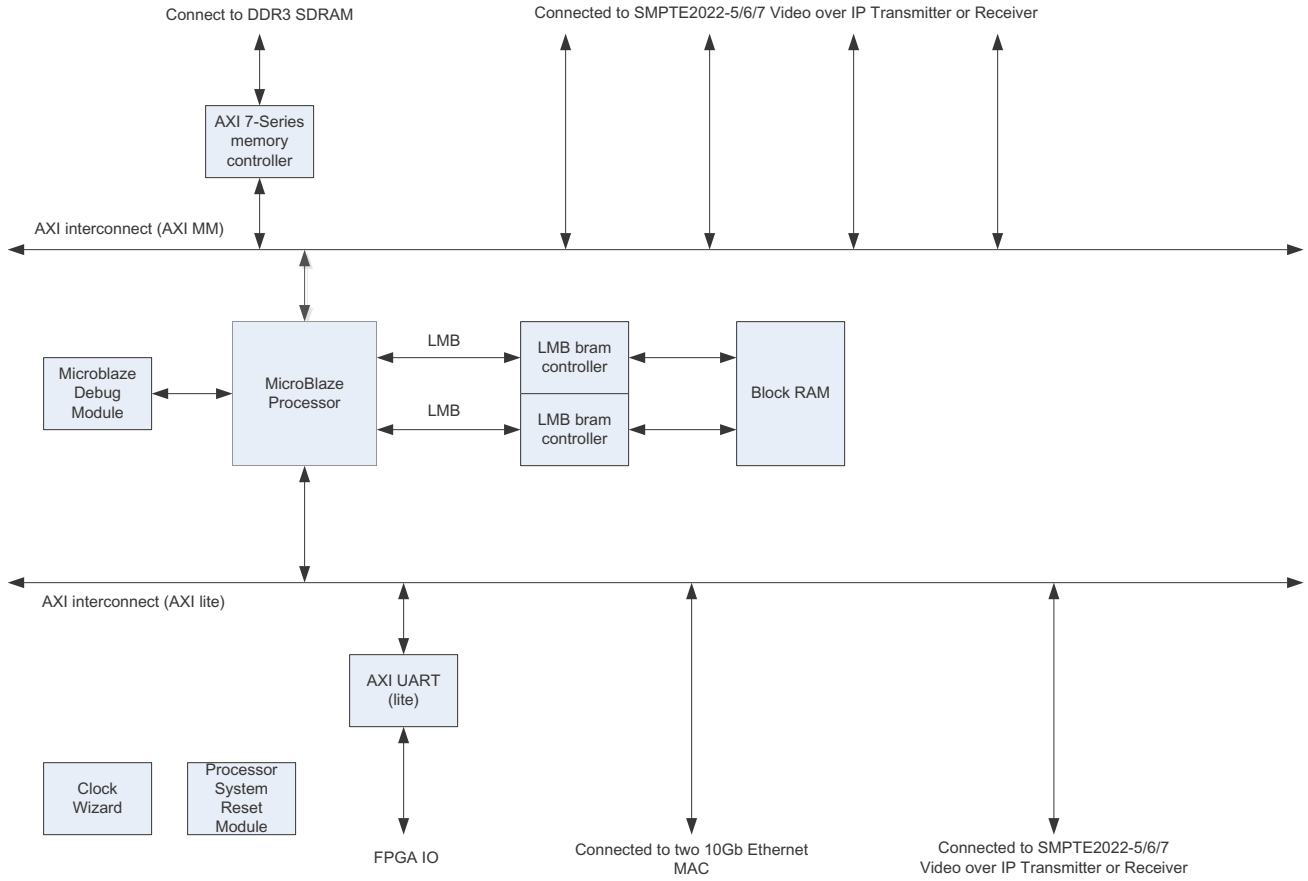

Figure 4: **MicroBlaze Processor System Block Diagram**

Table 1: **MicroBlaze Processor Subsystem Address Map**

Peripheral	Instance	Base Address	High Address
lmb_bram_if_cntlr	ilmb_bram_if_cntlr	0X00000000	0X0001FFFF
lmb_bram_if_cntlr	dlmb_bram_if_cntlr	0X00000000	0X0001FFFF
mig_7series	mig_1	0XC0000000	0XFFFFFFFF
axi_uartlite	axi_uartlite_1	0X40600000	0X4060FFFF
axilite_bridge	smpte2022_axilite	0X70E00000	0X70E0FFFF
axilite_bridge	ten_gig_eth_mac1_axilite	0X7C400000	0X7C400FFF
axilite_bridge	ten_gig_eth_mac2_axilite	0X7C500000	0X7C400FFF

Hardware Requirements

The hardware requirements for the reference design are:

- Two Xilinx Kintex-7 FPGA KC705 Evaluation Kits
- Two Inrevium 3G-SDI Boards (TB-FMCH-3GSDI2A)
- Two Faster Technology Quad SFP/SFP+ transceiver FMC (FM-S14)
- Two SFP+ Optical Transceiver modules
- Optical Cable
- Vivado Design Suite 2015.2
- SDK 2015.2

Reference Design Specifics

In addition to the SMPTE 2022-5/6 Video Over IP transmitter and receiver cores, the reference design includes the following cores:

- AXI Interconnect
- MicroBlaze Processor
- MicroBlaze Processor Debug Module
- Local Memory Bus
- LMB Block RAM Interface Controller
- Block Memory Generator
- Clocking Wizard
- Processor System Reset Module
- AXI UART Lite
- MIG 7 Series
- SMPTE SD/HD/3G-SDI
- 10-Gigabit Ethernet MAC
- 10-Gigabit Ethernet PCS/PMA

Hardware System Specifics

This section describes the high-level features of the reference design, including how the main IP blocks are configured.

Video Over IP System

The reference design implements the SMPTE 2022-5/6 Video Over IP cores as modules for broadcast applications that require bridging between broadcast connectivity standards (SD/HD/3G-SDI) and a 10 Gb/s Ethernet network. The cores are intended for developing Internet protocol-based systems to reduce the overall cost in broadcast facilities for distribution and routing of audio and video data. The SDI data to be transported are mapped into media datagram payloads as per SMPTE 2022-6. The systematically-generated redundant forward error correction datagram packets are formatted according to SMPTE 2022-5. IP/UDP/RTP protocols provide standard headers when transporting the media and FEC datagram packets over the IP network. The SMPTE 2022-5/6 datagrams are transmitted twice through two 10-Gigabit Ethernet MACs for seamless protection switch according SMPTE 2022-7.

To support the system functions correctly, the bandwidth available in the network must meet or exceed what is required to support the stream generated by the system. The overhead required for media datagram generation is approximately 5% due to the IP/UDP/RTP and SMPTE 2022-6 headers.

SMPTE 2022-5/6 Video Over IP Transmitter

The SMPTE 2022-5/6 Video Over IP transmitter in the reference design is configured to accept three channels of SDI input from the SMPTE SDI receiver. The transmitter connects to the 10-Gigabit Ethernet MAC through an AXI4-Stream data interface. The transmitter also connects to the MicroBlaze processor subsystem through an AXI4-Lite control interface. The transmitter core uses two AXI4 external master connectors to access the DDR3 SDRAM through the AXI4 interconnect. The memory map address range is fixed at `0xC0000000` — `0xFFFFFFFF`.

The transmitter source MAC address is set to `0x000000000000AA` and `0x000000000000CC` respectively. The transmitter source IP address for primary and secondary links are set to 192.168.0.50 and 192.168.1.50 respectively and the destination IP address for primary and secondary links are set to 192.168.1.100 and 192.168.1.100 respectively. The UDP ports are configured as shown in Table 2. The FEC matrix sizes set for the channels are shown in Table 3. These parameters are configurable through the registers.

Table 2: **UDP Port Values for SDI Channels**

BNC Connector	Channel	Source UDP Port	Destination UDP Port
RX1	0	0x10	0x10
RX2	1	0x20	0x20
RX3	2	0x30	0x30

Table 3: **FEC Matrix Size Values for SDI Channels**

BNC connector	Channel	L	D
RX1	0	77	77
RX2	1	77	77
RX3	2	77	77

The SMPTE 2022-5/6 Video Over IP transmitter contains an AXI4-Lite interface which allows dynamic control of the parameters within the core from a processor. For more information about the registers, see the *LogiCORE IP SMPTE 2022-5/6 Video over IP Transmitter Product Guide* (PG032) [Ref 4].

The registers are divided into two categories: general space registers and channel space registers. The channel space register is divided into two sections where the parameters are set based on either the respective links and channel or the respective channel only. In this reference design, three channels are supported and all of the parameters are differentiated by the UDP destination port and the primary and secondary links are differentiated by the IP Address. See Software Applications, page 8 for details.

For the general space registers, normal address read and write access is applied. For the Channel space registers, follow these steps to update the registers:

1. Set the channel to configure at register address `base_addr+0x00C`.
2. Configure the channel-specific register.
3. Pulse the `reg_update` bit of the Control register to commit the change to the channel register.
4. Repeat step 1 through step 3 for each additional channel or register. See Figure 5.

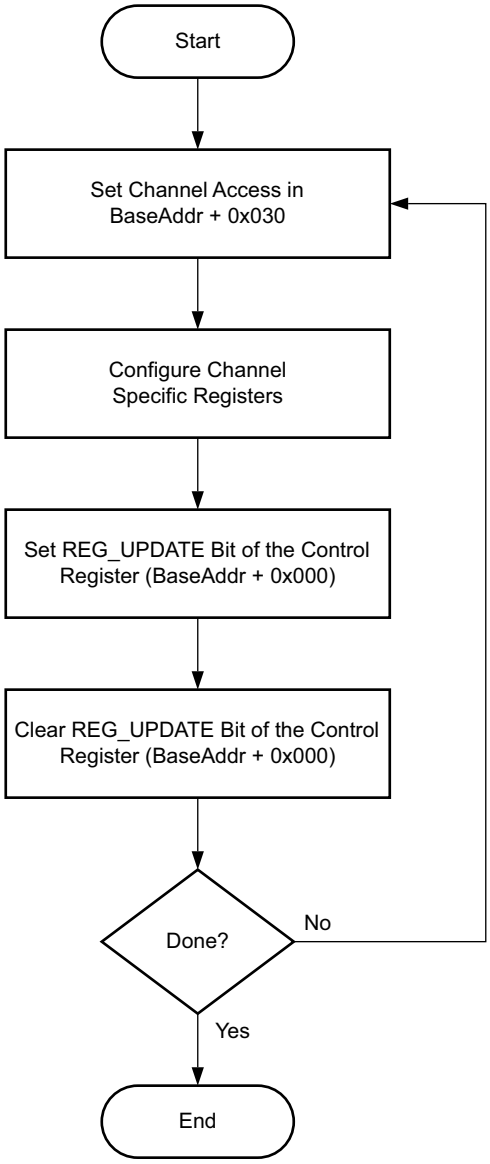

Figure 5: **Channel Register Configuration Flow Chart**

SMPTE 2022-5/6 Video Over IP Receiver

The SMPTE 2022-5/6 Video Over IP receiver in the reference design is configured to stream three channels of SDI output to the SMPTE SDI transmitters. The receiver connects to the 10-Gigabit Ethernet MAC through two AXI4-Stream data interfaces. The receiver also connects to the MicroBlaze processor subsystem through an AXI4-Lite control interface. The receiver core uses two AXI4 external master connectors to access the DDR3 SDRAM using an AXI4 interconnect. The memory map address range is fixed at `0xC0000000` — `0xFFFFFFFF`.

The incoming media packets are filtered based on UDP destination ports shown in Table 4.

Table 4: **UDP Port Values for SDI Channels**

BNC connector	Channel	Destination UDP port
TX1	0	`0x10`
TX2	1	`0x20`
TX3	2	`0x30`

The SMPTE 2022-5/6 Video Over IP receiver contains an AXI4-Lite interface which allows dynamic control of the parameters within the core from a processor. For more information about the registers, see the *LogiCORE IP SMPTE 2022-5/6 Video over IP Receiver Product Guide* (PG033) [Ref 5].

The registers are divided into two categories: general space registers and channel space registers.The parameters in the channel space apply to an individual channel.

For the general space registers, normal address read and write access is applied. For the Channel space registers, follow these steps to update the registers:

1. Set the channel to configure at register address `base_addr+0x00C`.
2. Configure all channel registers of interest for the particular channel.
3. Pulse bit 1 of register address, `base_addr+0x000`, to commit the channel registers change.
4. Repeat step 1 through step 3 for each additional channel. See Figure 5, page 6.

SMPTE SD/HD/3G-SDI

The SMPTE SDI core provides transmitter and receiver interfaces for SMPTE SD-SDI, HD-SDI and 3G-SDI standards. The core is connected to 7 series FPGA GTX transceivers to serialize and deserialize the SDI video streams. The SMPTE SDI receiver uses a 148.5 MHz GTX transceiver reference clock frequency to receive its supported SDI bit rates. The receiver automatically determines the incoming SDI bit rate and configures itself and the GTX transceiver appropriately for that SDI mode. The SMPTE SDI transmitter requires two different GTX transceiver reference clock frequencies to supply the supported SDI bit rates of 148.5 MHz and 148.35 MHz specified in the design. The clock multiplexer built into the GTX transceiver switches between these two reference clocks. A port dynamically determines the operating SDI mode for the transmitter. The transmitter, in turn, controls the GTX transmitter through the dynamic reconfiguration port (DRP) to provide the appropriate configuration for each SDI mode. See the *SMPTE SD/HD/3G-SDI Product Guide* (PG071) [Ref 6] for more information.

10-Gigabit Ethernet MAC

The 10-Gigabit Ethernet MAC instances on the transmitter side has the AXI4-Stream transmit interfaces connected to the output of the SMPTE 2022-5/6 /7video over IP transmitter. The 10-Gigabit Ethernet MAC instances on the receiver side has the AXI4-Stream receive interfaces connected to the input of the SMPTE 2022-5/6 video over IP receiver. A 64-bit SDR PHY port is configured in the 10-Gigabit Ethernet MAC to interface to the 10-Gigabit Ethernet PCS/PMA cores. No flow control is used. See the *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072) [Ref 7] for more information.

10-Gigabit Ethernet PCS/PMA

The 10-Gigabit Ethernet PCS/PMA core creates a 10GBASE-R optical link between the video over IP transmitter and receiver platforms. The PCS/PMA uses ones transceiver to achieve a 10 Gb/s data rate. An optical cable is connected between the SFP+ optical transceivers on both platforms. The PCS/PMA 10GBASE-R/KR standard is fully specified in clauses 45, 49, 72, 73, and 74 of the 10-Gigabit Ethernet IEEE 802.3-2008 specification. See the *LogiCORE IP 10-Gigabit Ethernet PCS/PMA Product Guide* (PG068) [Ref 8] for more information.

AXI Interconnect (AXI_MM)

This AXI4 interconnect instance provides the high F_{MAX} and throughput required by the design with a 256-bit core data width and a 200 MHz clock frequency. The AXI4 interconnect core data width and clock frequency matches the capabilities of the attached AXI4 MIG so that width and clock converters are not required. Setting the AXI4 interconnect core data width and clock

frequency below the native width and clock frequency of the memory controller creates a bandwidth bottleneck within the system. To help meet the timing requirements of a 256-bit AXI4 interface at 200 MHz, a rank of register slices are enabled between the AXI_MM interconnect and the AXI4 MIG. Together, the AXI4 interconnect and AXI4 MIG form a 4-port AXI4 multi-port memory controller (MPMC) connected to four AXI4 external master connectors. The AXI4 interconnect configuration is consistent with the system performance optimization recommendations for an AXI4 MPMC-based system as described in the *AXI Reference Guide* [Ref 9].

Memory Interface Generator

The Memory Interface Generator forms the single slave connected to the AXI4 Interconnect. The MIG AXI4 interface is 512 bits wide and runs at 200 MHz with disabled narrow burst support for optimal throughput and timing. This configuration matches the native AXI4 interface clock and width corresponding to a 64-bit DDR3 DIMM with an 800 MHz memory clock which is the nominal performance of the memory controller for a Kintex-7 device with a -2 speed grade. Register slices are enabled to ensure that the interface meets timing at 200 MHz. These settings ensure that a high degree of transaction pipelining is active to improve system throughput. See the *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 10] for more information.

AXI Interconnect (AXI Lite)

The MicroBlaze processor data peripheral (DP) interface master writes and reads control and status information to all AXI4-Lite slave registers in the design. Because these are 32-bit interconnects and do not require high F_{MAX} and throughput, they are connected to a slower F_{MAX} portion of the design by a separate AXI Interconnect. The AXI4-Lite Interconnect block is configured for shared-access mode because of the lower throughput in this portion of the design and to allow area to be optimized over performance on this interconnect block. Also, this interconnect is clocked at 100 MHz to ensure that synchronous integer ratio clock converters in the AXI Interconnect can be used which offer lower latency and less area than asynchronous clock converters. The AXI_Lite Interconnect slaves consist of AXI UART Lite, two 10-Gigabit Ethernet MAC and SMPTE 2022-5/6 Video Over IP transmitter or receiver cores.

Software Applications

The software application initializes the video over IP transmitter and receiver platforms. After software initialization, commands can be selected from the menu of the UART terminal display.

Application-level software and the drivers for controlling the system are written in C. Alternatively, drivers and application software can write directly to the IP control registers.

The software configures the register values as shown in Table 5 and Table 6. The base address of the register set is the AXI4-Lite bridge base address (0x70E00000). Registers not shown in the tables are not initialized and remain at their respective default values.

Table 5: **Initialized VoIP TX Register Values**

Offset	Register Name	Value
General Space		
0x010	Primary Mac Address (Low)	0x000000AA
0x014	Primary Mac Address (High)	0x00000000
0x018	Secondary Mac Address (Low)	0x000000CC
0x01C	Secondary Mac Address (High)	0x00000000
0x028	Memory Base Address 3-MSb	0x00000006
0x030	hitless_config	0x00000000

Table 5: **Initialized VoIP TX Register Values *(Cont'd)***

Offset	Register Name	Value		
Primary Channel Space		**Ch1**	**Ch2**	**Ch3**
0x080	ip_header	0x00006480		
0x084	vlan_tag_info	0x0000AB00	0x0000AB10	0x0000AB20
0x088	dest_mac_low_addr	0x000000FF		
0x08C	dest_mac_high_addr	0x00000000		
0x090	dest_ip_host_low_addr	0xC0A80064		
0x0A0	src_ip_host_low_addr	0xC0A80032		
0x0B0	udp_src_port	0x10	0x20	0x30
0x0B4	udp_dest_port	0x10	0x20	0x30
0x0D0	transmit_en	0x1		
0x0D8	ip_header_fec	0x00006480		
0x100	chan_en	0x1		
0x110	video_para_config	0x1		
0x118	ssrc	0x12345600	0x12345610	0x12345620
0x11C	FEC_config	0x6		
0x124	FEC_L	0x4D		
0x128	FEC_D	0x4D		
Secondary Channel Space		**Ch1**	**Ch2**	**Ch3**
0x084	vlan_tag_info	0x0000AB00	0x0000AB10	0x0000AB20
0x088	dest_mac_low_addr	0x000000EE		
0x08C	dest_mac_high_addr	0x00000000		
0x090	dest_ip_host_low_addr	0xC0A80164		
0x0A0	src_ip_host_low_addr	0xC0A80132		
0x0B0	udp_src_port	0x10	0x20	0x30
0x0B4	udp_dest_port	0x10	0x20	0x30
0x0D0	transmit_en	0x1		
0x0D8	ip_header_fec	0x00006480		

Table 6: **Initialized VoIP RX Register Values**

Offset	Register Name	Value		
General Space				
0x028	network_path_differential	0x00149970		
0x034	fec_buf_base_addr	0xD8000000		
0x038	fec_buf_pool_size	0x0457b000		
Primary Channel Space		**Ch1**	**Ch2**	**Ch3**

Table 6: **Initialized VoIP RX Register Values *(Cont'd)***

Offset	Register Name	Value		
0x088	match_vlan	0x0000AB00	0x0000AB10	0x0000AB20
0x08C	match_dest_ip_addr	0xC0A80064		
0x09C	match_src_ip_addr	0xC0A80032		
0x0AC	match_src_port	0x10	0x20	0x30
0x0B0	match_dest_port	0x10	0x20	0x30
0x0B4	match_sel	0x10		
0x100	chan_en	0x1		
0x110	match_ssrc	0x12345600	0x12345610	0x12345620
0x11C	playout_delay	0x002932E0		
0x12C	media_buf_base_addr	0xC0000000	0xC8000000	0xD0000000
0x118	media_pkt_buf_size	0x0000FFFF		
Secondary Channel Space		**Ch1**	**Ch2**	**Ch3**
0x088	match_vlan	0x0000AB00	0x0000AB10	0x0000AB20
0x08C	match_dest_ip_addr	0xC0A80164		
0x09C	match_src_ip_addr	0xC0A80132		
0x0AC	match_src_port	0x10	0x20	0x30
0x0B0	match_dest_port	0x10	0x20	0x30
0x0B4	match_sel	0x10		

Software Process Flow

Figure 6 shows the video over IP transmitter and receiver overall software process.

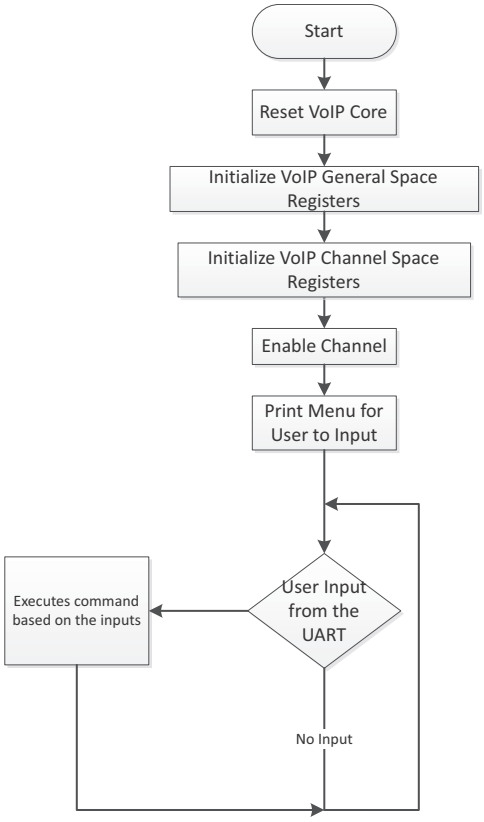

Figure 6: **Video Over IP Transmitter and Receiver Overall Software Process**

Note: Channel enable is asserted last to ensure proper core operation after reset.

Performing software reset while the core has been configured and running, follow steps as shown in Figure 7.

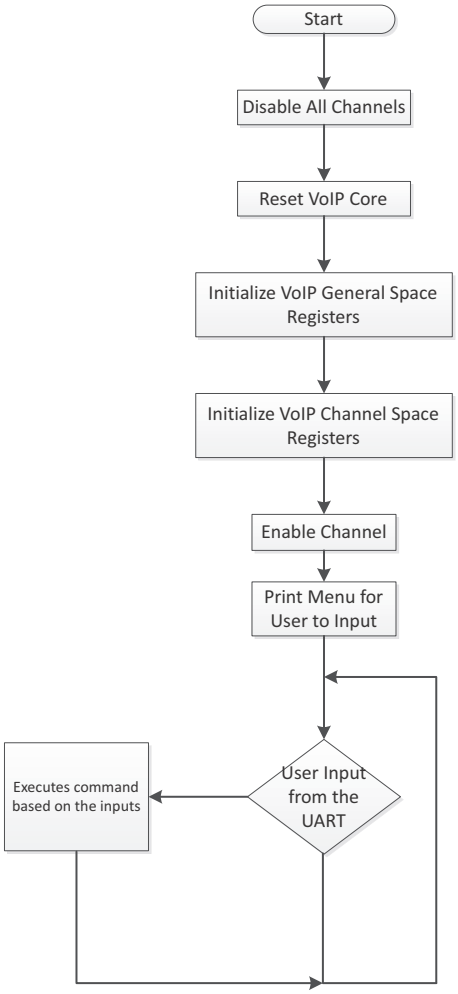

Figure 7: **Video Over IP Transmitter and Receiver Software Reset Process**

Note: Channel Reset can be performed by setting bit-0 to low at `chan_en` register (register offset 0x100).

Note: The core able to support changes of video stream (without performing channel reset) if the Video Format meets the register setting has been configured as stated in the *LogiCORE IP SMPTE 2022-5/6 Video over IP Receiver Product Guide* (PG033) [Ref 5], Memory Requirement and Register Configuration section.

Executing the Reference Design in Hardware

This section provides instructions detailing the setup and operation of the reference design on the KC705 evaluation board using the Inrevium TB-FMCH-3GSDI2A mezzanine boards (Figure 8 and Figure 9).

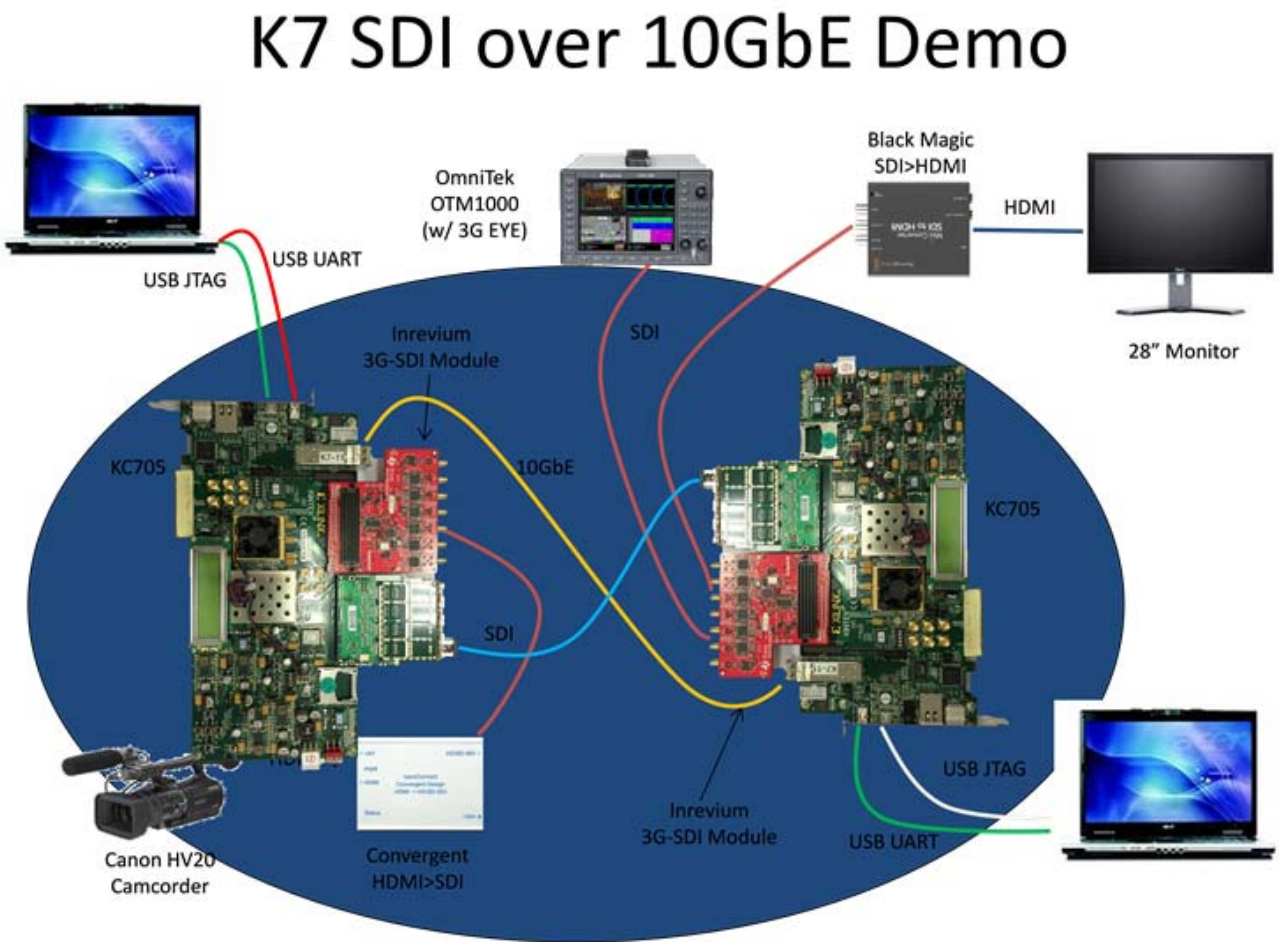

Figure 8: **Video Over IP System Setup**

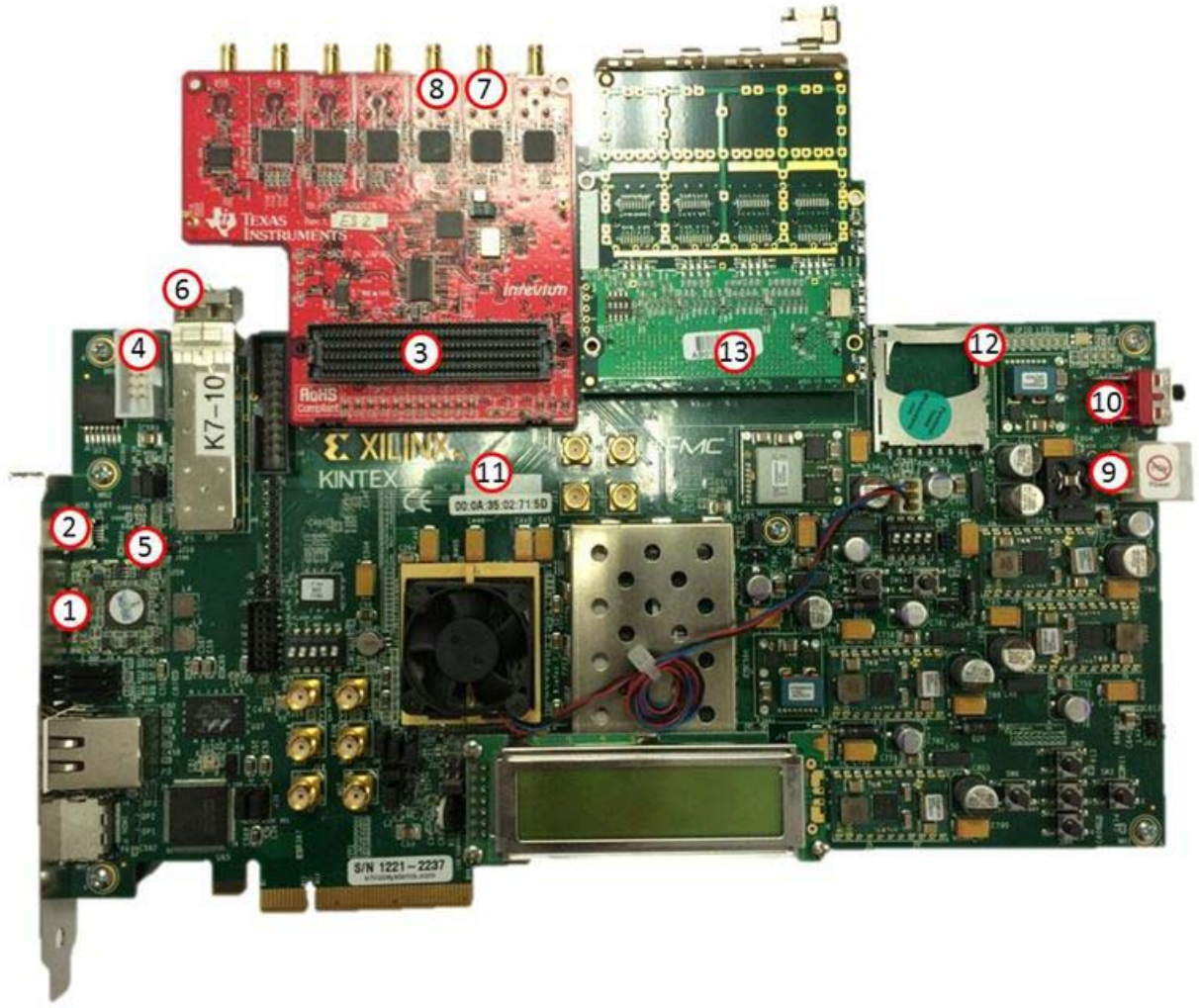

Figure 9: **KC705 and TB-FMCH-3FSDI2A Boards**

In these instructions, numbers in parentheses correspond to callout numbers in Figure 9.

1. Connect a USB cable from the host PC to the USB JTAG port (1). Ensure the appropriate device drivers are installed.
2. Connect a second USB cable from the host PC to the USB UART port (2). Ensure that USB UART drivers described in the section Hardware Requirements have been installed.
3. Connect TB-FMCH-3GSDI2A board to the HPC-FMC of KC705 (3).
4. Ensure that the payload ID is enabled in the SDI stream connected to the HPC-FMC of KC705 (3).
5. Connect an SFP+ Optical Transceiver to the SFP slot (4).
6. Connect a jumper to J4 (5) to enable SFP+ transmitter
7. Connect one end of the optical cable (6) to the SFP+ of VoIP transmitter board, the other end to the SFP+ of VoIP receiver board.
8. Connect the CH0-TX, CH1-TX & CH2 ports of TB-FMCH-3GSDI2A (7) to the SDI video monitor if the KC705 board is the VoIP receiver.
9. Connect the CH0-RX, CH1-RX & CH2 ports of TB-FMCH-3GSDI2A (8) to the SDI video generator if the KC705 board is the VoIP transmitter.
10. Connect the KC705 board to a power supply slot J49 (9).

11. Switch on the KC705 board (10).
12. Make sure that the HW-KC705 board revision (11) is the same for VoIP TX and RX platforms.

    Note: 10Gb ETH PCS/PMA MGT P and N pins were swapped on board revisions below 1.1 (e.g. 1.0 & C), this will cause optical signal compatibility issues on standard equipment.

    Workaround: MGT TX and RX ports need to be inversed and is done by tying the TXPOLARITY and RXPOLARITY to VCC in the `ten_gig_eth_pcs_pma_0_gtwizard_10gbaser_gt.VHD` RTL in `ten_gig_eth_pcs_pma_0` IP `synth` folder.
13. Connect one end of the optical cable (14) to the SFP+ of VoIP transmitter FM-S14 (13) board, the other end to the SFP+ of VoIP receiver FM-S14 (13) board.
14. Ensure all LEDs (12) are lit (refer to Debugging section for details).
15. Start a terminal program (HyperTerminal, for example) on the host PC with these settings:
    - Baud Rate: **115200**
    - Data Bits: **8**
    - Parity: **None**
    - Stop Bits: **1**
    - Flow Control: **None**

Executing the Reference System Using the Pre-Built Bitstream and the Compiled Software Application

This section details the steps necessary to execute the system using the files in the `ready_for_download` directory:

1. Launch the Xilinx Microprocessor Debugger by selecting **Start > All Programs > Xilinx Design Tools > Vivado 2015.2**.
2. In the Xilinx command shell window, change to the `ready_for_download` directory:

   VoIP_TX:
   ```
   >cd <unzip_dir>/kc705_smpte2022_56_tx/ready_for_download
   ```
   VoIP_RX:
   ```
   >cd <unzip_dir>/kc705_smpte2022_56_rx/ready_for_download
   ```
3. Download the bitstream to the FPGA:

   ```
   XMD% fpga -f download.bit
   ```
4. Exit the XMD command prompt:

   ```
   XMD% exit
   ```

   Note: The software application starts immediately on completion of FPGA configuration. The executable file (.elf) is embedded in the configuration file (`download.bit`).

Running the Hardware and Software

The HyperTerminal screen of VoIP transmitter and receiver displays the output in VoIP_TX UART Display and VoIP_RX UART Display respectively.

VoIP_TX UART Display

```
  _____  _____
 /    /\/    /
/___/  \  /    Xilinx Inc.
\   \   \/     V_SMPTE2022_567_TX 10G
 \   \         Vivado Reference Design
 /   /         Created: July 24, 2015
/___/   /\     Copyright (c) 2015 Xilinx, Inc.
\   \  /  \    All rights reserved.
 \___\/\___\

VoIP TX Reset

VoIP TX Initializing...

EMAC Fault Inhibit    : Enabled
Primary MAC Address   : 00-00-00-00-00-AA
Secondary MAC Address : 00-00-00-00-00-CC
Hitless Protection    : Enabled
VoIP TX Initialization done

Initializing for Primary Channel 1
IP Version:       IPv4
MEDIA TTL:        128
MEDIA TOS:        100
FEC TTL:          128
FEC TOS:          100
Dest MAC Address: 00-00-00-00-00-FF
Source IP Addr:   192.168.0.50
Dest IP Addr:     192.168.0.100
Source Port:      0x0010
Dest Port:        0x0010
VLAN:             Disabled
VLAN Tag:         0xAB00
SSRC:             0x12345600
Time Stamp        Enabled
FEC Size:         77x77
FEC On/Off:       On
FEC Level:        B
Block Align:      Block Aligned
Trasmit:          Enable
Primary Channel 1 Initialization Done

Initializing For Secondary Channel 1
IP Version:       IPv4
MEDIA TTL:        128
MEDIA TOS:        100
FEC TTL:          128
FEC TOS:          100
Dest MAC Address: 00-00-00-00-00-EE
Source IP Addr:   192.168.1.50
Dest IP Addr:     192.168.1.100
Source Port:      0x0010
Dest Port:        0x0010
VLAN:             Disabled
VLAN Tag:         0xAB00
SSRC:             0x12345600
Time Stamp        Enabled
FEC Size:         77x77
FEC On/Off:       On
FEC Level:        B
```

```
Block Align:      Block Aligned
Trasmit:          Enable
Secondary Channel 1 Initialization Done
VoIP TX Channel 1 Enabled
VoIP TX Configuration for Channel 1 Initialization Done

Initializing for Primary Channel 2
IP Version:       IPv4
MEDIA TTL:        128
MEDIA TOS:        100
FEC TTL:          128
FEC TOS:          100
Dest MAC Address: 00-00-00-00-00-FF
Source IP Addr:   192.168.0.50
Dest IP Addr:     192.168.0.100
Source Port:      0x0020
Dest Port:        0x0020
VLAN:             Disabled
VLAN Tag:         0xAB10
SSRC:             0x12345610
Time Stamp        Enabled
FEC Size:         77x77
FEC On/Off:       On
FEC Level:        B
Block Align:      Block Aligned
Trasmit:          Enable
Primary Channel 2 Initialization Done

Initializing For Secondary Channel 2
IP Version:       IPv4
MEDIA TTL:        128
MEDIA TOS:        100
FEC TTL:          128
FEC TOS:          100
Dest MAC Address: 00-00-00-00-00-EE
Source IP Addr:   192.168.1.50
Dest IP Addr:     192.168.1.100
Source Port:      0x0020
Dest Port:        0x0020
VLAN:             Disabled
VLAN Tag:         0xAB10
SSRC:             0x12345610
Time Stamp        Enabled
FEC Size:         77x77
FEC On/Off:       On
FEC Level:        B
Block Align:      Block Aligned
Trasmit:          Enable
Secondary Channel 2 Initialization Done
VoIP TX Channel 2 Enabled
VoIP TX Configuration for Channel 2 Initialization Done

Initializing for Primary Channel 3
IP Version:       IPv4
MEDIA TTL:        128
MEDIA TOS:        100
FEC TTL:          128
FEC TOS:          100
Dest MAC Address: 00-00-00-00-00-FF
Source IP Addr:   192.168.0.50
Dest IP Addr:     192.168.0.100
Source Port:      0x0030
```

```
Dest Port:         0x0030
VLAN:              Disabled
VLAN Tag:          0xAB20
SSRC:              0x12345620
Time Stamp         Enabled
FEC Size:          77x77
FEC On/Off:        On
FEC Level:         B
Block Align:       Block Aligned
Trasmit:           Enable
Primary Channel 3 Initialization Done
Initializing For Secondary Channel 3
IP Version:        IPv4
MEDIA TTL:         128
MEDIA TOS:         100
FEC TTL:           128
FEC TOS:           100
Dest MAC Address: 00-00-00-00-00-EE
Source IP Addr:    192.168.1.50
Dest IP Addr:      192.168.1.100
Source Port:       0x0030
Dest Port:         0x0030
VLAN:              Disabled
VLAN Tag:          0xAB20
SSRC:              0x12345620
Time Stamp         Enabled
FEC Size:          77x77
FEC On/Off:        On
FEC Level:         B
Block Align:       Block Aligned
Trasmit:           Enable
Secondary Channel 3 Initialization Done
VoIP TX Channel 3 Enabled
VoIP TX Configuration for Channel 3 Initialization Done

-----------------------
-- VoIP TX Main Menu --
-----------------------

 Select option
 1 = Reset Core
 2 = Initialize Core
 3 = Change Primary MAC Address
 4 = Change Secondary MAC Address
 5 ------------------
>
```

You can choose one of nine options that displayed in the VoIP TX main menu.

Note: Enables single (downstream) optical link from TX to RX by turning off the Hitless Protection (Option 5)

Select channel screen display:

```
-----------------------
--  Select Channel   --
-----------------------
 Primary Channels
 1 = Channel 1
 2 = Channel 2
 3 = Channel 3
 Secondary Channels
 a = Channel 1
```

```
 b = Channel 2
 c = Channel 3
------------------
>
```

You can choose one of three channels for each links (Primary/Secondary) or go back to main menu. After selecting any of these available channels, the **Select Option** menu is displayed and you can choose one of these options from the following menu list.

```
----------------------
--   Select Option   --
----------------------
 1 = Channel Init
 2 = Channel Enable/Disable
 3 = Change Host IP Address
 4 = VLAN En/Disable
 5 = Change VLAN Tag
 6 = Set Dest MAC Addr
 7 = Set Dest IP Addr
 8 = Set Source UDP Port
 9 = Set Dest UDP Port
 0 = Set SSRC
 a = FEC On/Off
 b = Toggle FEC Level
 c = Set Column FEC
 d = Set Row FEC
 e = Toggle Block Alignment
 f = Time Stamp Include En/Disable
 t = Transmit Enable/Disable
 r = Transmit Packet Count Stat Reset
 p = Probe Status
 m = Main Menu
 s = Channel Select
------------------
>
```

VoIP_RX UART Display

```
   ____  ____
  /   /\/   /
 /___/  \  /   Xilinx Inc.
 \   \   \/    V_SMPTE2022_567_RX 10G
  \   \        Vivado Reference Design
  /   /        Created: July 24, 2015
 /___/   /\    Copyright (c) 2015 Xilinx, Inc.
 \   \  /  \   All rights reserved.
  \___\/\___\

VoIP RX Reset

VoIP RX Initializing...

EMAC Fault Inhibit: Enabled

Network Diff. Path:      1350000
FEC Base Address:        0xD8000000
FEC Pool Size:           72855552
VoIP RX General Space Initialization done

Initializing Channel 1
Primary Stream Configure
IP Version:              IPv4
Match VLAN:              Disable
```

```
Match VLAN Tag:          0xAB00
Match Dest IP Addr:      192.168.0.100
Match Host IP Addr:      192.168.0.50
Match Dest Port:         0x0010
Match Source Port:       0x0010
Match SSRC:              0x12345600

Match Select:
   SSRC:                  Off
   Dest UDP:              On
   Source UDP:            Off
   Dest IP:               Off
   Src IP:                Off
   VLAN:                  Off

Secondary Stream Configure
IP Version:              IPv4
Match VLAN:              Disable
Match VLAN Tag:          0xAB00
Match Dest IP Addr:      192.168.0.100
Match Host IP Addr:      192.168.0.50
Match Dest Port:         0x0010
Match Source Port:       0x0010
Match SSRC:              0x00000000

Match Select:
   SSRC:                  Off
   Dest UDP:              On
   Source UDP:            Off
   Dest IP:               Off
   Src IP:                Off
   VLAN:                  Off

General Channel Setting:
Playout Delay:            2700000
Channel Buffer Address:   0xC0000000
Channel Buffer Size:      65535
Timestamp Bypass:         Disable
Channel 1 Enabled
Channel 1 Initialization Done

Initializing Channel 2
Primary Stream Configure
IP Version:              IPv4
Match VLAN:              Disable
Match VLAN Tag:          0xAB10
Match Dest IP Addr:      192.168.0.100
Match Host IP Addr:      192.168.0.50
Match Dest Port:         0x0020
Match Source Port:       0x0020
Match SSRC:              0x12345610

Match Select:
   SSRC:                  Off
   Dest UDP:              On
   Source UDP:            Off
   Dest IP:               Off
   Src IP:                Off
   VLAN:                  Off

Secondary Stream Configure
IP Version:              IPv4
```

```
Match VLAN:              Disable
Match VLAN Tag:          0xAB10
Match Dest IP Addr:      192.168.0.100
Match Host IP Addr:      192.168.0.50
Match Dest Port:         0x0020
Match Source Port:       0x0020
Match SSRC:              0x00000000

Match Select:
   SSRC:                  Off
   Dest UDP:              On
   Source UDP:            Off
   Dest IP:               Off
   Src IP:                Off
   VLAN:                  Off

General Channel Setting:
Playout Delay:             2700000
Channel Buffer Address:    0xC8000000
Channel Buffer Size:       65535
Timestamp Bypass:          Disable
Channel 2 Enabled
Channel 2 Initialization Done

Initializing Channel 3
Primary Stream Configure
IP Version:              IPv4
Match VLAN:              Disable
Match VLAN Tag:          0xAB20
Match Dest IP Addr:      192.168.0.100
Match Host IP Addr:      192.168.0.50
Match Dest Port:         0x0030
Match Source Port:       0x0030
Match SSRC:              0x12345620

Match Select:
   SSRC:                  Off
   Dest UDP:              On
   Source UDP:            Off
   Dest IP:               Off
   Src IP:                Off
   VLAN:                  Off

Secondary Stream Configure
IP Version:              IPv4
Match VLAN:              Disable
Match VLAN Tag:          0xAB20
Match Dest IP Addr:      192.168.0.100
Match Host IP Addr:      192.168.0.50
Match Dest Port:         0x0030
Match Source Port:       0x0030
Match SSRC:              0x00000000

Match Select:
   SSRC:                  Off
   Dest UDP:              On
   Source UDP:            Off
   Dest IP:               Off
   Src IP:                Off
   VLAN:                  Off

General Channel Setting:
```

```
Playout Delay:            2700000
Channel Buffer Address:   0xD0000000
Channel Buffer Size:      65535
Timestamp Bypass:         Disable
Channel 3 Enabled
Channel 3 Initialization Done

-----------------------
-- VoIP RX Main Menu --
-----------------------

 Select option
 1 = Reset Core
 2 = Initialize Core
 3 = 10G MAC Fault Inhibit On/Off
 r = Reset General Space Stat Counters
 s = Configure Channel
 p = Probe Current Settings
 ? = help
------------------
>
```

You can choose one of seven options that displayed in the VoIP RX main menu.

Select channel screen display:

```
-----------------------
--  Select Channel   --
-----------------------
 Primary Channels
 1 = Channel 1
 2 = Channel 2
 3 = Channel 3
 Secondary Channels
 a = Channel 1
 b = Channel 2
 c = Channel 3
------------------
>
```

You can choose one of three channels for each links (Primary/Secondary) or go back to main menu. After selecting any of these available channels, the **Select Option** menu is displayed and you can choose one of these options from the following menu list.

```
-----------------------
--   Select Option   --
-----------------------
 1 = Channel Init
 2 = Channel Enable/Disable
 3 = Match VLAN On/Off
 4 = Timestamp Bypass On/Off
 5 = Channel Filter Change
 p = Probe Status
 q = Probe Statistic
 r = Channel Statistics Reset
 m = Main Menu
 s = Channel Select
------------------
>
```

Rebuilding and Compiling the Reference Design

This section covers rebuilding the hardware design. Before rebuilding the project, ensure that the licenses for the SMPTE 2022-5/6 Video Over IP transmitter and receiver cores, 10-Gigabit Ethernet PCS/PMA and 10-Gigabit Ethernet MAC are installed.

Note: To ensure that no compilation errors occur due to long file paths, unzip the project files as close as possible to the root directory. For example, with a typical Windows installation, unzip the files at C:\.

Generating the Programming File with Vivado Design Suite 2015.2

1. Start Vivado Design Suite.
2. At the Tcl Console, change to the workspace directory by typing:

   VoIP_TX:
   >cd <unzip dir>/kc705_smpte2022_56_tx

   VoIP_RX:
   >cd <unzip dir>/kc705_smpte2022_56_rx
3. To create, compile and generate the project bitstream, run the `all.tcl` script by typing at the Tcl Console:

   >source all.tcl

Compiling the Software with SDK

The SDK environment must be prepared after the completion of "all.tcl" script. Do this by exporting the project's hardware information and importing the SDK source codes.

1. Export hardware: In Vivado 2015.2 select, **File > Export > Export Hardware**.
   a. In the Export Hardware pop-up window, Check Include bitstream option.
   b. Set the Export to: field correspondingly:

      VoIP_TX:
      <unzip dir>\kc705_smpte2022_56_tx\SW\SDK_Workspace

      VoIP_RX:
      <unzip dir>\kc705_smpte2022_56_rx\SW\SDK_Workspace
2. Launch Xilinx SDK 2015.2 from Vivado 2015.2 by selecting, File > Launch SDK.
   a. In the Launch SDK window, set the Exported Location field and Workspace field accordingly:

      VoIP_TX:

      <unzip dir>\kc705_smpte2022_56_tx\SW\SDK_Workspace

      VoIP_RX:

      <unzip dir>\kc705_smpte2022_56_rx\SW\SDK_Workspace
   b. Create a new Board Support Package in SDK by selecting, **File > New > Board Support Package**.
   c. In the Xilinx Board Support Package Project window, set the Project name to **voip_bsp**.
   d. Click **Finish**.
   e. In the Board Support Package Settings window, click **OK**.
3. Import SDK Sources: In SDK 2015.2 select, File > Import.
   a. In the Import pop-up window, select **General > Existing Projects into Workspace**.
   b. Click **Next**.
   c. Click on **Browse** button, and make sure that it points to the corresponding folders

      VoIP_TX:
      <unzip dir>\kc705_smpte2022_56_tx\SW\SDK_Workspace

VoIP_RX:

```
<unzip dir>\kc705_smpte2022_56_rx\SW\SDK_Workspace
```

d. Click **OK**.

e. Make sure voip_tx/rx are checked.

f. Click **Finish**.

The BSP and software applications compile at this step. The process takes 2 to 5 minutes. The existing software applications can now be modified and new software applications can be created in the SDK.

Running the Hardware and Software through the SDK

1. Select **Xilinx Tools > Program FPGA**.

Note: Ensure the Hardware Platform is the same as written in Project Field, e.g: hw

Note: Ensure the connection is set to Local

Note: Ensure bootloop is used for system_basic_i/microblaze_1.

2. Click **Program**.
3. In the Project Explorer window, right click and select:

VoIP_TX

```
voip_tx > Run As > Launch on Hardware (GDB)
```

VoIP_RX

```
voip_rx > Run As > Launch on Hardware (GDB)
```

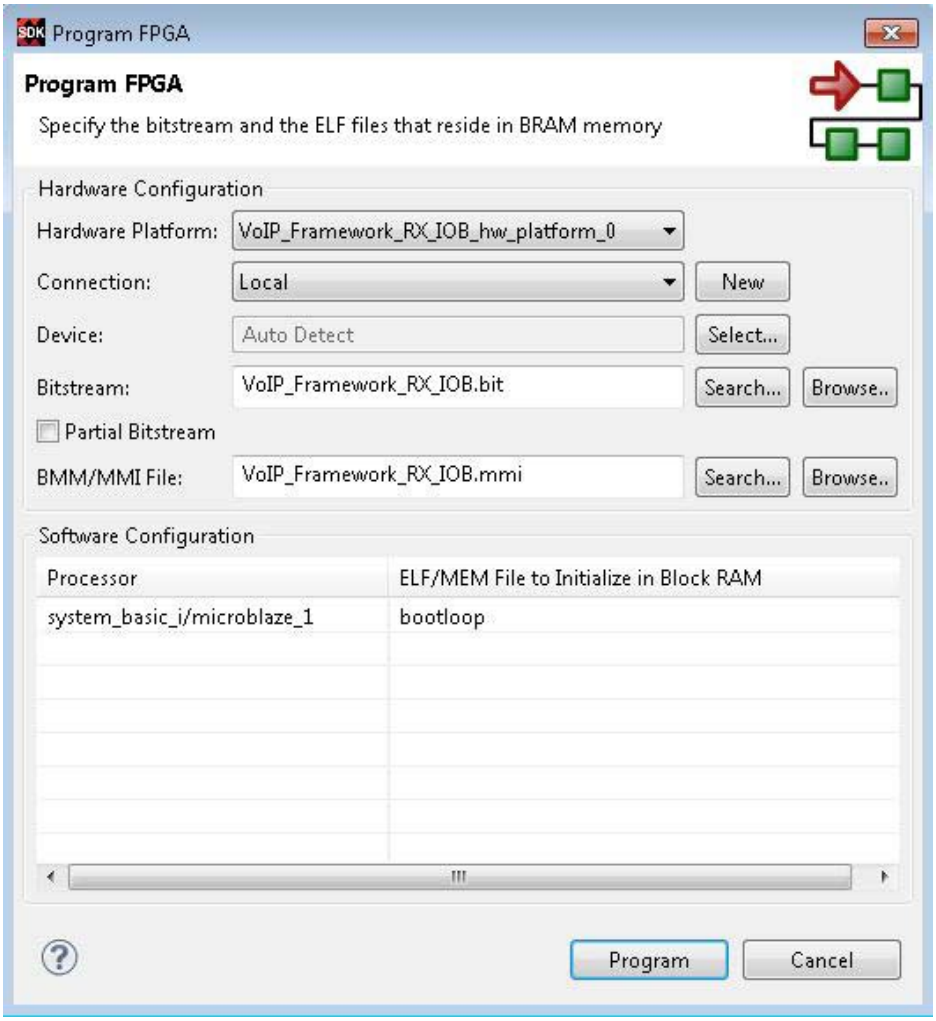

Figure 10: **JTAG Configuration Settings**

Note: The choice is provided whether to run the software application either from MIG or block RAM by editing the linker script (`lscript.ld`) under the `voip_tx/rx'src` folder. The default setting in the linker script is to execute the software application from block RAM.

The MIG base address in the linker script is set to `0xF8000000` to ensure a generous separation from the memory address range of the video over IP transmitter or receiver cores. For memory requirement details, refer to *LogiCORE IP SMPTE 2022-5/6 Video over IP Transmitter Product Guide* (PG032) [Ref 4] and *LogiCORE IP SMPTE 2022-5/6 Video over IP Receiver Product Guide* (PG033) [Ref 5].

Debugging

The onboard GPIO LEDs can be used for quick troubleshooting. During normal operation, all LEDs should turn on asynchronously within five seconds after completion of the bitstream configuration. The LED representations are shown in Table 7.

Table 7: **KC705 GPIO LED Designations for Transmitter and Receiver**

GPIO_LED	Designation
0	10G PCS/PMA Link Up for Primary Link
1	10G PCS/PMA Link Up for Secondary Link
2	10G PCS/PMA Reset Done for Primary Link
3	10G PCS/PMA Reset Done for Secondary Link

Table 7: **KC705 GPIO LED Designations for Transmitter and Receiver *(Cont'd)***

GPIO_LED	Designation
4	Si5324 Loss-of-Lock (Inverted)
5	Clock 100 MHz Locked
6	Clock 200 MHz Locked
7	DDR Memory Initialization Done

GPIO_LED 0 and 1: When this LED is Low, it can be an indication that J4 jumper of the opposite platform is not in place. For example, when VoIP_TX' LED 0 is Low, examine the VoIP_RX' J4 jumper setting.

GPIO_LED 7: When this LED is Low, it means that the memory subsystem did not successfully initialize. Sometimes switching development board helps to get around this problem.

Note: Ensure that the payload ID is turn on from the source.

After the system is brought up, IP (SMPTE 2022-56 TX and RX) debug must be performed. Refer to the *Core Debug* section in *LogiCORE IP SMPTE 2022-5/6 Video over IP Transmitter Product Guide* (PG032) [Ref 4] and *LogiCORE IP SMPTE 2022-5/6 Video over IP Receiver Product Guide* (PG033) [Ref 5].

Reference Design

The reference design files for this application note can be downloaded from:

https://secure.xilinx.com/webreg/clickthrough.do?cid=355405, registration required.

Table 8 shows the reference design checklist.

Table 8: **Reference Design Checklist**

Parameter	Description
General	
Developer name	Ilias Ibrahim, Gilbert Magnaye, Josh Poh, Tom Sun
Target devices (stepping level, ES, production, speed grades)	Kintex-7 FPGA
Source code provided	Yes
Source code format	VHDL and Verilog (some sources encrypted)
Design uses code/IP from existing Xilinx application note/reference designs, CORE Generator software, or third party	Cores generated from Vivado IP Catalog
Simulation	
Functional simulation performed	N/A
Timing simulation performed	N/A
Test bench used for functional and timing simulations	N/A
Test bench format	N/A
Simulator software/version used	N/A
SPICE/IBIS simulations	N/A
Implementation	
Synthesis software tools/version used	Vivado 2015.2

Table 8: **Reference Design Checklist *(Cont'd)***

Parameter	Description
Implementation software tools/versions used	Vivado 2015.2
Static timing analysis performed	Yes
Hardware Verification	
Hardware verified	Yes
Hardware platform used for verification	Xilinx Kintex-7 FPGA KC705 Evaluation Kit

Design Characteristics

The reference design is implemented in a Kintex-7 FPGA (XC7K325TFFG900-2) using the Vivado Design Suite 2015.2

Utilization and Performance

Table 9 shows the resource utilization for the video over IP transmitter reference design.

Table 9: **Video Over IP Transmitter Resource Utilization**

Resource	Utilization	Available	Percent Utilization
Slice LUTs	72796	203800	35.72
Slice Registers	86947	407600	21.33
Memory	233	445	52.36
DSP	3	840	0.36
IO	163	500	32.60
GT Channels	5	16	31.25
Clocking	21	32	65.62

Table 10 shows the resource utilization for the video over IP receiver reference design.

Table 10: **Video Over IP Receiver Resource Utilization**

Resource	Utilization	Available	Percent Utilization
Slice LUTs	73052	203800	35.84
Slice Registers	93160	407600	22.86
Memory	224	445	50.34
DSP	3	840	0.36
IO	163	500	32.60
GT Channels	5	16	31.25
Clocking	21	32	65.62

Note: Device resource utilization results depend on the implementation tool versions. Exact results can vary. These numbers should be used as a guideline.

Conclusion

This application note describes a video over IP network system using various Xilinx IP cores. The reference design demonstrates the ability of the SMPTE 2022-5/6 Video Over IP cores to encapsulate and de-encapsulate multiple SDI streams and transport it through a 10 Gb/s Ethernet pipe. The utilization of the Ethernet bandwidth is over 90% with three 3G-SDI videos and Forward Error Correction (FEC) with matrix size of 77x77. The reference design can

perform recovery of a limited number of Ethernet packets when impairment is introduced into the network with the FEC engine turned on.

References

This application note uses these references:

1. Kintex-7 FPGA KC705 Evaluation Kit product page
2. Inrevium TB-FMCH-3GSDI2A 3G/HD/SD 3GSDI FMC Connectivity mezzanine card product page
3. AMBA AXI4 specifications
4. *LogiCORE IP SMPTE 2022-5/6 Video over IP Transmitter Product Guide* (PG032)
5. *LogiCORE IP SMPTE 2022-5/6 Video over IP Receiver Product Guide* (PG033)
6. *SMPTE SD/HD/3G-SDI Product Guide* (PG071)
7. *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072)
8. *LogiCORE IP 10-Gigabit Ethernet PCS/PMA Product Guide* (PG068)
9. *AXI Reference Guide* (UG761)
10. *7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
11. Faster Technology FM-S14 Quad SFP/SFP+ transceiver FMC
    http://www.fastertechnology.com/products/fmc/fm-s14.html

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
09/30/2015	1.2	Updated to support SMPTE2022-56 RX v5.0 core additional port and other IP connectivity. Supports Vivado 2015.2.
02/01/2015	1.1	Updated for SMPTE 2022-5, 6, 7 Video over IP (Hitless) Reference Design.
01/28/2014	1.0	Initial Xilinx release.

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