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1G to 10G Ethernet Dynamic Switching Using Xilinx High Speed Serial IO Solution

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Summary

This application note targets Ethernet designs that require dynamic switching between 1 Gbps to 10 Gbps using high speed serial IO links. The design uses the Xilinx Ethernet solution suite along with a Xilinx Gigabit Transceiver (GT) to form the Ethernet interface. The same GT is used to interface with the gigabit Ethernet Physical Coding Sublayer/Physical Media Dependent (PCS/PMA) and the 10G Ethernet PCS/PMA IP core. The rate switching is handled using the Dynamic Reconfiguration Port (DRP) of GTs.

You can download the Reference Design Files for this application note from the Xilinx® website. For detailed information about the design files, see Reference Design.

Reference Design

Ethernet is the Media Access Control (MAC) specification that has been defined in the IEEE 802.3 and is a widely used universal standard deployed in network solution suite. Ethernet has found wide applicability due to its scalability across generations. As Ethernet is evolving from the earlier 10/100/1000 Mbps speed to 10 Gb/s and 100 Gb/s physical media speed, the network equipment already deployed across multiple network stations requires an upgrade.

To comply with the legacy Ethernet devices, Ethernet infrastructure must retain legacy Ethernet interfaces.The Ethernet interface (MAC) does not depend on physical media as long as the target speed is supported by the physical interface. For example, 1G and 10G Ethernet can use common optical interface for transporting Ethernet traffic over to the end point. To support both the legacy and the 10 Gb/s Ethernet interface using the same physical interface requires dynamic switching capability in the Ethernet PHY device.

Xilinx offers a vast portfolio of Ethernet IP including the 1G and 10G Ethernet MAC, and 1G and 10G Ethernet PCS/PMA. The Ethernet MAC has an AXI4-Stream compliant user interface and the MAC IP encapsulates the user payload in the form of Ethernet frames and transfers the data over to the PCS/PMA core. The PCS/PMA core uses physical layer encoding to convert the Ethernet frames to the specification defined encoded frames and sends the data over to the GT block. The PCS/PMA core performs GT initialization and the PHY housekeeping function.

The GT interface implements the serialization and de-serialization functionality. The serial bit period of the serialized data depends on the reference clock used in the GT and the GT PLL's clock dividers. To enable switching from 1G to 10G line rates, the PLL multipliers and dividers must be changed. The 1G and 10G links require different physical encoding schemes to be

performed, which are primarily implemented in the GT. The transceiver attributes used to configure protocol specific settings can be modified during runtime with the Dynamic Reconfiguration Port (DRP) interface. The DRP sequence is followed by a reset sequence of the GT which brings the transceiver back to normal operating condition.

This application note presents a solution to control the design using the DRP interface while switching from a 1G to 10G line rate.

Hardware

Figure 1 shows the re-use of the same transceiver for both 1G and 10G protocols. The GT channel (hard block) is separated from the PCS/PMA IP core and is configured using the DRP controller.

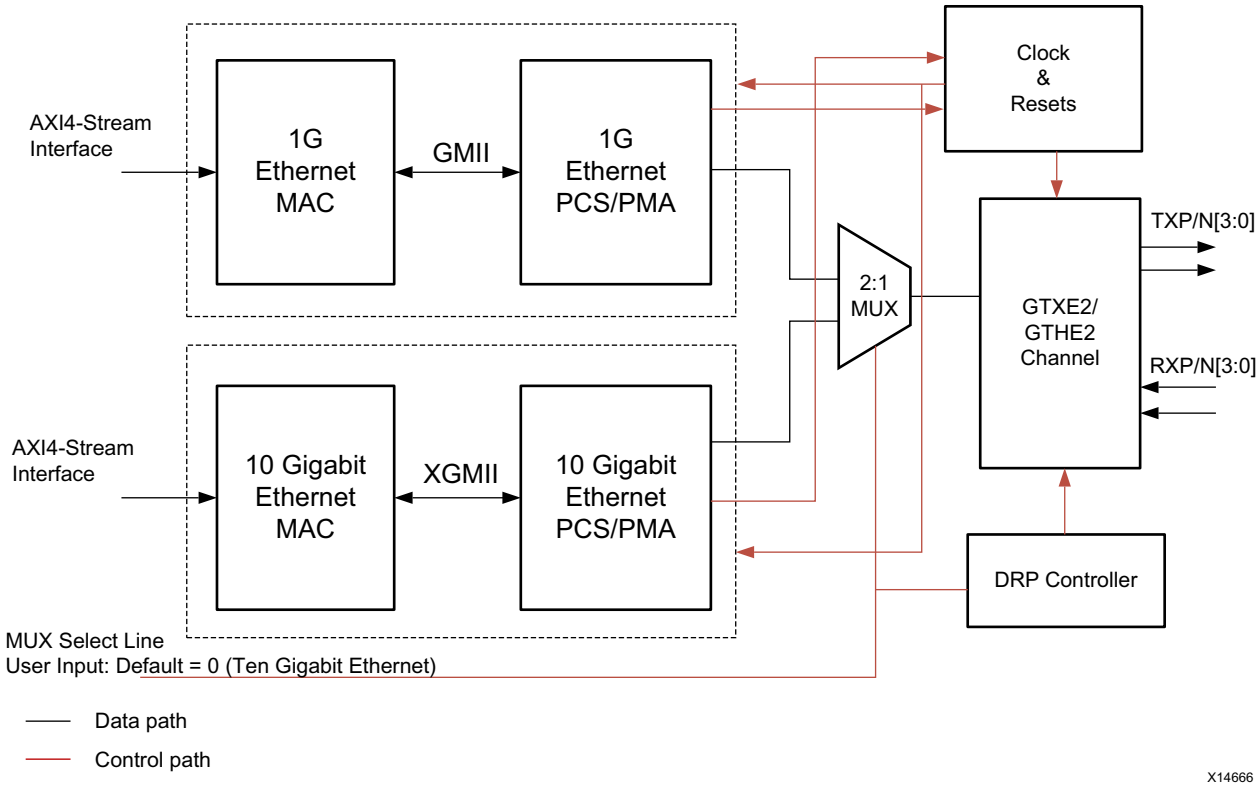

Figure 1: **Hardware Block Diagram**

The 1G/10G Ethernet reference design supports a throughput up to 10 Gb/s by varying its attributes. The DRP controller is designed to write suitable values in the appropriate register locations of the GT channel. This function enables configuration from 1G to 10G protocols and vice versa according to user input (select line to the 2:1 MUX).

The Ethernet packet is transferred via 1G MAC - 1G PCS/PMA and arrives at input 1 of the 2:1 MUX, while the 10G packet arrives at input 0 of the MUX. The user-driven select line of the MUX controls the routing of the Ethernet packet to the GT interface.

The DRP controller also takes in a select line as input to determine the configuration of the GT. Appropriate values are written to the corresponding registers through the DRP interface of the GT based on the select line input. The addresses and values to be written to the GT registers are

fixed, and they are hard-coded in the DRP controller. This allows the DRP controller to dynamically reconfigure the GT.

Tri-Mode Ethernet MAC

The Ethernet MAC is defined in IEEE 802.3-2012 specification clauses 2, 3 and 4. The MAC is responsible for the Ethernet framing protocols and error detection of these frames. The MAC is independent of, and can be connected to, any type of physical layer.

This IP is configured to support 1000 Mb/s and the management is through the configuration vector. The PHY layer is kept internal. The Ethernet and MDIO interface is customizable.

1G/2.5G Ethernet PCS/PMA or SGMII

The 1G/2.5G Ethernet PCS/PMA or SGMII core provides a flexible solution for connection to an Ethernet MAC or other custom logic. It supports the 1000 BASE-X Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) operation, as defined in the IEEE 802.3-2012 standard.

This IP is configured to support 1000 BASE-X standard and implements a device-specific transceiver interface. The shared logic is configured to be included in the example design.

10 Gigabit Ethernet MAC

The 10 Gigabit Ethernet MAC core connects to the PHY layer through an external XGMII. The PHY layers are managed through an optional MDIO STA master interface. Configuration of the core is done through a configuration vector. The Ethernet MAC core performs the Link function of the 10G Ethernet standard. The core supports 802.3 in transmit and receive directions. This IP is configured to support a 64-bit data path, and the physical layer interface is internal.

10 Gigabit Ethernet PCS/PMA 10GBASE-R

10GBASE-R/KR is a 10 Gb/s serial interface. It is intended to provide the Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) functionality between the 10-Gigabit Media Independent Interface (XGMII) interface on a 10 Gigabit Ethernet MAC and a Ten Gigabit Ethernet network PHY.

This IP is configured to support 10GBASE-R protocol with 64 bit data path and the shared logic is configured to be included the example design.

Clocking and Reset

The reference design uses a single 312.5 MHz reference clock for both 1G and 10G line rate selections. The VC709, KC705, and ZC706 reference designs source a 312.5 MHz reference from the FMC connector. The reference clock is connected as an input clock source to the GTXE2_CHANNEL/GTHE2_CHANNEL block's channel PLL instance for a 1G line rate and to the Quad PLL instance for the 10G line rate.

The PLL multipliers and dividers set the output TXOUTCLK and RXOUTCLK frequency as the serial line rate/parallel datapath width. TXOUTCLK and RXOUTCLK are used to generate TXUSERCLK/TXUSERCLK2 and RXUSRCLK/RXUSRCLK2 in the FPGA fabric. Figure 2 shows the clocking strategy used in the design.

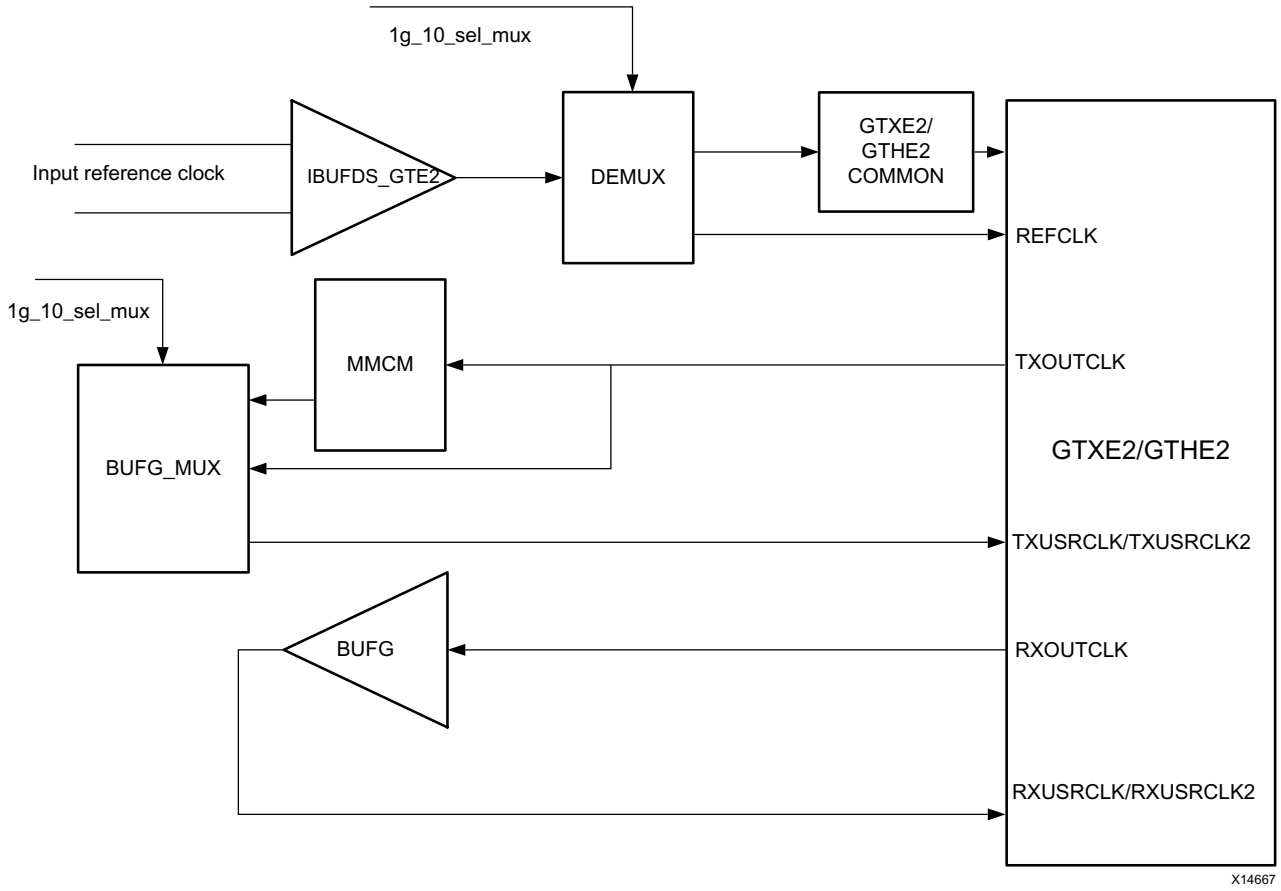

Figure 2: **Clock Strategy for 1G and 10G Line Rates**

Here is the summary of the clocking strategy used in the design:

- The 1G transceiver logic runs at TXUSRCLK/TXUSRCLK2 frequency which is 62.5 MHz clock for the 20-bit parallel datapath width.
- The 1G Ethernet PCS/PMA core works on a 10-bit interface at the user clock frequency of 125 MHz.
- The 10G Ethernet transceiver logic works at 322.23 MHz with a parallel datapath width of 32 bits.
- The 10G Ethernet PCS/PMA core operates at 156.25 MHz with a parallel data width of 64 bits.

Resetting the GTXE2/GTHE2 blocks used in the design is controlled by the reset sequence that is generated from the 1G/10G Ethernet PCS/PMA reference design. Once the DRP controller completes the attribute configuration for the 1G to 10G rate change and vice-versa, it generates a reset to the 1G/10G Ethernet PCS/PMA reference design which drives the reset sequence for the GTXE2/GTHE2 blocks used in the design.

DRP Controller

The DRP controller implements a FSM to write attribute values in the corresponding GT registers. The FSM is synchronized by a stable clock and is triggered by the MUX select line (user input). The attribute values of the GT for both 1G and 10G protocols are hard-coded and stored as a ROM in the DRP controller. The output of the DRP controller is mapped to the GT DRP interface. The FSM implemented follows the standard procedure to write or read the DRP registers of Xilinx 7 series device GTX, as mentioned in th *7 Series FPGAs GTX/GTH Transceivers User Guide* [Ref 5].

The DRP controller FSM flowchart is shown in Figure 3.

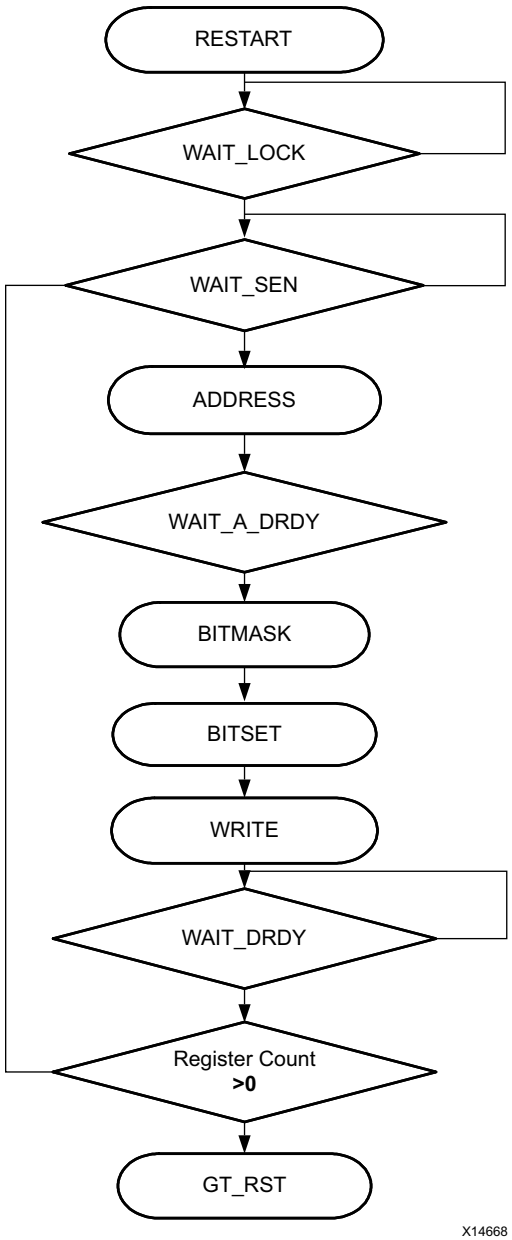

Figure 3: **Design Flow**

- RESTART: The ROM starting address and the output values are initialized to zero.

- WAIT_LOCK: The FSM polls for CPLL lock (for 1G) or QPLL (for 10G).Once the PLL is locked, it moves to the next state.
- WAIT SEN: The FSM waits in this state until the MUX select line value (user input) is toggled to select the 1G rate option from the previous 10G selection and vice-versa. Based on this trigger, the starting address to fetch the attribute values from the ROM is assigned.
- ADDRESS: In this state, a read from the GT registers is enabled and the attribute register address is set.
- WAIT_A_DRDY: The logic implements a read to verify the write procedure. Thus, the attribute values are initially read and then altered. This state polls for the ready signal from the GT to be asserted.
- BITMASK: The portions of bits of the attribute register which are not to be altered are masked in this state.
- BITSET: The attribute register bits are set in this state.
- WRITE: The new value of the attribute is written to the corresponding register location.
- WAIT_DRDY: This state polls for the ready signal from the GT to be asserted as an acknowledgement to a successful write.
- Register Count: In this state, the total number of the attribute registers to be changed is monitored. The FSM moves to the ADDRESS state until the register count becomes zero, indicating that all the registers are written.
- GT_RST: The GT channel is reset to apply the new attribute values written. The FSM moves to the WAIT LOCK state and subsequently remains in WAIT_SEN state until another SEN rising pulse is obtained.

Software Application

You can download the Reference Design Files for this application note from the Xilinx website.

Table 1 shows the reference design matrix.

Table 1: **Reference Design Matrix**

Parameter	Description
General	
Developer Name	Xilinx
Target Devices	KC705,VC709,ZC706
Source code provided?	Yes
Source code format (if provided)	Verilog
Design uses code or IP from existing reference design, application note, 3rd party or Vivado software? If yes, list.	1G/2.5G Ethernet PCS/PMA or SGMII (Xilinx) Tri-Mode Ethernet MAC (Xilinx) Ten Gigabit Ethernet PCS/PMA 10GBASE-R (Xilinx) Ten Gigabit Ethernet MAC (Xilinx)
Simulation	

Table 1: **Reference Design Matrix *(Cont'd)***

Parameter	Description
Functional simulation performed	Yes
Timing simulation performed?	No
Test bench provided for functional and timing simulation?	Yes
Test bench format	Verilog
Simulator software and version	Vivado Simulator 2014.4
SPICE/IBIS simulations	No
Implementation	
Synthesis software tools/versions used	Vivado synthesis
Implementation software tool(s) and version	Vivado Implementation
Static timing analysis performed?	Yes
Hardware Verification	
Hardware verified?	Yes
Platform used for verification	KC705,VC709,ZC706

Requirements

Hardware

- Xilinx 7 series FPGA board: KC705, VC709 or ZC706
- Power Supply: 100 VAC-240 VAC input, 12 VDC 5.0A output
- USB cable with standard-A plug to micro-B plug for Programming the FPGA
- Four SFP+ 10GBASE-SR/SW Transceiver Modules (Avago Technologies)
- Two LC-LC Duplex 10 Gb Multimode 50/125 OM3 Fiber Optic Patch Cable, 2 x LC Male to 2 x LC Male, part number FO-10GGBLCX20-001 (Amphenol Corporation)
- FMC Card (Part Name: FM-S14)

Software

- Vivado Design Suite 2014.4
- USB UART drivers (Silicon Laboratories CP210x VCP drivers)

Reference Design Files

Figure 4 shows the directory structure of the design files.

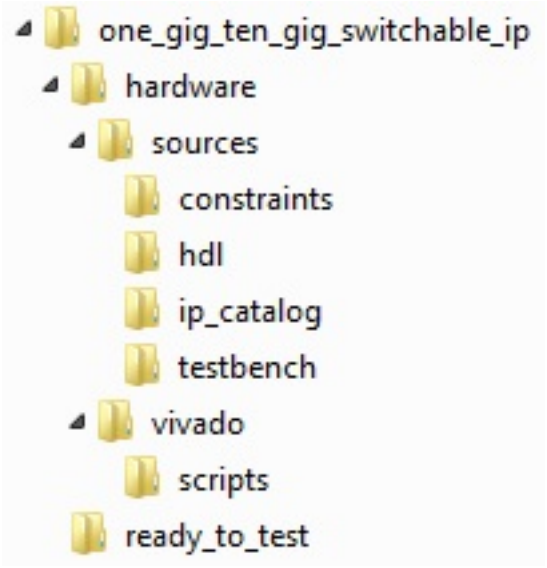

Figure 4: **File Structure**

The `one_gig_ten_gig_switchwable_ip` folder contains all the hardware design deliverables:

- The `sources/hdl` folder contains the source code deliverable files.
- The `sources/testbench` folder contains test bench files for simulation.
- The `vivado/scripts` folder contains the implementation and simulation scripts for the design for both Windows and Linux operating systems in command line and Vivado Design Suite IDE mode.
- The `sources/ip_catalog` folder contains the Xilinx IP cores required for this design.
- The `ready_to_test` folder contains programming files and scripts to configure the KC705 board.
- The `readme` file in the `one_gig_ten_gig_switchwable_ip` folder provides details on the use of simulation and implementation scripts.

Licensing

See the following product pages for details about licensing the 10 Gigabit Ethernet MAC and the 10 Gigabit Ethernet PCS/PMA cores:

- 10 Gigabit Ethernet MAC Product Page (www.xilinx.com/products/intellectual-property/do-di-10gemac.html)
- 10 Gigabit Ethernet PCS/PMA Product Page (www.xilinx.com/products/intellectual-property/10gbase-r.html)

Reference Design Steps

This section includes details about running the reference design from setup to results.

Setup

1. Connect the KC705 board to the control computer and power supply as shown in Figure 5.

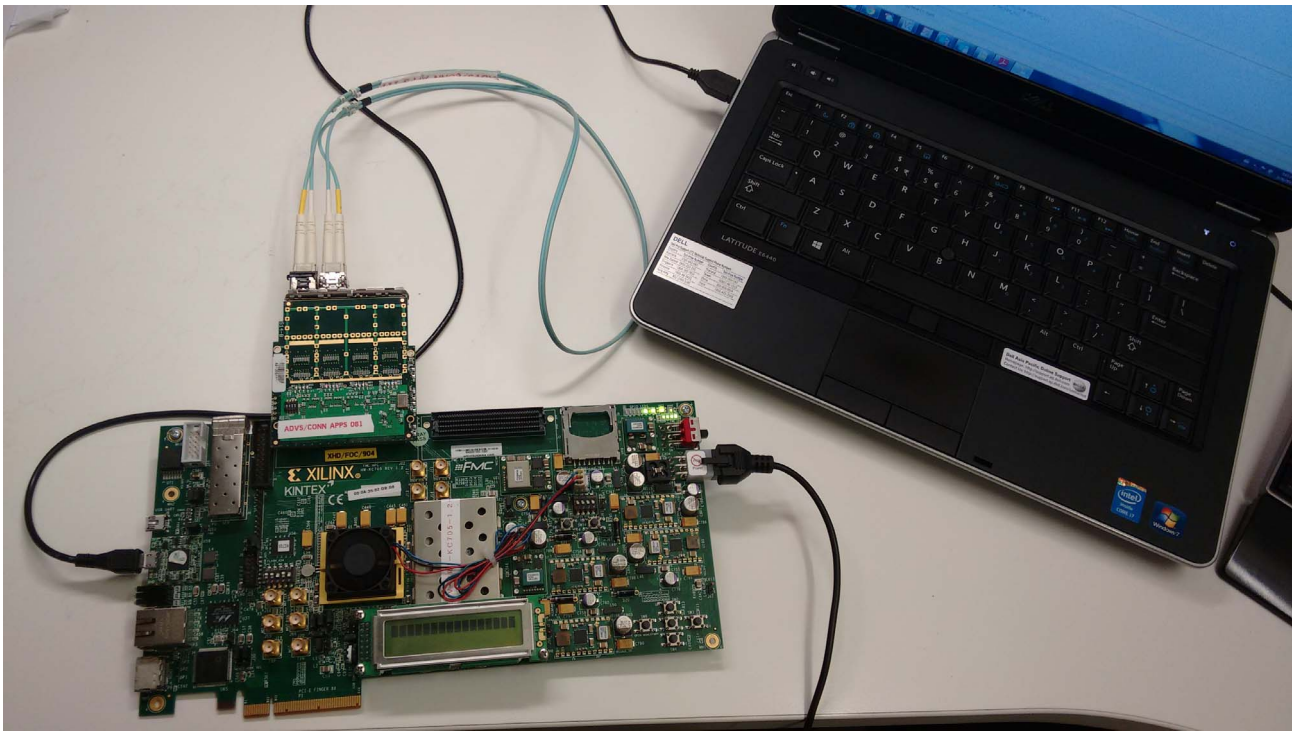

Figure 5: **Hardware Setup**

2. Insert the SFP+ modules into the SFP cage on the FMC card and connect the fiber optic cables.
3. Plug the FMC card (FM-S14) into the FMC slot (FMC HPC) of the board.
4. Ensure that switches P1 and P2 on the FMC card are in the on position as shown in Figure 6.

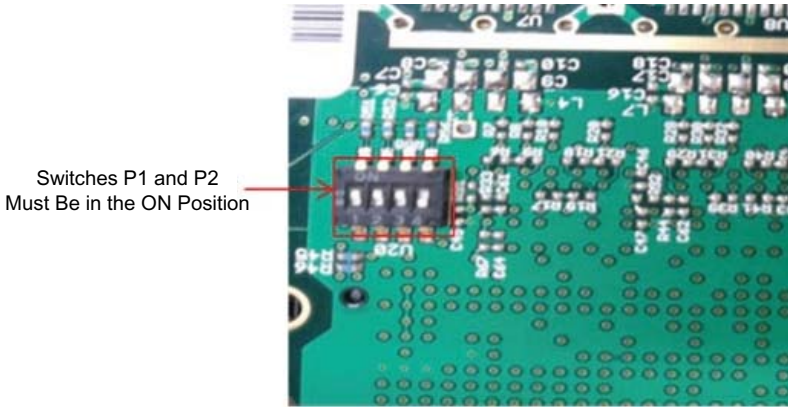

Figure 6: **FMC Card Switch Position**

Running the Reference Design

Implementing the Design

1. Launch the Vivado Integrated Design Environment (IDE) on the control computer.

   On Windows 7:

   a. Click **Start** > **All Programs** > **Xilinx Design Tools** > **Vivado 2014.4** > **Vivado 2014.4**.

   b. On the getting started page, click on Tcl Console.

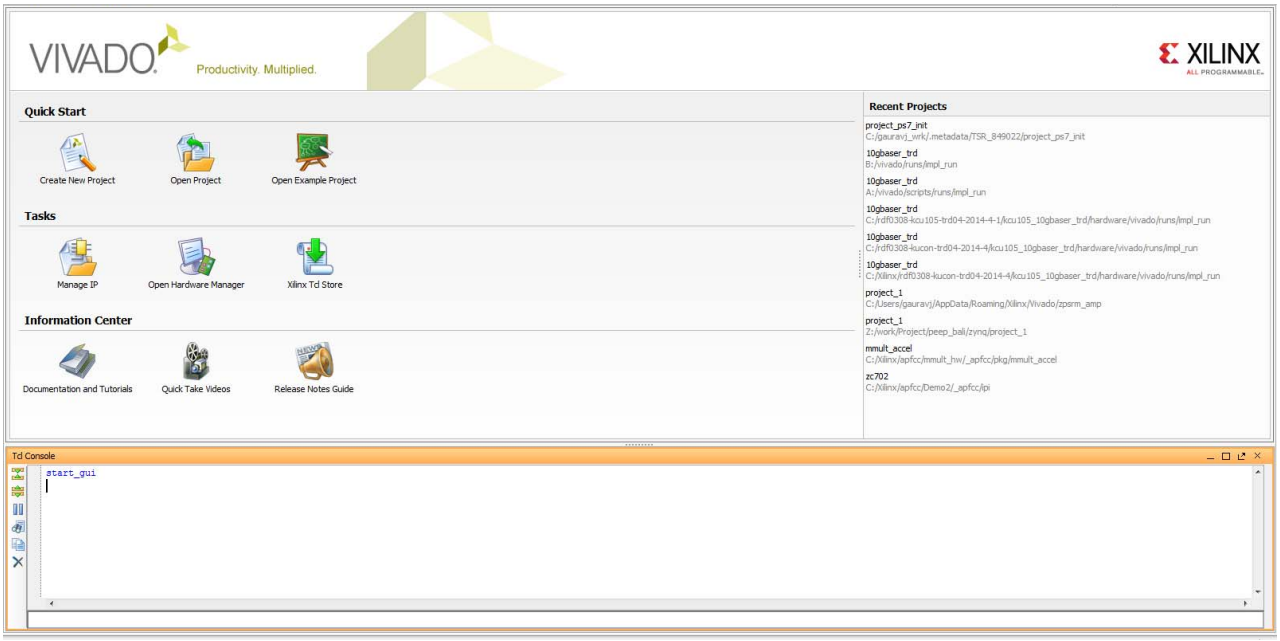

Figure 7: **Vivado IDE and Tcl Console**

   c. In the Tcl console type :

```
cd <working_dir>/one_gig_ten_gig_switchable_ip/hardware/vivado
source scripts/one_gig_ten_gig_switchable_ip.tcl
```

   On Linux:

   a. On a terminal window, change directory to `<working_dir>/one_gig_ten_gig_switchable_ip/hardware/vivado`

   b. At the command prompt enter:

```
vivado -source scripts/one_gig_ten_gig_switchable_ip.tcl
```

   c. In the Tool Flow Navigator, click **Generate Bitstream**.

Simulating the Design

Use the following instructions to run a simulation in the Vivado Design Suite Simulator.

1. In the Flow Navigator Panel under Simulation, click **Simulation Settings** (Figure 8).

2. In the Project Settings window, select the desired simulator in the Target simulator field and click **Yes**. Click **OK** in the Project Settings window. Vivado offers the Vivado Simulator as the default simulator. If there are other simulators, the compiled libraries path must be set along with the corresponding license.

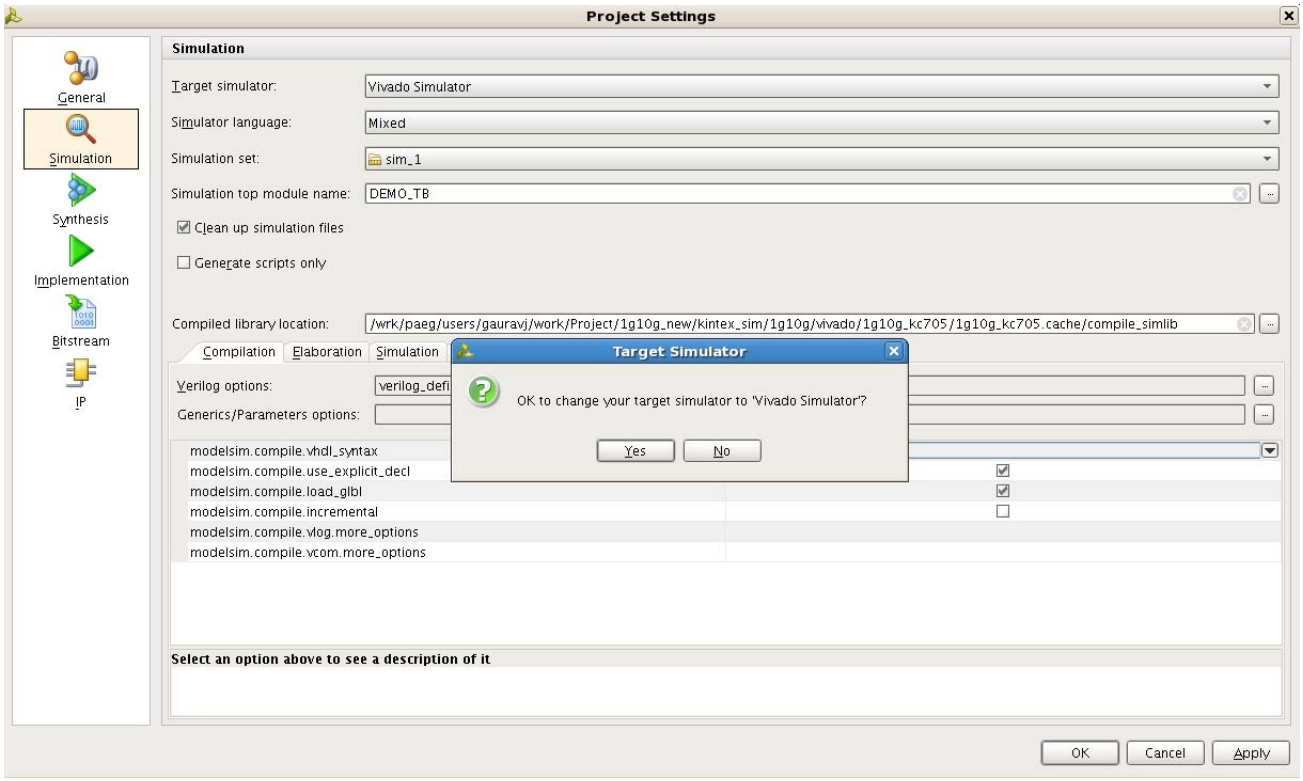

Figure 8: **Selecting the Simulator**

Programming the BIT File

1. Launch the Vivado Integrated Design Environment (IDE) on the control computer. Select **Start** > **All Programs** > **Xilinx Design Tools** > **Vivado 2014.4** > **Vivado 2014.4**.
2. On the getting started page, click **Open Hardware Manager**.
3. Open the connection wizard to initiate a connection to the KCU105 board. Click **Open Target** >**Open New Target** (see Figure 9).
4. Program the BIT file and `debug.ltx`.
5. Toggle the VIO probe to 0 for 10G and 1 for 1G.

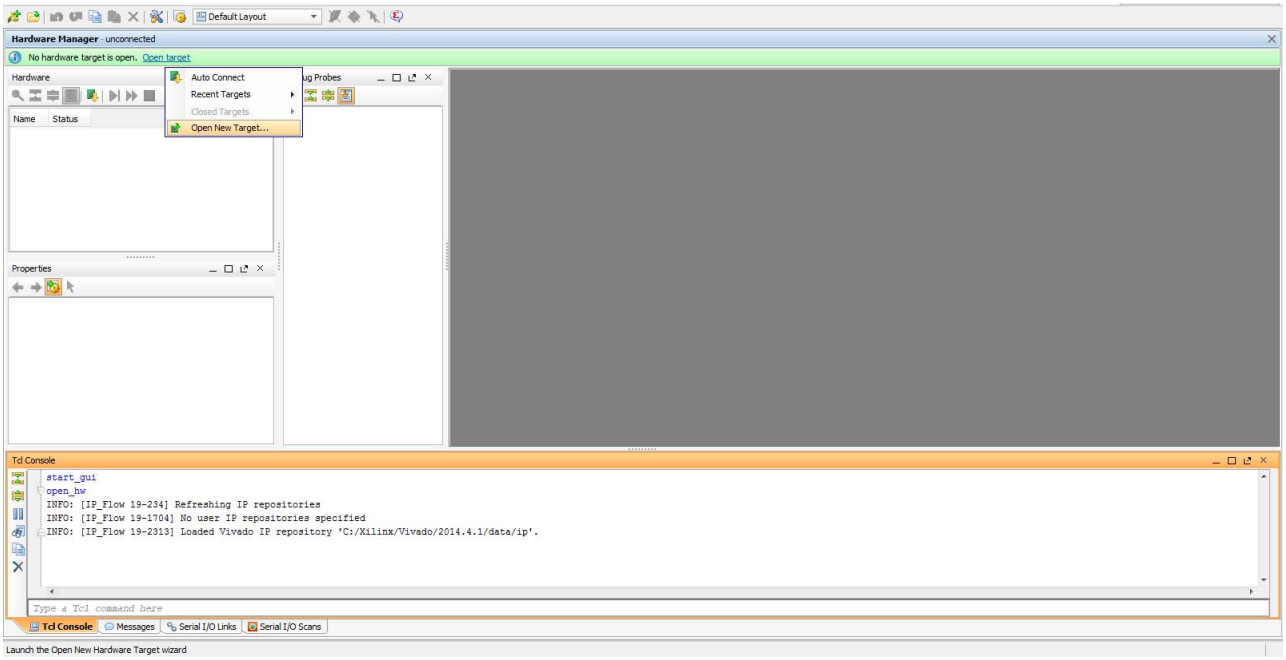

Figure 9: **Programming the BIT File**

6. Configure the wizard to establish a connection with the board by selecting the default value on each wizard page. Click **Next** > **Next** > **Next** > **Finish**.
7. In the hardware view, right-click the board name and click **Program Device**.

Integrating the Design in User Environment

1. Set the NUM_PCS_PMA_MAC_INST parameter to the desired number of channels to integrate in the top level file (`1g_10g_switchable.v`).
2. Connect Q0_CLK1_GTREFCLK_PAD_P_IN to a reference clock and change the constraints in the top level constraint file, `eth_1g10g_top.xdc`. In the provided reference design, the frequency setting is 312.5 MHz.
3. Connect the reset port in `eth_1g10g_top.xdc`.
4. Fix the location of the GTs in `eth_1g10g_top.xdc`.
5. Fix the location of sfp_tx_disable in `eth_1g10g_top.xdc`.

Results

Throughput of the reference design is listed in Table 2.

Table 2: **Throughput (Interframe Gap of 2 Clock Cycles)**

Packet Size	1 Gb/s	10 Gb/s
64	0.968	7.5
128	0.984	8.75
512	0.996	9.68

Table 2: **Throughput (Interframe Gap of 2 Clock Cycles) *(Cont'd)***

Packet Size	1 Gb/s	10 Gb/s
1024	0.998	9.843
1500	0.998	9.893

Resource utilization is shown in Table 3.

Table 3: **Resource Utilization (Implementation)**

Device	LUT	FF	BRAM
KC705	14.01%	7.78%	0%
ZC706	12.86%	6.92%	0%
VC709	6.07%	7.65%	0%

References

1. *10 Gigabit Ethernet MAC LogiCORE IP Product Guide* (PG072)
2. *10 Gigabit Ethernet PCS/PMA LogiCORE IP Product Guide* (PG068)
3. *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051)
4. *1G/2.5G Ethernet PCS/PMA or SGMII LogiCORE IP Product Guide* (PG047)
5. *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476)
6. Faster Technology, LLC: FM-S14 Quad SFP/SFP+ transceiver VITA 57 FMC Module (www.fastertechnology.com/products/fmc/fm-s14.html)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/17/2015	1.0	Initial Xilinx release.

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