



XAPP1244 (v1.0) April 10, 2015

JPEG 2000 and SMPTE 2022 Video over IP Reference Design

Author: Jean-François Marbehant and Virginie Brodeux

Summary

This application note describes the Video over IP reference design that integrates Xilinx® SMPTE 2022-1/2 and SMPTE 2022-5/6 Video over IP cores with Barco-Silex JPEG2000 IP cores on Zynq®-7000 All Programmable (AP) SoC (OmniTek OZ745 Evaluation Kit). The design supports up to four SD/HD-SDI streams.

The reference design is composed of two platforms: the transmitter platform and receiver platform. The transmitter platform design uses four SMPTE SDI IP cores to receive the incoming SDI video streams. On the uncompressed path, all received SDI streams are multiplexed and encapsulated into fixed-size datagrams by the SMPTE 2022-5/6 Video over IP Transmitter core and sent out through the Xilinx 10 Gigabit Ethernet MAC (10GEMAC). The 10G link is supported by the 10 Gigabit Ethernet PCS/PMA (10GBASE-R) using an SFP+ cable connected to the receiver end. On the compressed path, all SDI streams are compressed by the JPEG2000 encoder, encapsulated into transport stream packets by the TS Engine, packed into fixed sized datagrams by the SMPTE 2022-1/2 Video over IP Transmitter core and sent out through the 10GEMAC and 10G PCS/PMA cores. Because these paths share the same Ethernet link, both paths cannot be enabled at the same time.

On the receiver platform, the Ethernet datagrams of the uncompressed streams are collected at the 10GEMAC. The SMPTE 2022-5/6 Video over IP Receiver core filters the datagrams, de-encapsulates and de-multiplexes them into individual streams, and outputs the SDI videos through the SMPTE SDI cores. The Ethernet datagrams of the compressed streams are collected at the 10GEMAC, de-encapsulated by the SMPTE 2022-1/2 Video over IP Receiver core and by the TS Engine, and fed to the JPEG2000 decoder. Its output video is converted to SDI and sent to the SMPTE SDI cores. All the Ethernet datagrams are buffered in a DDR3 SDRAM for both the transmitter and receiver.

A Linux application running on an ARM® Cortex™-A9 processor is used to initialize the cores and read the status.

Figure 1 shows a global view of the modules involved.

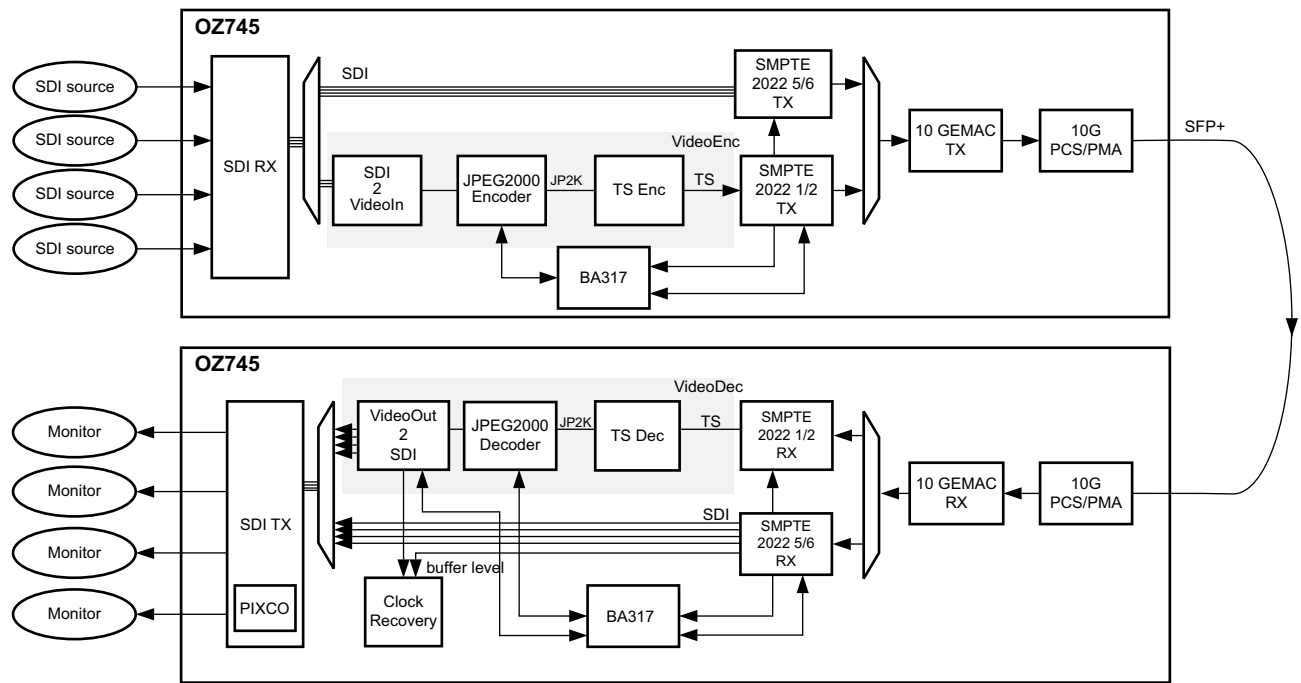


Figure 1: Video over IP Block Diagram

You can download the [Reference Design Files](#) for this application note from the Xilinx Video over IP member lounge (registration required). For detailed information about the design files, see [Reference Design Files](#).

Reference Design

The reference design implements two separate paths:

- Four SDI streams are handled by the SMPTE2022-5/6 and 10GEMAC cores as described in the *SMPTE 2022-5/6 High Bit Rate Media Transport Over IP Networks with Forward Error Correction Application Note* (XAPP1199) [Ref 11], which should be consulted for the details on the uncompressed path. This application note only addresses the differences from XAPP1199.
- Four SDI streams are routed to the compressed path where the reference design implements the SMPTE2022-1/2 IP cores and JPEG2000 IP cores as modules for broadcast applications that require bridging between broadcast connectivity standards (SD-SDI/ HD-SDI/3G-SDI) and gigabit Ethernet networks.

The compressed data to be transported are encapsulated in MPEG-2 Transport Stream (MPEG2-TS) packets. The TS packets are processed by the SMPTE2022-1/2 IP core and transported over the same SFP+ link using the 10GEMAC and 10G PCS/PMA IP cores. To support the system functions correctly, the bandwidth available in the network always meets or exceeds the bandwidth required by the stream generated by the system.

The input and output of both complete compressed and uncompressed paths are SDI video streams. The system contains two platforms with the encoder core in one platform and the decoder core in the other. An SFP+ cable connects the two platforms simulating an IP network, as shown in [Figure 2](#).

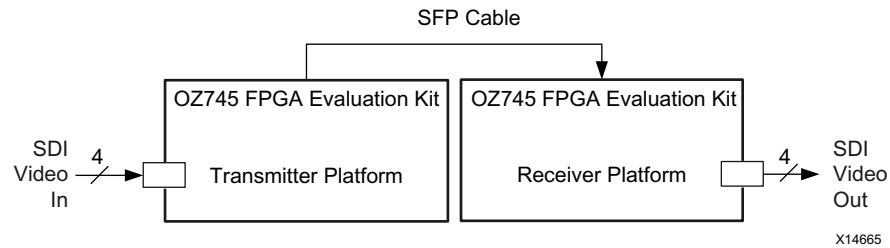


Figure 2: Complete Video over IP System

The SMPTE SDI core enables the system to receive and transmit SDI streams while the 10GEMAC transfers the compressed video data in the Ethernet medium (see [Figure 3](#) and [Figure 4](#)).

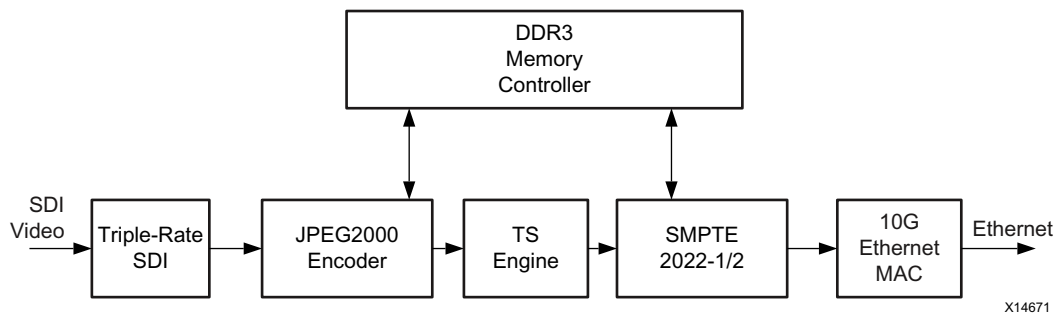


Figure 3: Transmitter Compressed Path

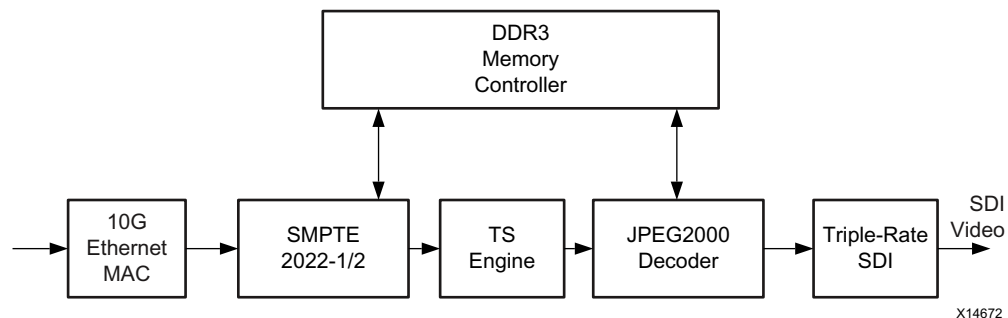


Figure 4: Receiver Compressed Path

Hardware

This section describes the high-level features of the reference design, including how the main IP blocks are configured.

SMPTE 2022-5/6 Video over IP Transmitter and Receiver

The SMPTE 2022-5/6 Video over IP Transmitter and Receiver in the reference design are configured to transport four channels of SDI input. The transmitter and receiver connect to the

10GEMAC through an AXI4-Stream data interface. They also connect to a customized IP core (axilite_bridge) in the ARM processor subsystem through an AXI4-Lite control interface.

The MAC and IP addresses, UDP ports, FEC parameters are configurable through the registers. See the SMPTE 2022-5/6 Video over IP product guides (PG032 and PG033) [Ref 5] [Ref 6].

The SMPTE 2022-5/6 Receiver uses a VCXO replacement solution for video clock recovery. See the *All Digital VCXO Replacement for Gigabit Transceiver Applications Application Note* (XAPP589) for details [Ref 13].

SMPTE SD/HD/3G-SDI

The SMPTE SDI core provides transmitter and receiver interfaces for SMPTE SD-SDI, HD-SDI and 3G-SDI standards. The core is connected to 7 series GTX transceivers to serialize and de-serialize the SDI video streams. The SMPTE SDI receiver uses a 148.5 MHz GTX transceiver reference clock frequency to receive its supported SDI bit rates. The receiver automatically determines the incoming SDI bit rate and configures itself and the GTX transceiver appropriately for that SDI mode. The SMPTE SDI transmitter requires two different GTX reference clock frequencies (148.5 MHz and 148.35 MHz) to support all SDI bit rates. The transmitter dynamically determines the operating SDI mode and controls the GTX transmitter through the dynamic reconfiguration port (DRP) to provide the appropriate configuration for each SDI mode. See the *SMPTE SD/HD/3G-SDI LogiCORE IP Product Guide* (PG071) for more information [Ref 12].

BA317 DDR3 Memory Controller

The Barco-Silex BA317 IP core is a highly configurable DDR3-SDRAM memory controller. It supports features to achieve high bandwidth efficiency even with random address accesses. The memory controller is optimized for high frequency, low latency and low resource count.

The user interface is a configurable multi-port interface supporting AXI ports for the SMPTE2022-1/2 and SMPTE2022-5/6 cores (256-bit wide interface running at 200 MHz) and DCI ports for the JPEG2000 cores (32, 64 or 128 bits wide running at different frequencies).

JPEG2000 Encoder

The JPEG2000 Encoder core from Barco-Silex compresses a video stream to the JPEG2000 format to be transferred to the gigabit Ethernet cable. Its input must be a video stream. As a result, the SDI stream coming out of the SMPTE SDI core must be converted (generation of HSync, VSync and DE video signals). Its parameters have been fixed in the VideoEnc netlist, except the bit rate which can be changed dynamically through software. It has 15 DCI ports to the memory controller and uses the fourth quarter of the memory (upper addresses). It is provided as an encrypted netlist.

JPEG2000 Decoder

The JPEG2000 Decoder core from Barco-Silex decompresses a JPEG2000 stream received from the Gigabit Ethernet cable. Its video output must be converted to SDI and sent to the SMPTE SDI core. It has 8 DCI ports to the Memory controller and uses the fourth quarter of the memory

(upper addresses). The frames coming out of the decoder are stored in DDR and read as required by the SDI bit rate constraints. Some may be dropped and some repeated if necessary. The decoder and video conversion logic are provided as encrypted netlists (VideoDec/VideoOut).

MPEG2-TS Transport Stream Engine

The Barco-Silex Transport Stream (TS) engine encapsulates and de-encapsulates a JPEG2000 stream into and out of an ISO/IEC 13818-1 compatible transport stream.

The JPEG2000 stream is converted to the AXI4-Stream format and is packetized and encapsulated in a TS stream by the TS engine before the SMPTE2022-1/2 core.

The TS engine adds an ELSM header to the JPEG2000 picture stream and a PES header to obtain a packetized elementary stream (PES). It fragments the PES into Transport Stream packets of 188 bytes. The engine generates additional information for the Transport Stream: PAT/PMT for stream information and PCR for clock recovery.

The TS engine follows the VSF technical recommendation in VSF-TR01, Transport of JPEG 2000 Broadcast Profile video in MPEG-2 TS over IP [\[Ref 14\]](#).

SMPTE2022-1/2 Video over IP Transmitter and Receiver

The SMPTE 2022-1/2 Video over IP Transmitter and Receiver in the reference design are configured to transport four channels of transport streams.

The transmitter and receiver connect to the 10GEMAC through an AXI4-Stream data interface. They also connect to a customized IP core (axilite_bridge) in the ARM processor subsystem through an AXI4-Lite control interface.

The MAC and IP addresses, UDP ports, and FEC parameters are configurable through the registers. See the SMPTE 2022-1/2 Video over IP product guides (PG180 and PG181) [\[Ref 2\]](#) [\[Ref 3\]](#).

10-Gigabit Ethernet MAC

The AXI4-Stream interface of the transmitter 10-Gigabit Ethernet MAC instance is connected to the output of either the SMPTE 2022-1/2 or the SMPTE 2022-5/6 Video over IP transmitters. The AXI4-Stream interface of the receiver 10-Gigabit Ethernet MAC instance is connected to the input of the SMPTE 2022-1/2 and the SMPTE 2022-5/2 Video over IP receivers. A 64-bit SDR PHY port is configured in the 10-Gigabit Ethernet MAC to interface to the 10-Gigabit Ethernet PCS/PMA core. No flow control is used. See the *10-Gigabit Ethernet MAC LogiCORE IP Product Guide* (PG072) for more information [\[Ref 15\]](#).

10-Gigabit Ethernet PCS/PMA

The 10-Gigabit Ethernet PCS/PMA core creates a 10GBASE-R optical link between the video over IP transmitter and receiver platforms. The PCS/PMA uses one transceiver to achieve a 10 Gb/s data rate. An optical cable is connected between the SFP+ optical transceivers on both

platforms. See the *10-Gigabit Ethernet PCS/PMA LogiCORE IP Product Guide* (PG068) for more information [Ref 15].

Resource Utilization

The reference design is implemented with a Zynq-7045 AP SoC (XC7Z045-1-FFG900) using the Vivado® Design Suite: System Edition 2014.2. The resources used for the Video over IP Transmit and Receive platforms are shown in Table 1.



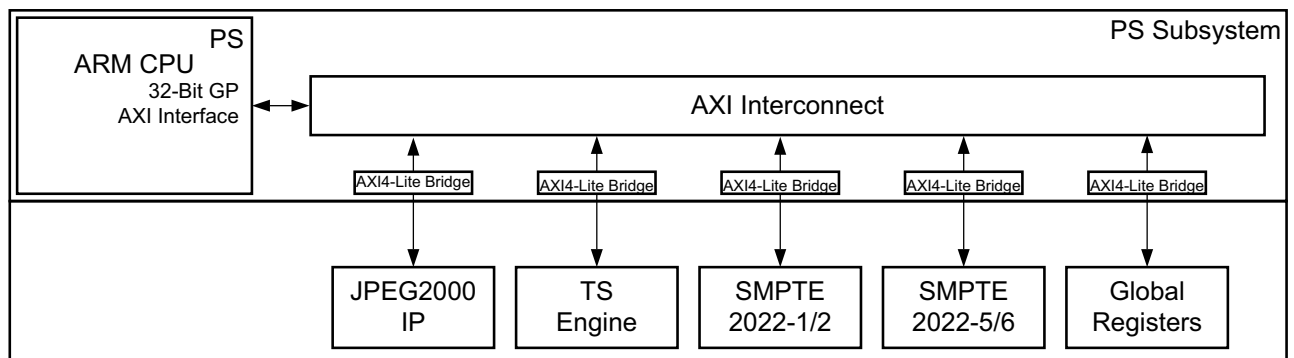
IMPORTANT: Device resource utilization results depend on the implementation tool versions. Exact results can vary. These numbers should be used as a guideline.

Table 1: Resource Utilization

Platform	LUTs	I/Os	RAMB36	RAMB18
TX	128501 out of 218600 (59%)	122 out of 362 (34%)	264 out of 545 (48%)	115 out of 1090 (10%)
RX	135470 out of 218600 (62%)	122 out of 362 (34%)	382 out of 545 (70%)	119 out of 1090 (11%)

Software Application

The ARM processor subsystem implements overall system control. A Linux application is run to configure all the IP cores (SMPTE 2022-1/2 and SMPTE 2022-5/6 cores, JPEG2000 encoder and decoder and Transport Stream engines) and to read the status and debug information. Several AXI4-Lite bridges have been added to access the device modules. Figure 5 shows a block diagram of the ARM processor subsystem.



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Figure 5: ARM Processor Subsystem

Table 2 shows the memory address map of the processor subsystem.

Table 2: Processor Subsystem Memory Address Map

Peripheral	Base Address	High Address
SMPTE 2022-5/6	0x70000000	0x7000FFFF
SMPTE 2022-1/2	0x70100000	0x7010FFFF
TS Engine	0x70200000	0x7020FFFF

Table 2: Processor Subsystem Memory Address Map (Cont'd)

Peripheral	Base Address	High Address
JPEG2000 Encoder	0x70300000	0x7030FFFF
System	0x70400000	0x7040FFFF

Tool Flow and Verification

Table 3 shows the reference design matrix.

Table 3: Reference Design Checklist

Parameter	Description
General	
Developer names	Jean-François Marbehan and Virginie Brodeux
Target devices (stepping level, ES, production, speed grades)	Zynq®-7000 SoC (XC7Z045-1-FFG900)
Source code available	Netlists are provided for the BA317 memory controller, the JPEG2000 encoder and decoder, the TS Engine and Xilinx LogiCORE IPs. The rest is provided as source code.
Source code format	VHDL and Verilog
Design uses code/IP from existing Xilinx application note/reference designs, Vivado IP Catalog, or third party	Cores generated from Vivado Design Suite
CORE Generator software	Vivado IP Catalog
Simulation	
Functional simulation performed	N/A
Timing simulation performed	N/A
Test bench used for functional and timing simulations	N/A
Test bench format	N/A
Simulator software/version used	N/A
SPICE/IBIS simulations	N/A
Implementation	
Synthesis software tools/version used	For the JPEG2000 cores: SynplifyPro 2014.03 All other cores: Vivado Design Suite 2014.2
Implementation software tools/versions used	Vivado Design Suite: System Edition 2014.2
Static timing analysis performed	Yes
Hardware Verification	
Hardware verified	Yes
Hardware platform used for verification	OZ745 Zynq-7000 AP SoC Evaluation Kit

Requirements

This section details any requirements for running the reference design.

Hardware

The hardware requirements for the reference design are:

- Two Omnitek OZ745 Zynq-7000 All Programmable SoC Video Development Kits
- Eight SDI 75Ω BNC cables
- Two UART USB cables
- One SFP+ cable
- SDI Sink and Source with support for up to 4 inputs and outputs

Software

The reference design is created and built using the Vivado Design Suite: System Edition, version 2014.2. Part of the design is created using the Xilinx Platform Studio (XPS) tool. The design also includes software built using the Xilinx Software Development Kit (SDK). The software runs on the ARM processor subsystem and implements control and status functions.

Reference Design Files

You can download the [Reference Design Files](#) for this application note from the Xilinx Video over IP member lounge (registration required).

The reference design includes the following cores:

- Xilinx AXI4-Stream Interconnect (www.xilinx.com/products/intellectual-property/axi4-stream_interconnect.html)
- Barco-Silex DDR3 Memory Controller (BA317) [Ref 8]
- Xilinx SMPTE2022-1/2 Transmitter and Receiver (www.xilinx.com/products/intellectual-property/ef-di-smpte2022-12.htm)
- Xilinx SMPTE2022-5/6 Transmitter and Receiver (www.xilinx.com/products/intellectual-property/ef-di-smpte2022-56.htm)
- Barco-Silex JPEG2000 Encoder (BA110) and Decoder (BA109) [Ref 7]
- Barco-Silex TS Engine
- Xilinx SMPTE SDI (www.xilinx.com/products/intellectual-property/smpte_sdi.html)
- Xilinx 10 Gigabit Ethernet MAC (www.xilinx.com/products/intellectual-property/do-di-10gemac.html)
- Xilinx 10 Gigabit PCS/PMA (www.xilinx.com/products/intellectual-property/10gbase-r.html)

Licensing

Each Xilinx and Barco-Silex core must be licensed. See the product pages listed in [Reference Design Files](#) for details about how to license each core.

Reference Design Steps

This section includes any details about running the reference design from setup to results.

Setup

This reference design runs on the OZ745 Video Development Kit. [Figure 6](#) shows the overall setup.

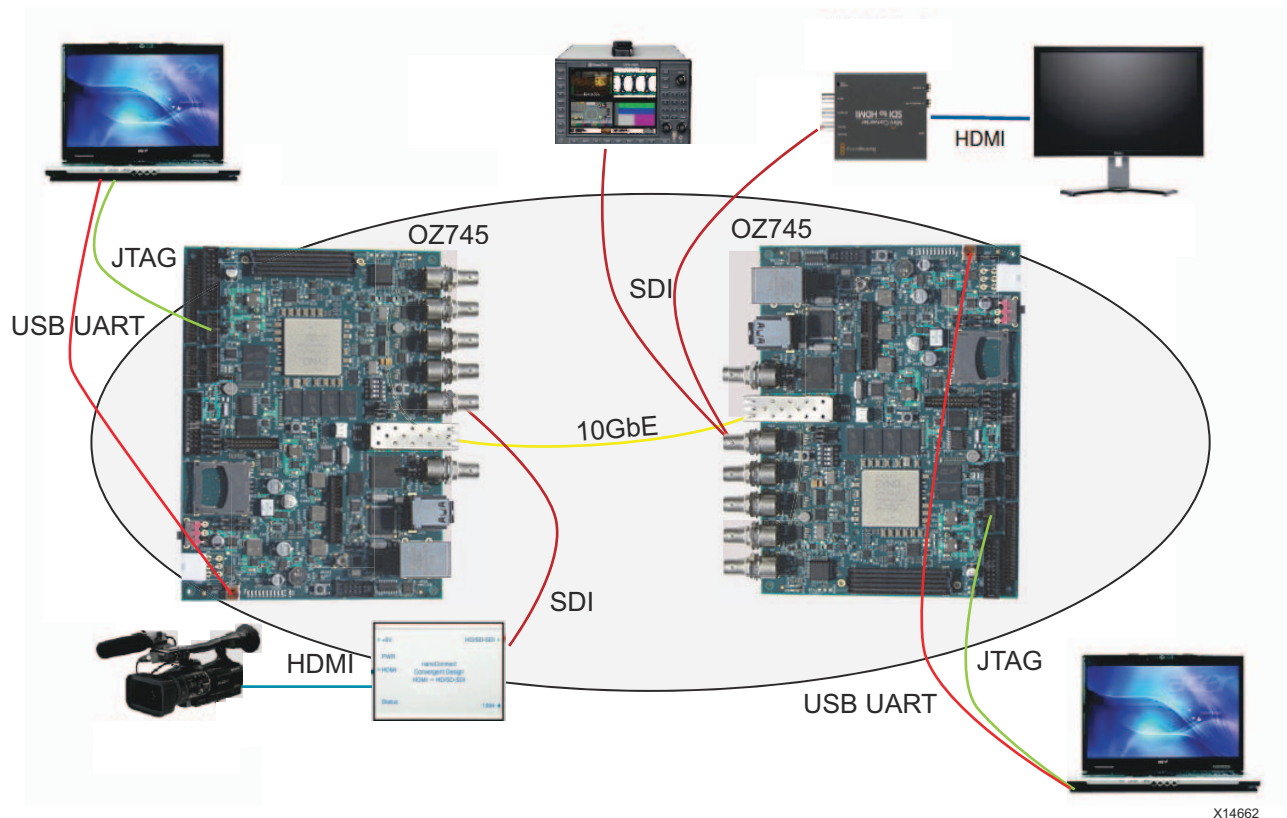
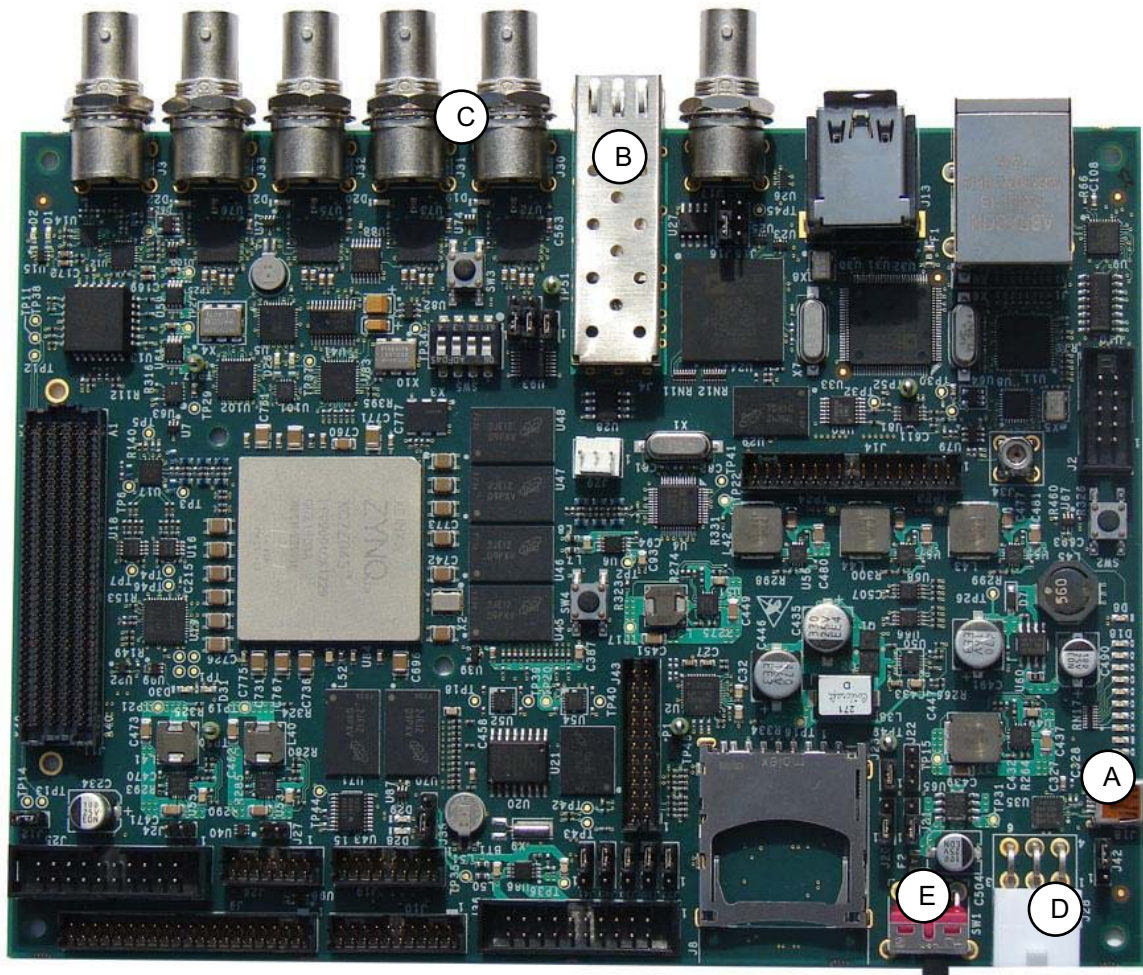


Figure 6: Video over IP Setup

Running the Reference Design

The following instructions for running the design include steps that correlate to the lettered labels in [Figure 7](#).



X14664

Figure 7: OZ745 Video Development Board

1. Copy the BIT file (device bitstream), the shell script and ELF file present in the `ready_for_download` directory of the TX and RX reference designs to the SD card of the transmitter board and receiver board, respectively. Files should be copied into the `videoip` directory at the root of the SD card.
2. Connect a USB cable from the host PC to the USB UART port (A) on the TX board. Ensure that the Silicon Labs CP210x USB to UART Bridge Device Driver has been installed [Ref 17].
3. Connect one end of the SFP+ cable (B) to the Video over IP transmitter board, and the other end to Video over IP receiver board.
4. If the OZ745 board is the Video over IP receiver, connect the SDI ports 1 to 4 (C) to the SDI video monitor (using an SDI to HDMI converter if needed).
5. If the OZ745 board is the Video over IP transmitter, connect the SDI ports 1 to 4 (C) to the SDI video generator.
6. Connect the power supply to the OZ745 board (D).
7. Switch on the OZ745 board (E).
8. From the Device Manager in Windows (search for `devmgmt.msc` in the **Start** menu and run it), identify the COM port to which the USB to UART bridge is connected, as shown in

Figure 8.

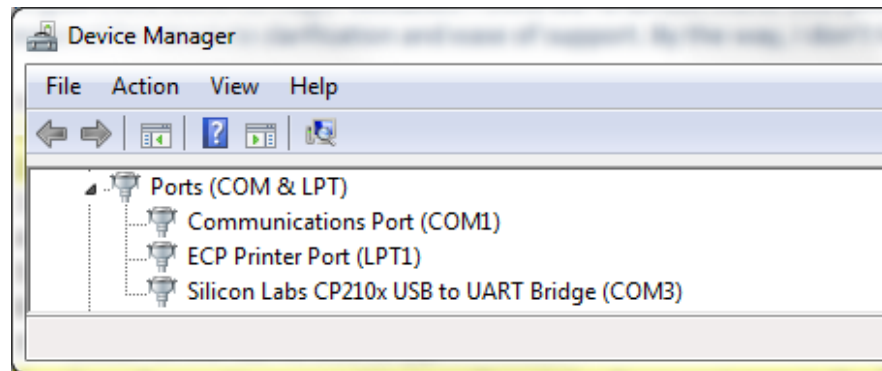


Figure 8: Device Manager

9. Start a terminal program (for example, TeraTerm or PuTTY) on the host PC on the determined UART COM port, as shown in Figure 9.

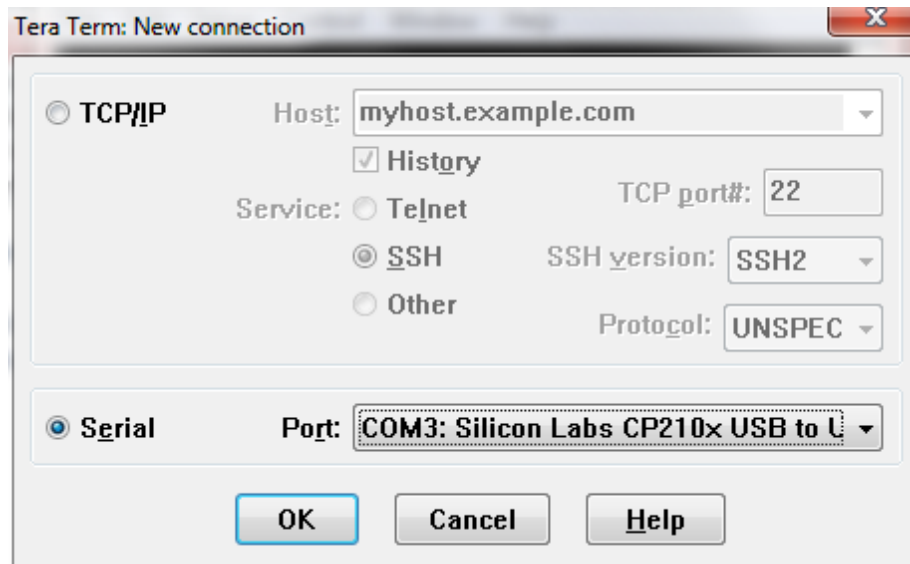


Figure 9: New Serial Connection

10. In the Serial Port Setup, use the following settings:
 - **Baud Rate:** 115200
 - **Data Bits:** 8
 - **Parity:** None
 - **Stop Bits:** 1
 - **Flow Control:** None
11. In the terminal window (Figure 8), locate the `/mnt/videoip` directory and source the shell script:

```
source videoip_tx.sh
```

12. Program the device with the help of the `zynqProgramBitstream` utility present on the OZ745 SD card:

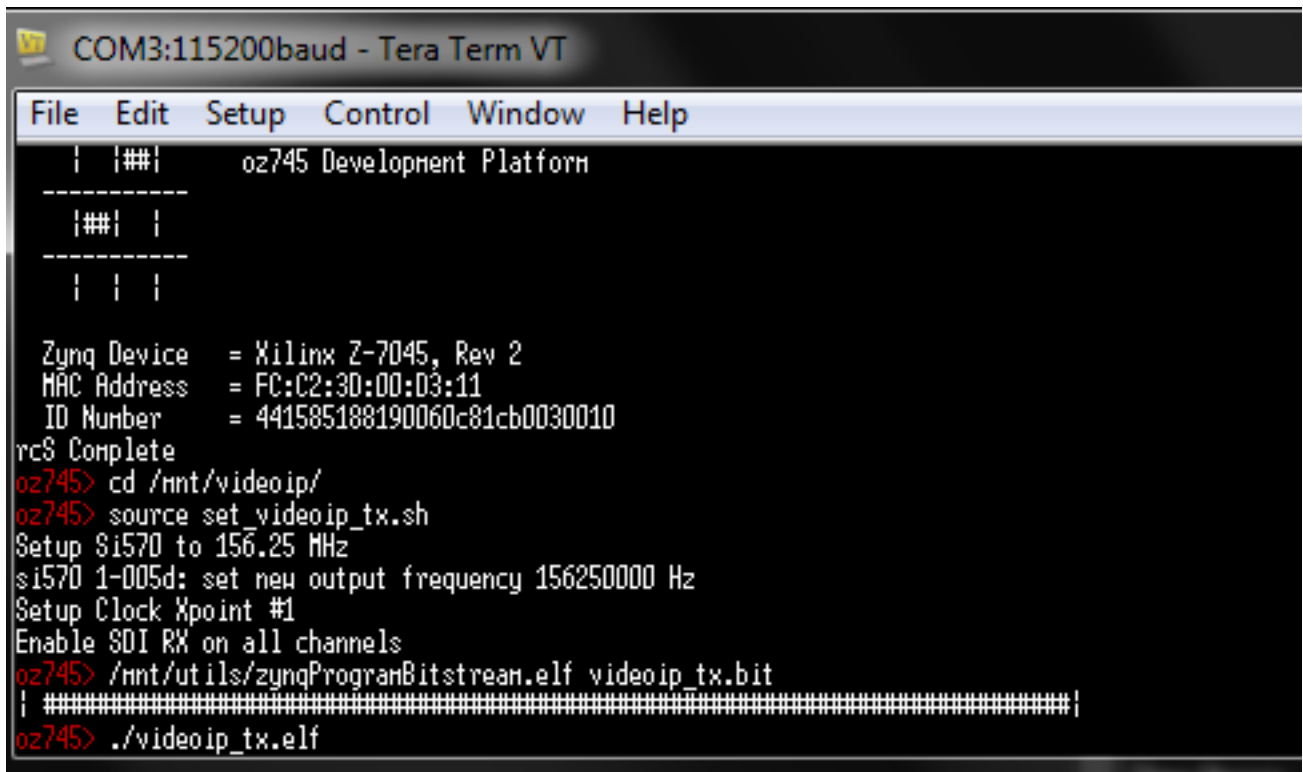
```
/mnt/utils/zynqProgramBitstream videoip_tx.bit
```

13. Run the configuration software:

```
./videoip_tx
```

14. Remove the USB UART cable from the TX board and connect the cable to the RX board.

15. Start again from [step 8](#) with the `videoip_rx.sh`, `videoip_rx.elf` and `videoip_rx.bit` files.



```
COM3:115200baud - Tera Term VT
File Edit Setup Control Window Help
| |##| oz745 Development Platform
-----
|##| |
-----
| | |

Zynq Device = Xilinx Z-7045, Rev 2
MAC Address = FC:C2:30:00:D3:11
ID Number = 441585188190060c81cb0030010
rcS Complete
oz745> cd /mnt/videoip/
oz745> source set videoip_tx.sh
Setup Si570 to 156.25 MHz
si570 1-005d: set new output frequency 156250000 Hz
Setup Clock Xpoint #1
Enable SDI RX on all channels
oz745> /mnt/utils/zynqProgramBitstream.elf videoip_tx.bit
| #####|
oz745> ./videoip_tx.elf
```

Figure 10: Terminal Window

Results

The software interface is identical to that presented in the *SMPTE 2022-1/2 CBR MPEG2 Over IP with Forward Error Correction Application Note* (XAPP1194) [\[Ref 10\]](#) and the *SMPTE 2022-5/6 High Bit Rate Media Transport Over IP Networks with Forward Error Correction Application Note* (XAPP1199) [\[Ref 11\]](#), with additional options to configure the JPEG2000 encoder rate interactively. [Figure 8](#) shows the Video over IP TX software output display.

```

-----
VoIP TX Main Menu
-----

0 = Enable uncompressed path
--
Options SMPTE2022-1/2
 1 = Reset Core
 2 = Initialize Core
 3 = Configure Channel
 4 = Probe Current Settings
--
Options SMPTE2022-5/6
 5 = Reset Core
 6 = Initialize Core
 7 = Configure Channel
--
Options J2K Encoder
 8 = Configure Quantization
 9 = Configure Channel
--
Options TS Encoder
 t = Probe TS settings/status
--
r = Read/Write Registers
e = Control SOI inputs
? = Help
-----
>e

Select Channel
1 = Enable channel 1 (disabled)
2 = Enable channel 2 (disabled)
3 = Enable channel 3 (disabled)
4 = Enable channel 4 (disabled)
e = Enable all channels
d = Disable all channels
n = Main Menu
-----
>1

Select Channel
1 = Disable channel 1 (enabled)
2 = Enable channel 2 (disabled)
3 = Enable channel 3 (disabled)
4 = Enable channel 4 (disabled)
e = Enable all channels
d = Disable all channels
n = Main Menu
-----
>2

Select Channel
1 = Disable channel 1 (enabled)
2 = Disable channel 2 (enabled)
3 = Enable channel 3 (disabled)
4 = Enable channel 4 (disabled)
e = Enable all channels
d = Disable all channels
n = Main Menu
-----

```

Figure 11: VoIP TX Main Menu

The menu options displayed allow the user to:

- Enable (or disable) the uncompressed path.

- Configure or probe the settings/status of SMPTE2022-1/2.
- Configure or probe the settings/status of SMPTE2022-5/6.
- Configure the JPEG2000 encoder.
- Probe the TS engine settings/status.
- Access all registers.
- Control the SDI inputs.
- Change the rate of the JPEG2000 encoder, which has a direct influence on the quality of the displayed image at the SDI output of the receiver: the lower the rate value, the lower the quality of the output.

```
>9
Select Channel
1 = Channel 1
2 = Channel 2
3 = Channel 3
4 = Channel 4

n = Main Menu
-----
>1
Select rate: bytes per compressed frame (bit rate @ 60fps)
0 = 5 kB (2.5 Mbps)
1 = 20 kB (10 Mbps)
2 = 50 kB (25 Mbps)
3 = 100 kB (50 Mbps)
4 = 200 kB (100 Mbps)
5 = 300 kB (150 Mbps)
6 = 400 kB (200 Mbps)
n = Main Menu
-----
>4
Changed JPEG2000 rate of channel 1 to 200000

Select Channel
1 = Channel 1
2 = Channel 2
3 = Channel 3
4 = Channel 4

n = Main Menu
-----
>
```

Figure 12: VoIP TX Change JPEG2000 Rate

Choose one of the seven proposed rates or go back to the main menu. The fourth value 100 kB (equivalent to 50 Mbps at 60 fps) is the default one.

Rebuilding Hardware

This section details the steps to rebuild the hardware design.



IMPORTANT: Before rebuilding the project, ensure that the licenses for the SMPTE 2022-1/2 and SMPTE 2022-5/6 Video over IP Transmitter and Receiver cores and the 10GEMAC and PCS/PMA cores are installed.

To generate the programming file:

1. Change to the implementation directory of the reference design.
2. To create, compile and generate the project bitstream, run the `buildfpga.sh` script.

References

1. SMPTE2022-1/2 Video over IP Core Product Page (www.xilinx.com/products/intellectual-property/ef-di-smpte2022-12.html)
2. SMPTE 2022-1/2 Video over IP Transmitter LogiCORE IP Product Guide ([PG180](#))
3. SMPTE 2022-1/2 Video over IP Receiver LogiCORE IP Product Guide ([PG181](#))
4. SMPTE2022-5/6 Video over IP Core Product Page (www.xilinx.com/products/intellectual-property/ef-di-smpte2022-56.html)
5. SMPTE 2022-5/6 Video over IP Receiver LogiCORE IP Product Guide ([PG033](#))
6. SMPTE 2022-5/6 Video over IP Transmitter LogiCORE IP Product Guide ([PG032](#))
7. Barco-Silex JPEG2000 Cores (www.barco-silex.com/ip-cores/jpeg-2000)
8. Barco-Silex BA317 DDR Controller (www.barco-silex.com/ip-cores/BA317)
9. OmniTek OZ745 Zynq®-7000 AP SoC Video Development Kit (www.xilinx.com/products/boards-and-kits/1-2UHUFU.htm)
10. SMPTE 2022-1/2 CBR MPEG2 Over IP with Forward Error Correction Application Note ([XAPP1194](#))
11. SMPTE 2022-5/6 High Bit Rate Media Transport Over IP Networks with Forward Error Correction Application Note ([XAPP1199](#))
12. SMPTE SD/HD/3G-SDI LogiCORE IP Product Guide ([PG071](#))
13. All Digital VCXO Replacement for Gigabit Transceiver Applications Application Note ([XAPP589](#))
14. VSF-TR01, Transport of JPEG 2000 Broadcast Profile Video in MPEG-2 TS over IP (www.videoservicesforum.org/activity_groups/VSF_TR-01_2013-04-15.pdf)
15. 10-Gigabit Ethernet MAC LogiCORE IP Product Guide ([PG072](#))
16. 10-Gigabit Ethernet PCS/PMA LogiCORE IP Product Guide ([PG068](#))

17. Silicon Labs CP210x USB to UART Bridge Device Driver
www.silabs.com/products/mcu/pages/usbtouartbridgevcpcdrivers.aspx

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/10/2015	1.0	Initial Xilinx release.

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