Virtex-E LVPECL Receivers in Multi-Drop Applications

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Summary

This application note describes how to use differential LVPECL (low-voltage positive emitter-coupled logic) signaling for high-performance multi-drop applications with Virtex-E FPGAs. Multi-drop LVPECL allows a single LVPECL driver to connect directly to multiple LVPECL receivers on a single transmission line. SPICE simulations verify multi-drop operation from DC up to 311 Mbits/s, with ten loads. This application note includes DC specifications, and an Appendix with microstrip and layout guidelines. The LVPECL receivers on the Virtex-E FPGA eliminate costly LVPECL-TTL translators, reducing board area and skew.

Introduction

Differential LVPECL offers higher noise immunity than single-ended techniques due to the differential swing of the dual signals. Multi-drop LVPECL allows many LVPECL receivers to be driven by a single industry standard LVPECL driver. By providing a direct connection, the fully differential LVPECL inputs of the Virtex-E FPGA are ideal for preserving low-jitter clocks. They also eliminate costly LVPECL-TTL translators, decrease signal timing skew, and reduce the board area required to develop high-performance applications.

Multi-Drop LVPECL Circuits

Figure 1 shows a typical multi-drop LVPECL application. The Q and $\overline{Q}$ outputs of the LVPECL driver on the left connect serially to the inputs of the Virtex-E LVPECL receivers along the length of the multi-drop lines. A resistor R_T differentially terminates the Q and $\overline{Q}$ signals in parallel at the end of the multi-drop lines. Simple microstrip lines made on standard PC boards with ground planes suffice for this application.

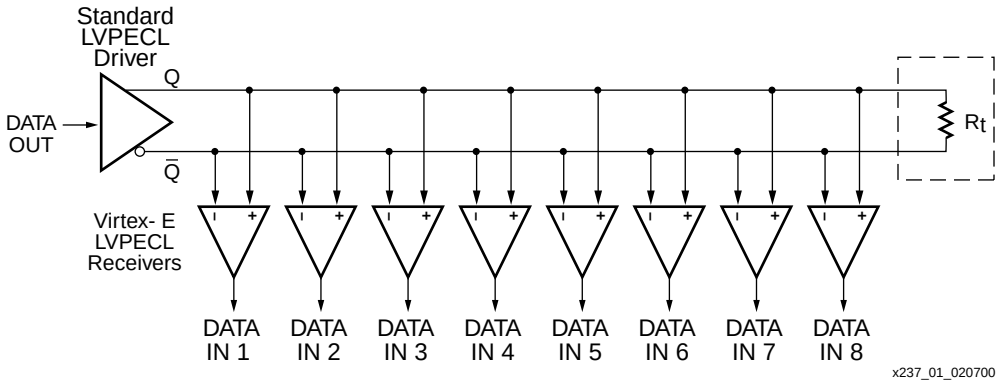

Figure 1: **Typical Multi-Drop LVPECL Application**

Microstrip Transmission Lines for Multi-Drop LVPECL

Microstrip is a PCB (printed-circuit board) trace on the top or bottom layer of the PCB over a ground or power plane on the next inner layer. Figure 2 shows the cross-section of a microstrip transmission line. The trace width (w), trace height above ground plane (h), trace thickness (t), and the relative dielectric constant (εr) of the PCB determine the microstrip characteristic impedance (Z_0). Table 1 summarizes the characteristic impedance of the microstrip in Figure 2 for typical values of w and h on an FR4 PCB using one ounce copper.

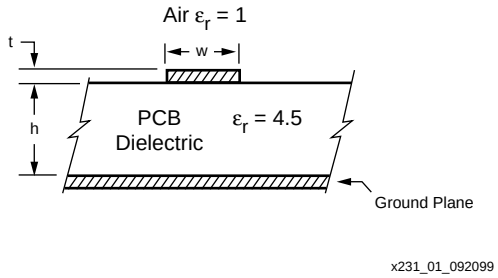

Figure 2: **Microstrip Transmission Line Cross-Section**

Table 1: **Microstrip Impedance for Typical Values of w and h**

Trace Width (w) Mils	Height Above Plane (h) Mils	Impedance (Z_0) Ohms
4	5	70
6	5	59
8	5	51
16	10	52

Trace widths and heights above the plane are rounded to the nearest mil for ease of layout and fabrication. Note the microstrip transmission line impedance is approximately constant with the w/h ratio. A w/h ratio of four, gives approximately Z_0 = 29 to 30 ohms. A w/h ratio of 1.6, gives approximately Z_0 = 51 to 52 ohms. Using the w/h ratio approximation, the characteristic impedance of a microstrip with any plane spacing can be estimated.

Multi-Drop LVPECL DC Specifications

LVPECL outputs typically drive a ± 750 mV voltage swing (Q - $\overline{Q}$), and the average of Q and $\overline{Q}$, (Q + $\overline{Q}$) /2, is sometimes referred to as the common-mode voltage, or V_{BB}. Typical LVPECL output V_{BB} is 2.0 V for a 3.3V V_{CC} and tracks V_{CC} linearly. A 100 mV change in V_{CC} causes a 100 mV change in V_{BB}. Table 2 summarizes the DC output specifications of LVPECL.

Virtex-E LVPECL differential receivers have a wide common-mode input range and are completely compatible with the Motorola 100E and 100EL Series DC LVPECL voltage levels shown in Table 2.

Table 2: **Standard LVPECL DC Output Specifications**

LVPECL Voltages Under Various V_{CC} Values		MIN	TYP	MAX	Units
LVPECL Output HIGH V_{OH} Relative to V_{CC}	Motorola 100E	V_{CC} - 1.025	V_{CC} - 0.955	V_{CC} - 0.880	V
LVPECL Output V_{BB} Relative to V_{CC}		V_{CC} - 1.418	V_{CC} - 1.330	V_{CC} - 1.25	V
LVPECL Output LOW V_{OL} Relative to V_{CC}		V_{CC} - 1.810	V_{CC} - 1.705	V_{CC} - 1.620	V

Table 2: **Standard LVPECL DC Output Specifications**

LVPECL Voltages Under Various V_{CC} Values		MIN	TYP	MAX	Units
LVPECL Output HIGH V_{OH} for V_{CC} = 3.3V ± 10%	Motorola 100EL	1.975	2.345	2.720	V
LVPECL Output V_{BB} for V_{CC} = 3.3V ± 10%		1.582	1.970	2.350	V
LVPECL Output LOW V_{OL} for V_{CC} = 3.3V ±10%		1.190	1.595	1.980	V

Notes:

1. Motorola 100E and 100EL Series DC LVPECL output levels and threshold voltage, 0 - 85 °C, over the full range of V_{CC}. V_{CC} is assumed to be the 3.3V supply and varies ±10% from 3.0V to 3.6V. LVPECL levels are referenced to the higher-voltage rail and track V_{CC} linearly.
   Threshold voltage = V_{BB} = (V_{OH} + V_{OL}) / 2

Receiving Multi-Drop LVPECL on Virtex-E Devices From Industry Standard LVPECL Drivers

Figure 3 shows the reference design schematic of an industry standard differential LVPECL driver in a multi-drop connection to 10 Virtex-E or other LVPECL receivers. The LVPECL signal is driven from the industry standard LVPECL driver on the left, and is daisy-chained with two 50 Ω transmission lines and stubs to all 10 LVPECL receivers at the IN[1:10] and IN[1:10]X nodes. Each LVPECL receiver taps off the main multi-drop lines every 2.5 inches for a multi-drop line length of 25 inches. Each stub can be up to one inch long with a 50 Ω transmission line impedance to ground, or a differential impedance of 100 Ω between the two stubs. A 66 Ω termination resistor R_T (rounded to the nearest standard 1% value of 66.5 Ω) is placed across the LVPECL_TERM and $\overline{\text{LVPECL\_TERM}}$ nodes close to the final LVPECL receiver, on the right. The two 84.5 Ω (standard 1% value) resistors R_{PULL} provide pull-down current for the emitter-follower outputs of the LVPECL driver. The design calls for a 66 Ω termination impedance because the added load of the LVPECL receivers brings the 50 Ω line down to an effective impedance of 33 Ω on average. The 66 Ω termination differentially terminates each line with 33 Ω.

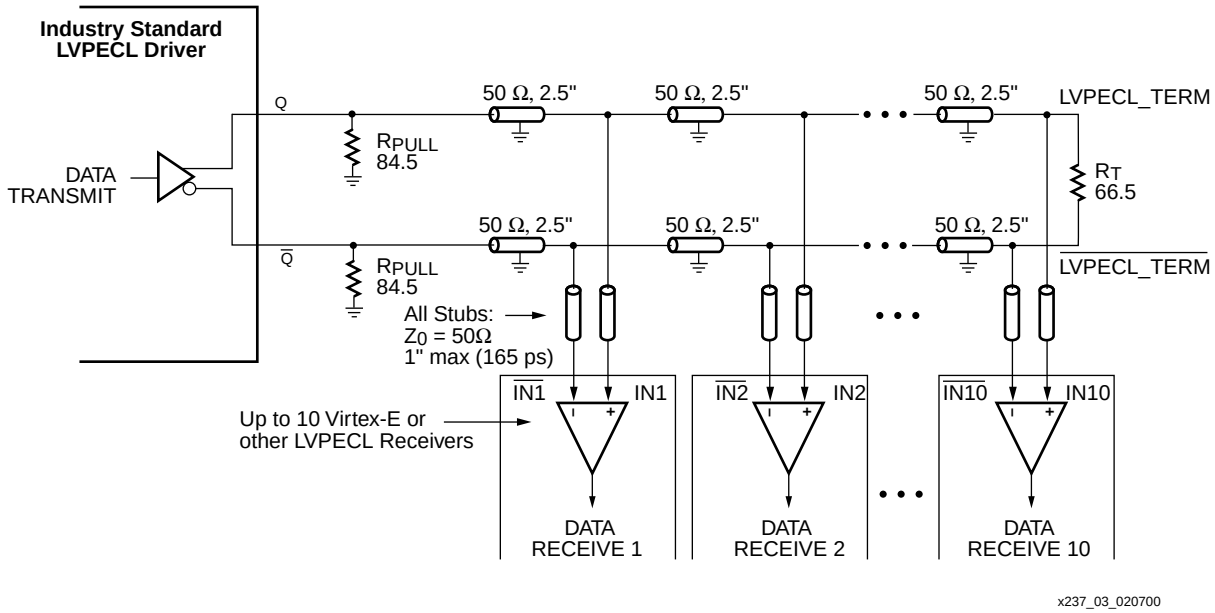

Figure 3: **Virtex-E LVPECL Multi-drop Schematic**

Why are 50 Ω transmission lines terminated with 66.5 Ω? The answer lies in the behavior of transmission lines. When capacitive receivers and stubs load down a transmission line, the extra capacitance reduces the effective impedance. The receivers in Figure 3 have an effective load capacitance of roughly 9 pF, including receiver capacitance, trace and stub capacitance. A 9 pF capacitor placed every 2.5 inches on a 50 Ω line brings the line down to 33 Ω. Therefore, the reflections are minimized if the line is terminated into 33 Ω. A differential termination must be twice this impedance or 66 Ω. Note that if the stub locations are altered significantly, the characteristic impedance will change and the optimal termination resistor changes accordingly.

For further information on effective transmission line impedance, see Howard W. Johnson, "High-speed digital design: a handbook of black magic," 1993, pp. 172-174. The section on equally-spaced capacitive loads provides the following equations.

The characteristic unloaded impedance of a transmission line is given by:

$$Z_0 = \sqrt{\frac{L}{C}}$$

Where L this the inductance per unit length, C is the capacitance per unit length, N is the number of loads, and C_L is the capacitance of each load. If H is the total length of the transmission line and the loads are evenly spaced, then the effective line impedance is:

$$Z_0(\text{effective}) = \sqrt{\frac{L}{C + \frac{NC_L}{H}}}$$

Although the termination of the transmission lines in Figure 3 uses a lower impedance than the typical 100 Ω, the industry standard LVPECL driver is designed to drive a higher current for applications, such as multi-drop, where a lower impedance termination is required to achieve good signal integrity. The total length of the multi-drop line is limited to 25 inches by skin-effect losses in the PCB microstrip trace, assuming an 8-mil wide trace over a 5 mil dielectric. Losses can be reduced by using a wider trace and larger dielectric spacing to the plane, such as 16 mils wide by 10 mils spacing to the plane, giving the same 50 Ω line impedance.

Figure 4 on page 6 shows the typical step response of the multi-drop LVPECL reference design schematic in Figure 3. All simulations were done with SPICE using package parasitics of drivers and receivers and LVPECL drivers from Motorola's application note 1560: Low Voltage ECLinPS SPICE Modeling Kit at: **http://mot-sps.com/lit/html/an1560.html**

The top graph shows the single-ended waveforms at output stubs 1, 5, and 10, corresponding to receivers at the beginning, middle, and end of the multi-drop line. The bottom graph shows the differential voltage at the same three receivers. All voltages are measured at the on-die differential input of the receiver. All received waveforms show similar characteristics with little undershoot or overshoot and negligible load reflections. Figure 5 on page 7 shows typical 311 Mbit/s burst data response of Virtex-E multi-drop LVPECL outputs for the schematic in Figure 3. Single-ended and differential waveforms are shown for outputs 1, 5, and 10 along the multi-drop line. All received waveforms show similar characteristics with little or no undershoot/ overshoot and negligible reflections. Some smoothing of the waveform occurs over the length of the multi-drop line loaded by the receivers, but the attenuation is minor. Even the last receiver sees about 800 mV peak differential signal at the end of the 25 inch line after the nine other receivers.

The Virtex-E multi-drop LVPECL receiver is fully compatible with LVPECL drivers from Motorola, Micrel, and other companies.

Conclusion

Virtex-E LVPECL receivers can acquire multi-drop LVPECL signals at a rate of up to 311 Mb/s in the -7 speed grade. These receivers provide significant improvement in system performance and clock distribution networks by receiving LVPECL signals directly onto the Virtex-E device. Reliable data and clock transmission is possible for up to 10 LVPECL receivers over electrical lengths of 4 ns (25 inches), limited only by skin effect losses on the PCB trace. Virtex-E

LVPECL receivers eliminate costly and jitter-prone LVPECL-TTL converters, decrease board area, and reduce signal delay skew, while reliably receiving high-speed data and clocks over long distances from industry-standard LVPECL drivers.

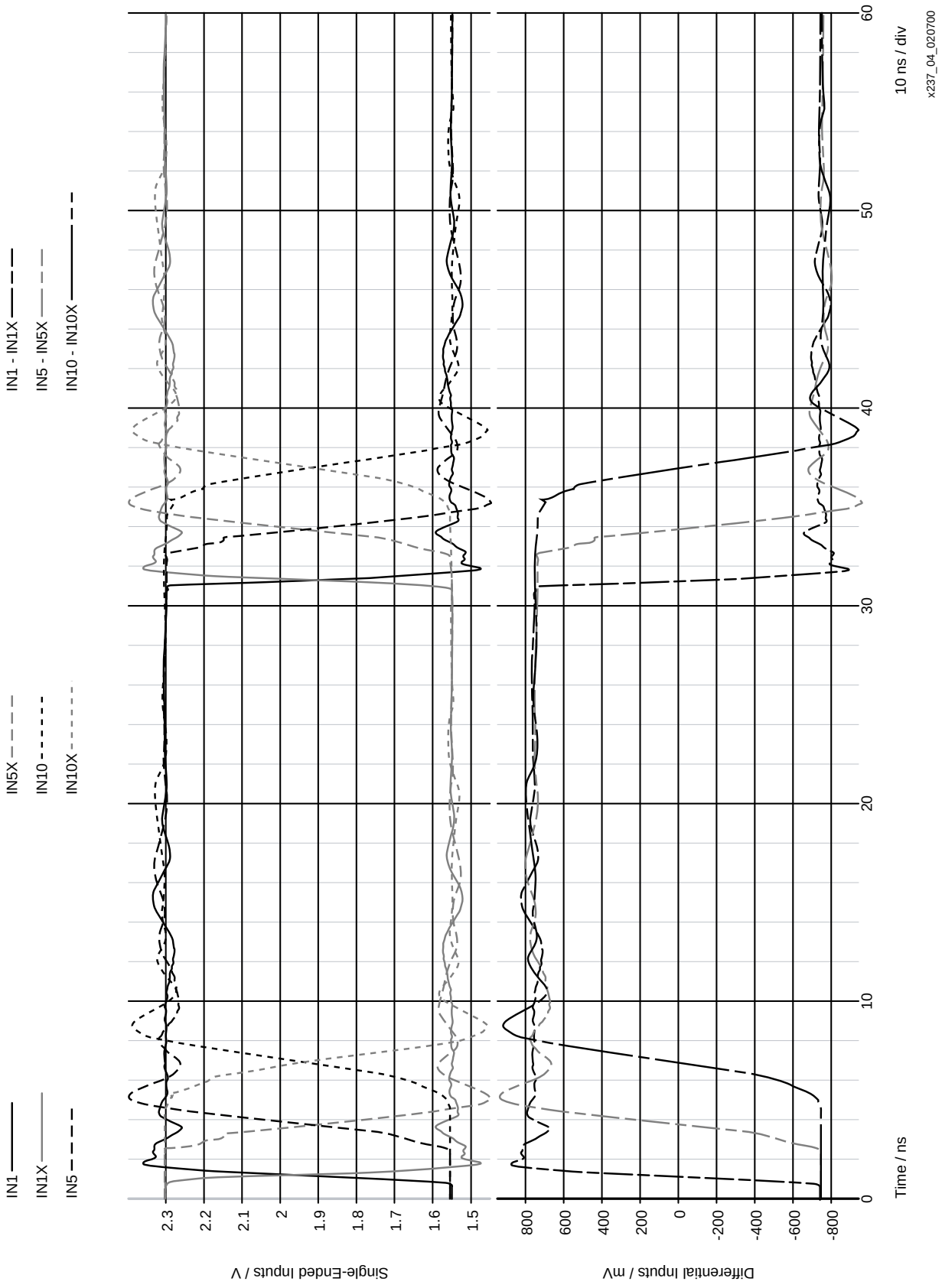

Figure 4: **Typical step response of the Multi-Drop LVPECL Reference Design.**

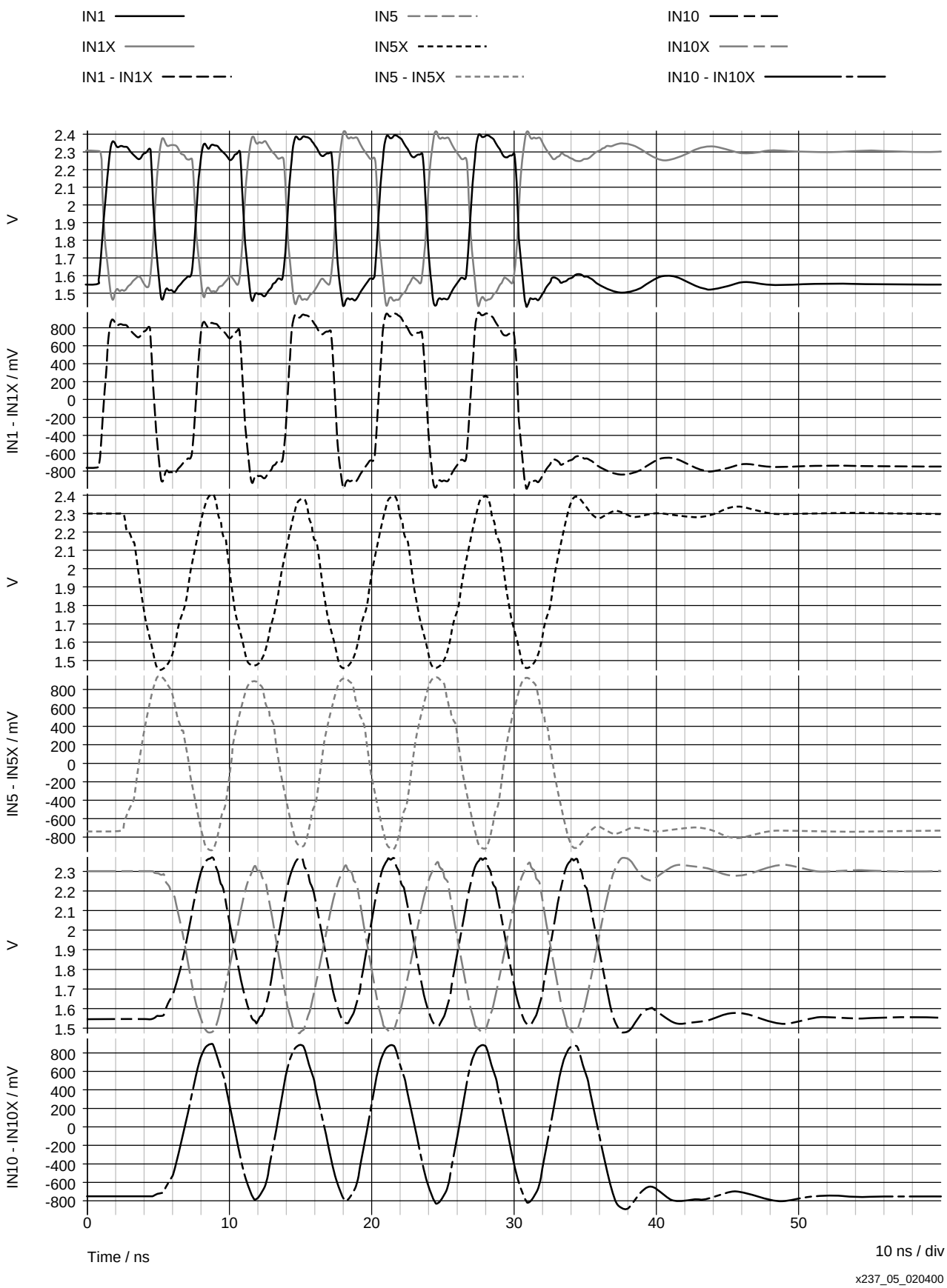

Figure 5: **Typical 311 Mb/s Burst Data Response of Virtex-E Multi-Drop LVPECL Outputs.**

Appendix A

PCB Layout Guidelines for Virtex-E Multi-drop LVPECL Receivers

Printed-circuit board layout guidelines for the Virtex-E multi-drop LVPECL circuit in Figure 3 are as follows:

A multi-layer printed-circuit board with controlled transmission line impedances is required.

1. A multi-layer printed-circuit board with controlled transmission line impedances is required.
2. The recommended transmission line structure for PCB layout is microstrip on the outer layer over ground plane on the next inner layer.
3. All transmission lines between LVPECL drivers and Virtex-E LVPECL receivers should be referenced to a common ground plane between the Virtex/TTL section of the board and the LVPECL section of the board, except when routed through a balanced differential transmission line such as twisted-pair. For twisted-pair and other balanced lines, utilize a grounded shield that connects to the ground planes at the beginning and ending of the twisted-pair cable to allow for common-mode return current. If no shield connection is available, take extra care to use symmetric and equal-length routing and ensure capacitive load balancing on the differential pair to prevent excessive common-mode to differential mode conversion. Do not split the ground plane under the signal path between the Virtex/TTL section of the board and the LVPECL section of the board as this will cause large impedance discontinuities from increased inductance.
4. Place the parallel termination resistor R_T close to the final LVPECL inputs at the far end of the multi-drop line.
5. To maximize common-mode rejection, use symmetric and equal-length routing for the multi-drop LVPECL signal pair. Route the two LVPECL signals with minimal spacing between the traces along the multi-drop line and the stubs. If the trace spacing is less than the dielectric thickness to the ground plane, differential impedance effects must be included to determine the effective transmission line impedance since the trace impedance will be significantly affected by the differential impedance between the two traces. Wider spacing has a smaller effect on the impedance.
6. The V_{CC} plane for the LVPECL section and the V_{CC} plane for the Virtex/TTL section should be separate planes on different layers or split planes on the same layer of the PCB. Since TTL generates much more noise than LVPECL and LVPECL is referenced to V_{CC}, it is necessary to split these planes using separate ferrite beads for isolation and separate bulk capacitors to minimize TTL V_{CC} noise coupling to sensitive LVPECL chips.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
2/18/00	1.0	Initial Xilinx release.
2/24/00	1.1	Edited formula for Z_0effective on page 4.