XPLA3 I/O Cell Characteristics

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Summary

This paper describes the features and benefits of the I/O cells provided by Xilinx CoolRunner® XPLA CPLDs.

Introduction

The I/O cell architecture used in XPLA3 CPLDs is intended to give designers maximum control and flexibility when implementing their designs. Each I/O cell can be implemented in one of several different modes such as a high impedance input, input with weak pull-up, output, bidirectional, or unused pin without the need for external termination. The specific I/O cell function implemented is supervised by a set of internally generated control signals.

XPLA3 I/O cells have several other beneficial features such as PCI compatibility, ability to sink and source up to 8 mA, "hot plugging" capability, half latch, and 5.0V tolerance. Additionally, the XPLA3 I/O cells have a slew rate control option for each macrocell which can be used to reduce reflections and electromagnetic interference (EMI).

A brief overview of the XPLA3 architecture as it pertains to macrocell configuration will be described in the following sections. The XPLA3 architecture will not be fully described in this application note. For more details on the XPLA3 architecture, please refer to white paper WP105, "CoolRunner XPLA3 CPLD Architecture Overview."

CoolRunner XPLA3 Architecture

As shown in Figure 1, the XPLA3 architecture consists of logic blocks containing macrocells interconnected by a routing matrix. The routing matrix is called the ZIA (Zero-power

Interconnect Array) and provides 36 true and complement signals to each logic block. Each XPLA3 logic block contains 16 macrocells.

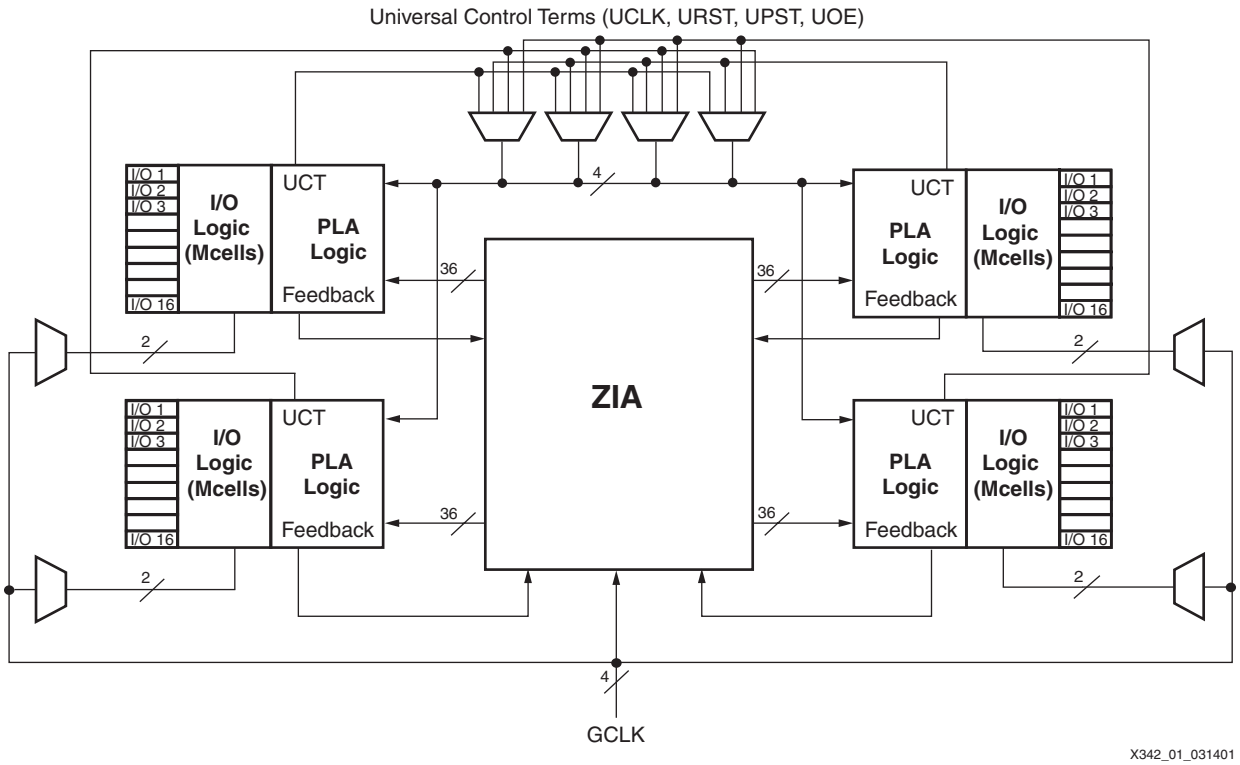

Figure 1: **XPLA3 High-level Architecture (64 macrocell device shown)**

Each logic block contains a pure PLA array (programmable AND, programmable OR). The PLA array provides a pool of 48 product terms that can be used for any of the 16 macrocells in the logic block. These product terms have several possible functions other than input logic to the macrocell. These other functions include macrocell clocks, foldback NANDs, or controls terms used as resets, presets, clock enables, or output enables. The first eight product terms in the PLA are used to generate the eight Local Control Terms (LCT0:7). Note that if these product terms are not needed as control terms, they are available for other logic within the logic block. Local Control Term 7 is routed from the logic block to the Universal Control Term multiplexers. The Universal Control Terms are then available to all the logic blocks in the XPLA3 device.

As seen in Figure 2, the I/O cell consists of a control multiplexer (mux), adjustable slew rate control, a weak pull-up resistor, and the I/O pin with a feedback connection to the ZIA. A description of each component and its function will be covered in the remaining sections.

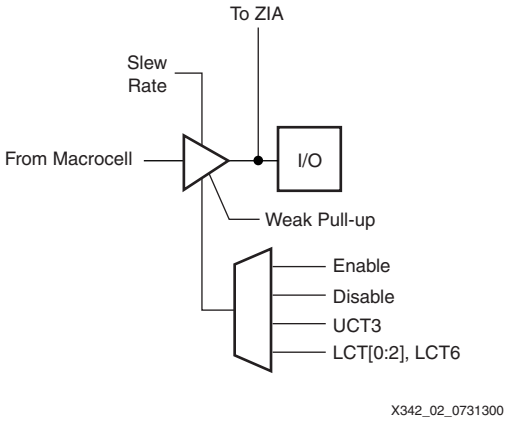

Figure 2: **Input/Output Cell Architecture**

Overview of I/O Functions

The control mux has eight inputs that can be used to select the function of the I/O cell. Within each logic block, each I/O cell is uniquely configurable with one of the eight functions listed in Table 1. In other words, using any one of the eight I/O functions, each macrocell I/O could be configured differently from the next.

Table 1: **XPLA3 Output Enable Selection**

OE Decode	I/O Pin State
0	Disable (High-Z)
1	Function LCT0
2	Function LCT1
3	Function LCT2
4	Function LCT6
5	Universal OE (UCT3)
6	Enable
7	Disable (High-Z with Weak Pull-up)

The first state of the control mux, OE0, disables the output buffer and places it in the high impedance state with no internal weak pull-up. This is used when the I/O cell is to be used as input pin or if there are external pull-ups or pull-downs on an unused I/O pin. By disabling the output buffer, the macrocell can be used as an internal node and there will not be any signal conflicts between the output of the macrocell and any external signals present on the corresponding pin. When an output goes to a high-impedance state, it disconnects the output of the I/O from the component(s) to which it is connected on the circuit board. For this state to be selected, the control mux is connected to zero. Note that this selection is automatically set by the fitter software when an I/O cell disabled in the high impedance state with no internal weak pull-up.

The next five states of the control mux, OE[1:5], are used as active High output enables and are controlled by either Local Control Terms (LCT[0:2] and LCT6) or the Universal Output Enable Control Term. These states allow the designer to place the output pin in a 3-state condition as needed. For example, consider multiple devices that are connected to a bidirectional data bus. Only one device is allowed to drive the bus at a time. Therefore, while one device is driving data

on the bus, the remaining devices must be in a high-impedance state so as not to cause any conflicts. By using an output enable control term in the output cell, potential errors associated with bus contention can be avoided.

The next output state for the control mux, OE6 or the enabled output, is used when the I/O cell is an output without the use of any output enable control terms. For this option to be selected, the control mux is connected to V_{CC}. As with the disabled output, this function is automatically set by the fitter software.

The final state of the control mux, OE7, is the disable with weak pull-up selection. This option is used when the I/O cell is not used by the design. If the pin is left unterminated, the voltage on the I/O pin can "float" or fluctuate. In total CMOS devices like XPLA3, a voltage fluctuation will cause the device to draw more current than actually required. This is due to the nature of CMOS circuits which only draw current when the voltage is changing or in the linear region. When the voltage is a logic High or Low, no current flows through the circuit and therefore consumes no power. By connecting the pin to a weak pull-up resistor, the voltage on the unused pin will be pulled up to a logic High state. The typical values for the weak pull-up in UMC material is nonlinear and can range from 69k to 114k Ohms, for a 3.3V, 25C environment. Worse case pull-up resistance values for UMC material range from 62k to 150k Ohms which varies dependent upon temperature, current, and voltage through the I/O cell. These resistors are automatically activated by fitter software for all unused pins. Buried macrocells that do not have the I/O pin used for input also have the weak pull-up resistor automatically activated. As a result of the weak pull-up resistor, it is recommended that any unused I/O pins remain unconnected. Note that dedicated inputs such as global clocks do not have a pull-up resistor and therefore should be properly terminated (pulled High or Low) if left unused.

Slew Rate

With most circuits, a fast signal rise time is desirable. However, with some circuits, the fast signal rise time can cause reflections and/or EMI in the circuit, which can affect the circuit's performance. EMI is caused by the rapid change in current as the signal transitions between states. Signal overshoot and undershoot are also a side effect of this rapid change in current. Overshoot and undershoot, described in Figure 3, and EMI can be minimized by increasing the time it takes for a signal transition to occur. The slew rate control in XPLA3 devices is a feature that allows the designer to slow down the time it takes for a signal transition to occur as seen in Figure 4. Enabling the slew rate option adds a nominal delay of 2.0 ns when the signal is applied to a typical load and has been shown to dramatically reduce reflections and EMI.

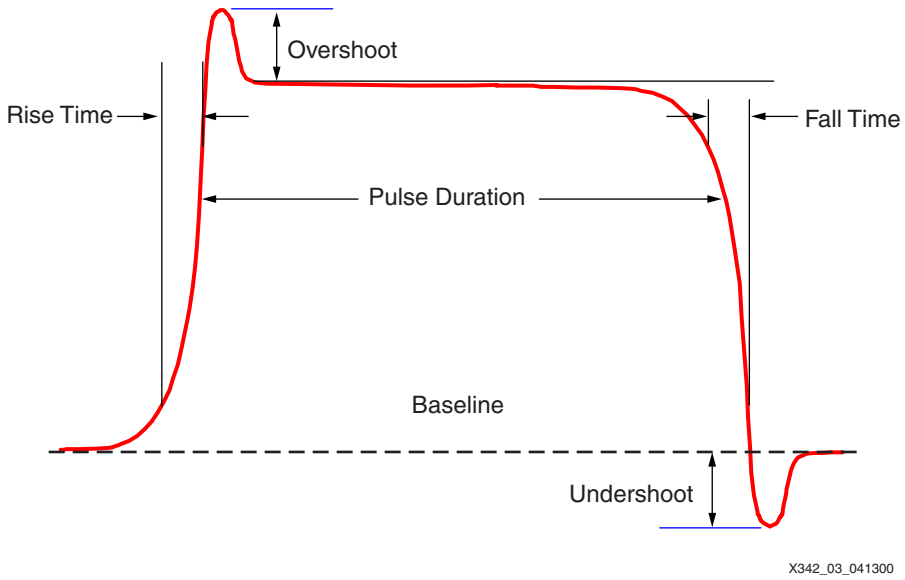

Figure 3: **Discrete Signal Characterization**

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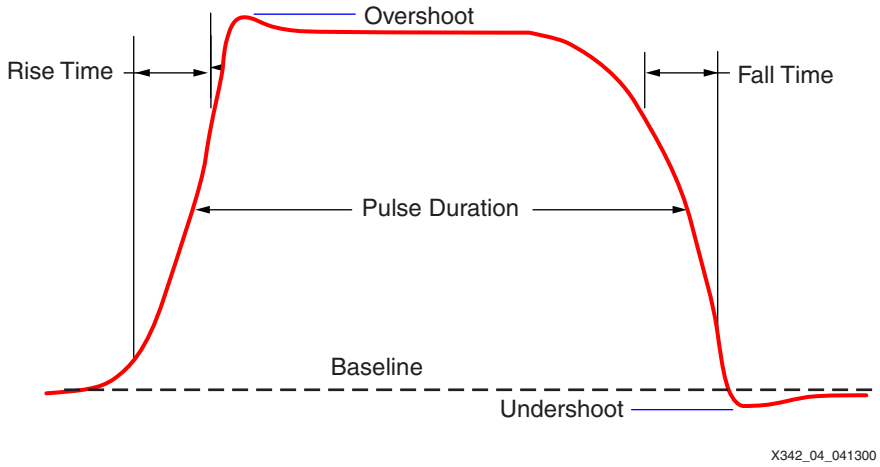

Figure 4: **Discrete Signal with Slew Added**

PCI Compatibility

One of the benefits of XPLA3 devices is the fact that they are PCI compatible. All I/O cells on XPLA3 devices are 5V tolerant and provide timing, voltage and current characteristics required by the PCI specification. XPLA3 devices are not compliant because the PCI specification requires overshoot and undershoot signal conditioning diodes, which are not provided (neither the upper nor the lower clamp diodes are available in the XPLA3 I/O cell). If a designer wishes to implement a PCI driver/receiver, the designer will be required to provide external diode clamps. The diode clamps can be implemented using either a standard diode or a Schottky diode. Schottky diodes are the diode of choice due to their lower threshold voltage. With the exception of the clamp diodes, XPLA3 devices meet the stringent requirements of the PCI specification.

Half Latch

XPLA3 devices provide internal pull-up resistors, which can be turned on or off with Xilinx ISE™ software. ISE enables pull-up resistors by default. It is always good practice to terminate XPLA3 CMOS inputs to V_{CCIO}--doing so will reduce current consumption and will prevent the

input buffers from oscillating. These internal pull-up resistors help ensure that the input is held High, even if the user does not drive the I/O pin.

Some designs may require that the internal pull-up resistors be turned off. Although Xilinx strongly recommends against disabling internal pull-up resistors, the resistors can be turned off by setting the software option for termination to "Float." However, designers must recognize that in XPLA3 devices, when voltage at a pin is allowed to float, the I/O cell will allow the pin to exist in one of two states: the pin will either be driven High, or it will be allowed to float, depending on the last logic level prior to the floating condition. Each I/O cell will drive its respective pin with a logic High level if the previous logic state was High prior to the floating condition. If the previous logic state was Low prior to the floating condition, then the I/O cell will continue to allow the pin to float. This is commonly referred to as the Half Latch circuit.

When the pin floats, the voltage level may rise high enough for the Half Latch to sense logic High, in which case the I/O cell will drive the pin at a logic High level. However, if floating voltage never reaches this threshold, the pin will continue to float. This Half Latch is always enabled, regardless if the pin is an input, output, or bidirectional signal. It can not be disabled**.**

The presence of a Half Latch means that an XPLA3 I/O pin will never be truly high impedance. XPLA3 devices are designed with low power in mind, and hence, the Half Latch attempts to force the I/O pin High. Allowing for a truly high impedance pin would mean drawing upwards of 20 uA per floating I/O pin. The current draw could be quite substantial if multiplied across several I/O pins. Xilinx recommends against using XPLA3 devices in any design that requires I/O pins to truly float.

When pulling a pin Low externally, the value of an external pull-down resistor must be chosen such that it can overcome the presence of the Half Latch. An external pull-down resistor must force the pin voltage below V_{IL} Max, so that it does not affect either another attached chip, or the CPLD's own input buffer. If the pin is pulled in the Low direction, but fails to go below V_{IL} Max, the input pin can actually source current. This could happen if the Half Latch circuit continues to pull High, creating a current path from V_{CCIO} to ground via the series connection of the Half Latch and the external pull-down resistor. Hence, assign pull-down resistor sizes correctly. Xilinx recommends that any pull-down resistor value be 10k ohms or less.

Power-Up Characteristics

During power-up, the CoolRunner XPLA3 device I/Os may be undefined until V_{CC} rises above 1.0 Volt. This time period is called the Subthreshold State, as transistors have not yet fully been turned on. When V_{CC} rises above 1.0 Volt, the device I/Os enter the Quiescent State, and I/Os are disabled with weak pull-up as shown in Table 2. When V_{CC} reaches the threshold of the User Operation State (approximately 2.1V), user registers are initialized (typically within 200 µs) after which I/Os will assume the behavior determined by the user pattern, as shown in Figure 5.

If the device is in the erased state (before any user pattern is programmed), the device outputs remain disabled with weak pull-up. The JTAG pins are enabled to allow the device to be programmed at any time. All devices are shipped in the erased state from the factory.

If the device is programmed, the device inputs and outputs take on their configured states for normal operation.

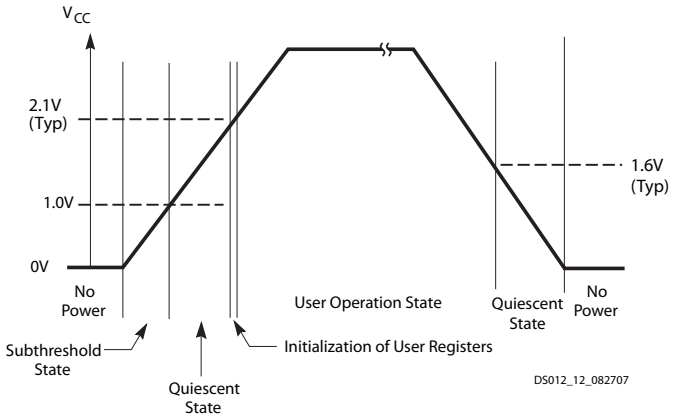

Figure 5: **Device Behavior During Power Up**

Table 2: **I/O Power-Up Characteristics**

Device Circuitry	Subthreshold State	Quiescent State	Erased Device Operation	Valid User Operation
Device I/Os	Undetermined	Disabled with Weak Pull-up	Disabled with Weak Pull-up	As Configured
Device Inputs/Clocks	Undetermined	High-Z	High-Z	High-Z
JTAG Controller	Undetermined	Disabled with Weak Pull-up	Enabled	As Configured

Other Features

XPLA3 devices also support "hot plugging". This refers to the ability to insert or remove devices from a system while it is powered on. This is accomplished in XPLA3 devices by two mechanisms. First, XPLA3 devices are not able to "steal" power from the I/O cells. Therefore, when an XPLA3 device is removed from a live system, any voltage spikes or fluctuations on the I/O pins will not damage the device. Second, when inserting into a live system, XPLA3 devices behave as shown in Table 2. Note that power and ground should be connected first. This prevents the XPLA3 device from sending any spurious signals to the system that could disrupt or damage the system.

Similarly, signals may be applied to the XPLA3 device when it is not powered provided these signals meet the V_{CC} maximum specification of 3.6V. The pin will appear as a capacitive load to the signal driving the I/O.

Finally, XPLA3 I/O cells are capable of sinking and sourcing up to 8 mA. This allows greater flexibility when interfacing with other I/O systems.

Additional Information

[CoolRunner Datasheets and Application Notes]
[Device Packages]
[Online Store]

Conclusion

XPLA3 devices are designed to provide a wide range of I/O options. The I/O pins can be used to support input, output, or bidirectional signals. Futhermore, when configured as an output, there are five options for controlling the output of the I/O cells. Additionally, XPLA3 I/O cells are PCI compatible, 5V tolerant, capable of "hot plugging", capable of reducing EMI and can sink and source up to 8 mA. All of these features in one device provides for a very powerful, dynamic chip that can adapt to almost any need.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/14/00	1.0	Initial Xilinx release.
07/31/00	1.1	Updated.
03/15/01	1.2	Updated.
7/18/03	1.3	Updated
12/01/03	1.4	Updated
12/30/03	1.5	Added values for weak pull-up in UMC material.
03/11/05	1.6	Revised Half Latch discussion.
02/16/06	1.7	Change to PCI compatibility paragraph, page 5.
06/06/08	1.8	Added Power Up Characteristics section. Changes to hot plugging.