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Using the RGMII to Interface with the Gigabit Ethernet MAC

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Summary

The Reduced Gigabit Media Independent Interface (RGMII) is an alternative to the Gigabit Media Independent Interface (GMII). In this application note, an RGMII adaptation module is used to reduce the number of pins required to connect the Gigabit Ethernet MAC to a Gigabit PHY from 24 to 12. The RGMII achieves this 50 percent pin count reduction in the interface by using double-data-rate (DDR) flip-flops.

Introduction

This application note shows how to combine an RGMII adaptation module with the GMII configuration of the Gigabit Ethernet MAC v3.0, resulting in a Gigabit MAC with an RGMII interface. A reference design and the required RGMII adaptation module are included with this application note. The LogiCORE™ 1-Gigabit Ethernet MAC v3.0 is available under license through the Xilinx IP Center, www.xilinx.com/ipcenter.

The RGMII adaptation module was designed to the IEEE Std 802.3®-2000. Support is provided for the Hewlett-Packard *Reduced Gigabit Media Independent Interface (RGMII),* versions 1.3 and 2.0. The reference design is supported in the Virtex™-II Pro family and is provided in both Verilog and VHDL source code formats.

Features

The RGMII reference design features the following:

- Compatible with the 1-Gigabit Ethernet MAC v3.0
- Compatible with the *HP RGMII Specification*, versions 1.3 and 2.0

Applications

The RGMII reference design can be used:

- In switching applications
- With a mezzanine daughter card that contains a Marvell Alaska 88E1111 10/100/1000 Mb/s transceiver in RGMII mode connected to the Virtex-II Pro ML32*x* series of Xilinx evaluation platforms

Implementation

The RGMII adaptation module is connected to the RX data, RX error, and RX data valid ports on the *receive* side of the 1-Gigabit Ethernet MAC core, and to the TX data, TX error, and TX enable ports on the *transmit* side. All signals are synchronous with a 125 MHz clock signal. The RGMII data signals switch on the positive and negative edges of the clock. The two control signals are multiplexed: one arrives on the positive clock edge, the other on the negative edge.

Figure 1 shows the interface between the 1-Gigabit Ethernet MAC core and the RGMII adaptation module.

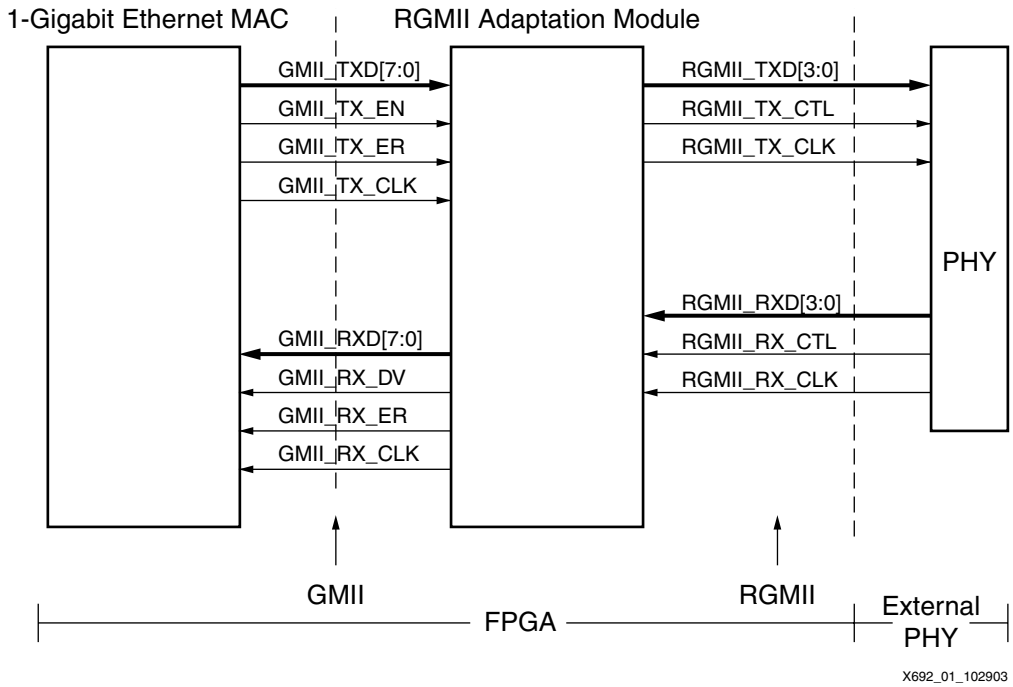

Figure 1: **High-Level Block Diagram**

The **GMII_TX_CLK** clock runs at 125 MHz and is provided to the RGMII adaptation module.

Figure 2, page 3 shows the RGMII_TX sub-module that connects to a set of DDR D-type flip-flops (FDDRRSE). When data from the **GMII_TXD[7:0]** data bus enters the adaptation module, the lower four bits (**GMII_TXD[3:0]**) are registered on the positive edge of the **RGMII_TX_CLK** clock, and the upper four bits (**GMII_TXD[7:4]**) are registered on the negative edge of the **RGMII_TX_CLK** clock. The outputs of these two registers go to the FDDRRSEs that combine the signals to form **RGMII_TXD[3:0]**, which switches on both clock edges.

The transmit control signals are multiplexed. **GMII_TX_EN** is registered on the positive edge of the **RGMII_TX_CLK** clock. A logical derivative of **GMII_TX_EN** and **GMII_TX_ER** is registered on the negative edge of the **RGMII_TX_CLK** clock. The outputs of these registers go to an FDDRRSE that combines the signals to form **RGMII_TX_CTL**, which switches on both clock edges. The timing diagram for the transmit side (Figure 2, page 3) shows two clock cycles of delay before data and control signals are presented on the RGMII interface.

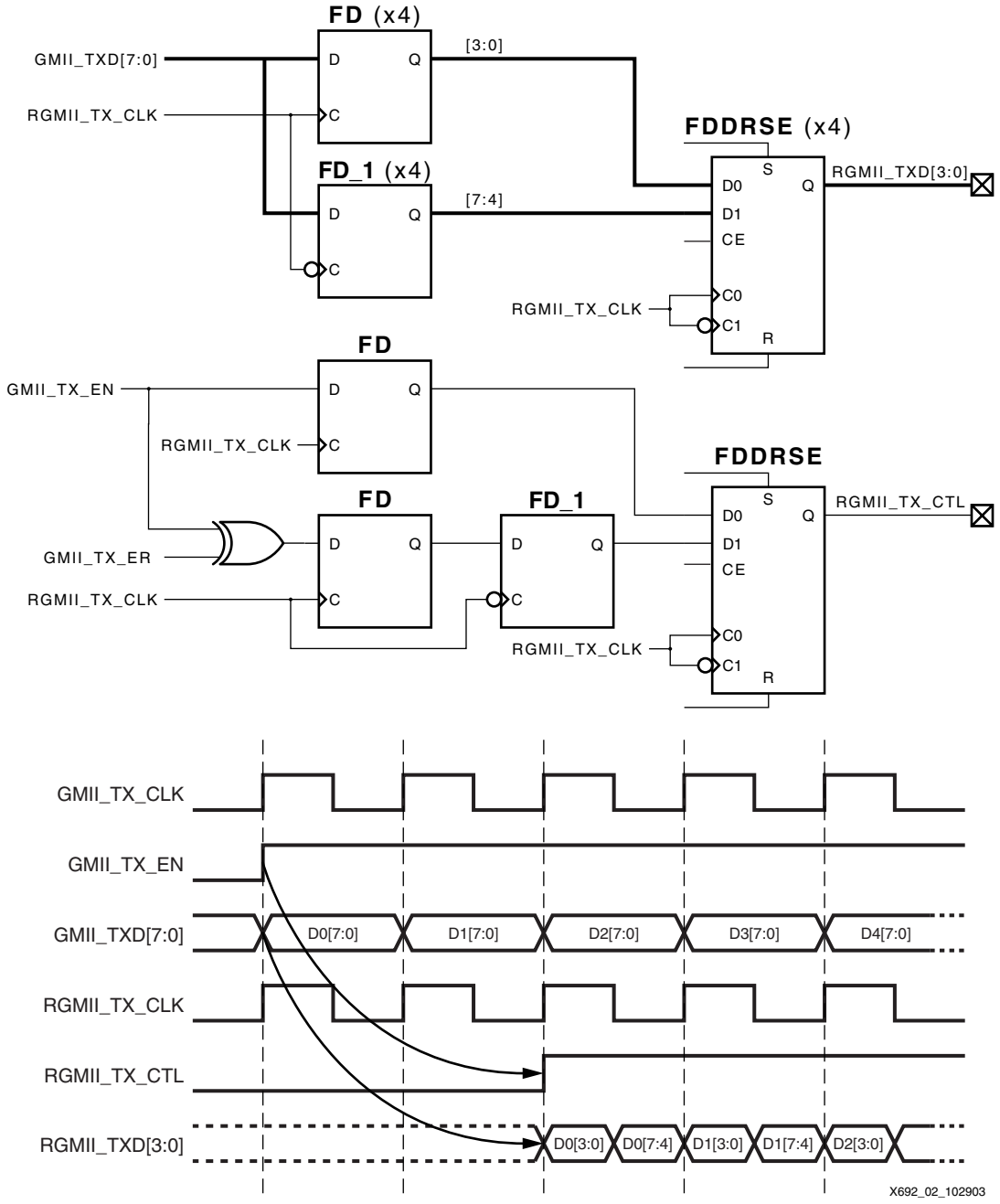

Figure 2: **RGMII Transmit Side**

Figure 3, page 4 shows the RGMII_RX sub-module. It is similar to the RGMII_TX submodule, but it connects instead to a set of DDR Input D-type flip-flops (IFDDRRSE). RGMII data from the IFDDRRSE flip-flops is registered on the positive and negative edges of the **RGMII_RX_CLK** clock. The output of the 4-bit registers is clocked into an 8-bit register on the positive edge of **RGMII_RX_CLK** to synchronize it; the output is then registered again and presented as the **GMII_RXD[7:0]** data bus. These additional registers synchronize the data with the control signals.

The RGMII control signals are demultiplexed by the adaptation module. **GMII_RX_DV** is registered from the IFDDRRSE on the positive edge of **RGMII_RX_CLK**. **GMII_RX_ER** is registered on the negative edge of **RGMII_RX_CLK**. The outputs of both registers are clocked on the positive edge of **RGMII_RX_CLK** to synchronize them. The output of the **GMII_RX_DV** synchronization register is registered again and passed directly to the GMII interface. The outputs of the **GMII_RX_DV** and **GMII_RX_ER** synchronization registers are XORed and registered to produce the GMII interface's **GMII_RX_ER** signal. The timing diagram for the receive side (Figure 3) shows three clock cycles of delay before data and control signals are presented on the GMII interface.

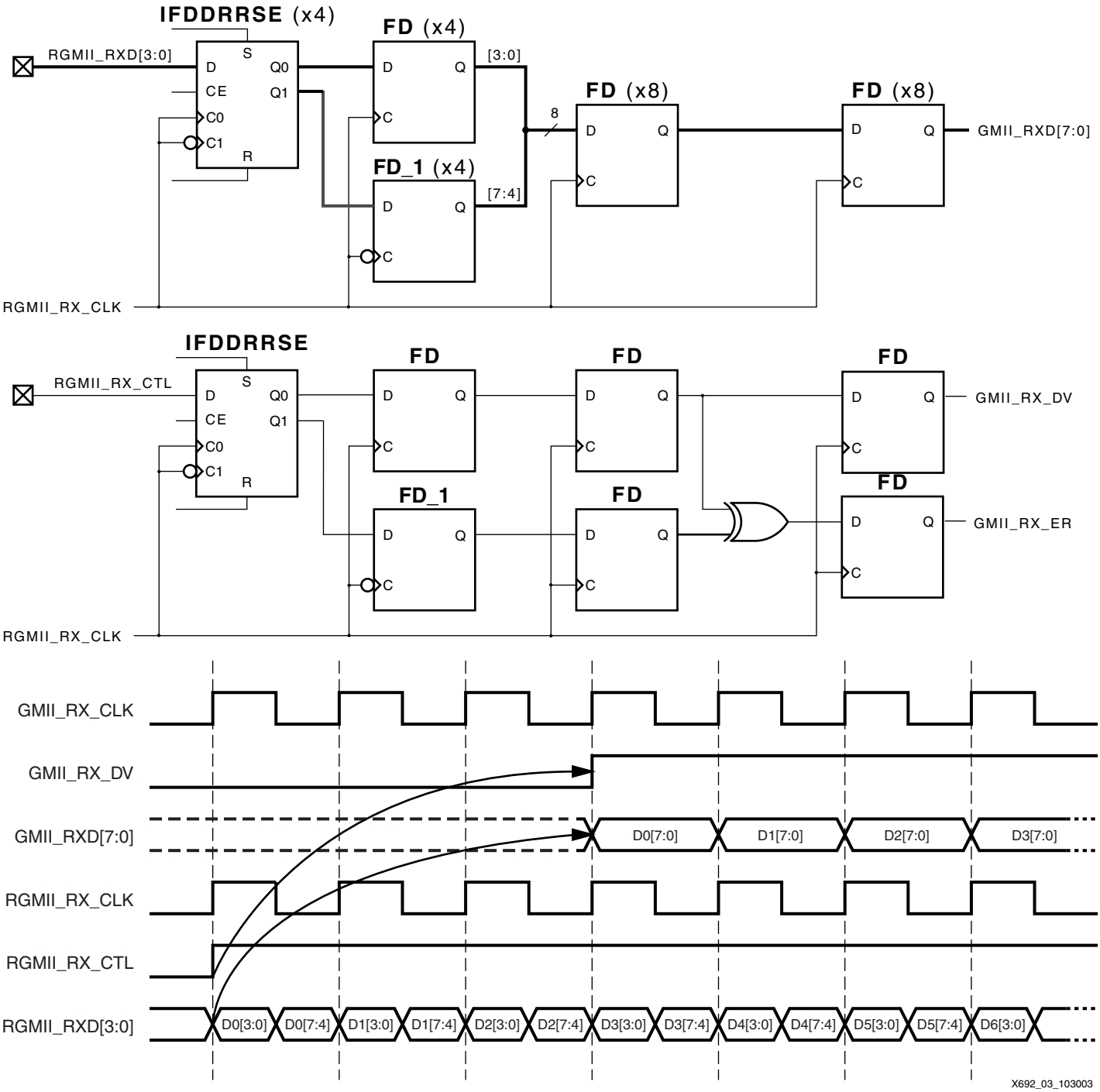

Figure 3: **RGMII Receive Side**

Figure 4 shows the RX status register that handles the **GMII_RX_ER** encoding that is described in the *HP RGMII Specification*. The status bits use the **GMII_RXD[3:0]** signals to determine the link, speed, and duplex status of the PHY. These signals can be connected to LEDs or registers.

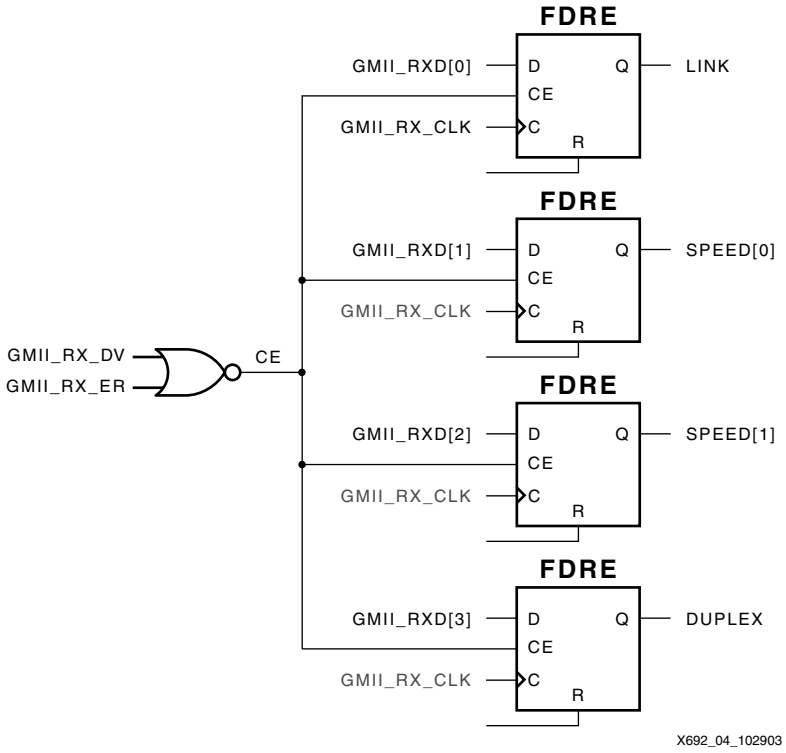

Figure 4: **Receive Status Register**

Clock Considerations

For correct operation, data must arrive at least 2 ns before each clock edge on both the transmit and the receive side. From the *HP RGMII Specification, v1.3*, this clock skew is achieved by adding the delay on the traces of the clock going to the PHY on the printed-circuit board. From the *HP RGMII Specification, v2.0*, this clock skew is achieved inside the design using the 90 degree phase shift of the Digital Clock Manager (DCM) unit. Figure 5 shows the DCMs that are needed to achieve this clock skew.

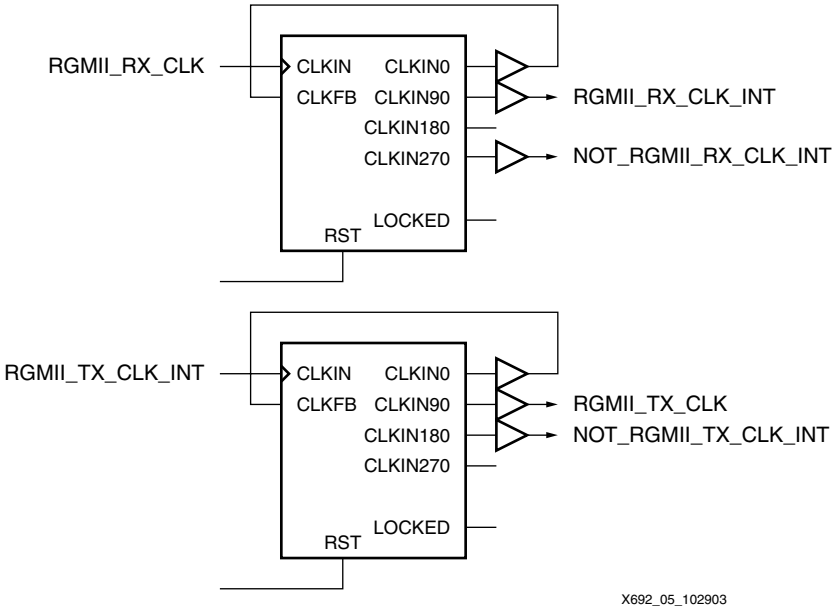

Figure 5: **DCMs Needed to Achieve Clock Skew**

The DCMs directly generate inverted clock signals for the RX and TX side DDR interfaces. These clock signals connect to the DDR interfaces with dedicated clock buffers. The RX inverted clock comes from the CLKIN270 port of the RGMII_RX_CLK DCM and is connected with a BUFG to the IFDDRRSEs on the RX side. The TX inverted clock comes from the CLKIN180 port of the RGMII_TX_CLK DCM and is connected with a BUFG to the FDDRRSEs on the TX side.

Signal Definitions

Table 1 shows the signals between the RGMII adaptation module and the PHY.

Table 1: **RGMII to PHY Interface Signal Definitions**

Signal	Direction	Description
RGMII_TX_CLK	Output	Transmit reference clock at 125 MHz
RGMII_TXD[3:0]	Output	Contains bits GMII_TXD[3:0] on positive edge of RGMII_TX_CLK and bits GMII_TXD[7:4] on negative edge of RGMII_TX_CLK
RGMII_TX_CTL	Output	Contains GMII_TX_EN on positive edge of RGMII_TX_CLK and a logical derivative of GMII_TX_EN XOR GMII_TX_ER on negative edge of RGMII_TX_CLK
RGMII_RX_CLK	Input	Receive reference clock from the PHY at 125 MHz

Table 1: **RGMII to PHY Interface Signal Definitions *(Continued)***

Signal	Direction	Description
RGMII_RXD[3:0]	Input	Contains bits GMII_RXD[3:0] on positive edge of RGMII_RX_CLK and bits GMII_RXD[7:4] on negative edge of RGMII_RX_CLK
RGMII_RX_CTL	Input	Contains GMII_RX_DV on positive edge of RGMII_RX_CLK and a logical derivative of GMII_RX_DV XOR GMII_RX_ER on negative edge of RGMII_RX_CLK

Table 2 shows the signals between the RGMII adaptation module and the GMII core.

Table 2: **RGMII to GMII Interface Signal Definitions**

Signal	Direction	Description
GMII_TXD[7:0]	Input	Transmit data to RGMII
GMII_TX_EN	Input	Data Enable control signal to RGMII
GMII_TX_ER	Input	Error control signal to RGMII
GMII_TX_CLK	Input	Clock out to RGMII
GMII_RXD[7:0]	Output	Received data from RGMII
GMII_RX_DV	Output	Data Valid control signal from RGMII
GMII_RX_ER	Output	Error control signal from RGMII
GMII_RX_CLK	Output	Clock signal from RGMII

Simulation

A simulation testbench accompanies this application note to verify the RGMII adaptation module connected to the 1-Gigabit Ethernet MAC. This testbench is similar to the one provided by the Xilinx CORE Generator™ tool and consists of a packet generator and an internal loopback path. Four different packets are generated, then verified through the statistics gathering registers. To run the testbench, use either the evaluation or the full license version of the LogiCORE 1-Gigabit Ethernet MAC v3.0.

Reference Design

The reference design files for this application note are written in both VHDL and Verilog and are available at www.xilinx.com/bvdocs/appnotes/xapp692.zip. The reference design consists of an echo design. It uses the Gigabit Ethernet MAC FIFO v2.0 bundled with this reference design and additional logic that swaps the destination and source Ethernet MAC addresses of incoming frames before retransmitting them. Figure 6, page 8 shows the top level diagram for the GMAC RGMII echo design.

The reference design was verified using the Xilinx Virtex-II Pro ML320 Development Platform with a mezzanine daughter card containing a Marvell Alaska 88E1111 10/100/1000 Mb/s Transceiver. The bitstream was implemented using ISE 5.2i with Service Pack 3 targeting a –5 speed grade XC2VP7 device. The bitstream contains the full system evaluation version of the 1-Gigabit Ethernet MAC. This evaluation core will timeout after eight hours of usage. To obtain more information about the development boards, please contact your local FAE.

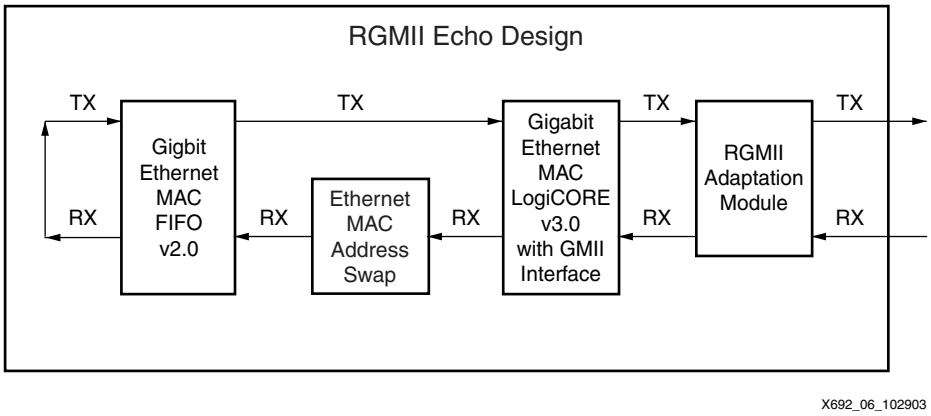

Figure 6: **Top Level Diagram for the GMAC RGMII Echo Design**

The functionality of this echo design is:

1. The 1-Gigabit Ethernet MAC is connected to the RGMII adaptation module and is generated with the following options:
   - GMII interface
   - Full and half-duplex capability
   - MDIO interface
   - Statistics gathering using block RAM

   The RGMII signals are connected to the appropriate ports of the RGMII-mode PHY.
2. The MAC address swap module takes Ethernet frames from the MAC, swaps the source and destination MAC addresses, and puts them into the GMAC FIFO for transmission. Once this packet is processed, it goes to the GMAC FIFO. Figure 7 shows how the MAC addresses are swapped in the header of the packet where Destination MAC Address (1) equals Source MAC Address (2) and Destination MAC Address (2) equals Source MAC Address (1).

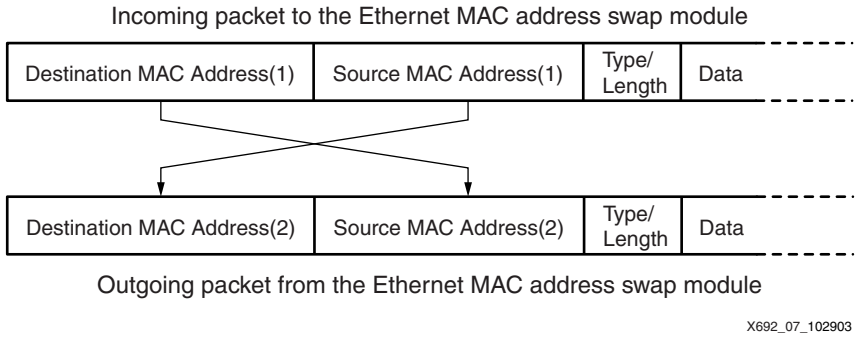

Figure 7: **Example of MAC Addresses being Swapped**

3. The GMAC FIFO buffers data from the MAC address swap module. This data is sent back to the transmit side of the MAC to be transmitted to the PHY.

Figure 8 shows the hardware setup for verifying this reference design as follows:

- A computer with packet generator software is connected to a Gigabit Ethernet switch
- The ML320 board with a mezzanine daughter card receives the incoming packet and echoes it back
- A sniffer tool monitors and verifies the incoming and outgoing packets from the ML320 board

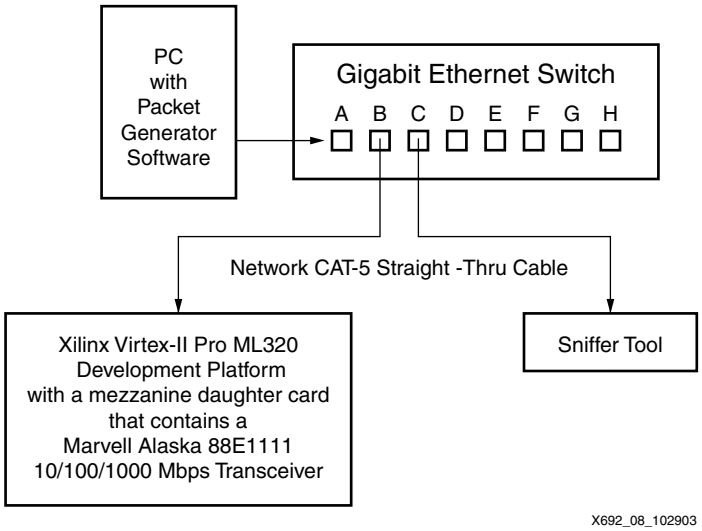

Figure 8: **Hardware Set Up for Verifying the Reference Design**

Design Hierarchy

The design hierarchy for this reference design is shown below. A bitstream with the Xilinx 1-Gigabit Ethernet MAC v3.0 evaluation core and a testbench described in "Simulation," page 7 are provided.

```
<GMAC DESIGN>            top level design)
|___build                (implementation, bitstream, .ucf)
|    |___ml320_phy0
|    |___ml320_phy1
|___src                  (hdl code)
|    |___gmac_fifo
|    |___rgmii
|___synth                (synthesis .ngc)
|___test                 (simulation, back-annotated files, testbench)
     |___func_sim
     |    |___backanno
     |    |___fpga
     |___testbench
```

Device Utilization

Table 3 shows the logic resources used by both the RGMII adaptation module and the RGMII echo reference design.

Table 3: **Logic Resources**

Logic Resources	Slice	LUT	FF	BRAM	DCM
RGMII Adaptation Module	18	7	20	0	0
RGMII Echo Reference Design	1,513	1,949	1,571	5	2

Conclusion

The RGMII adaptation module in this application note reduces the number of pins that are required to communicate with a Gigabit PHY by 50 percent. This application note illustrates how the RGMII adaptation module is implemented and used with the LogiCORE 1-Gigabit Ethernet MAC v3.0. The reference design, which includes the Gigabit Ethernet MAC FIFO v2.0 and the Ethernet MAC address swap module, demonstrates RGMII operation.

References

1. DS200, *1-Gigabit Ethernet MAC Core with PCS/PMA Sublayers (1000BASE-X) or GMII v3.0*
2. Hewlett-Packard Company. 2000. *Reduced Gigabit Media Independent Interface (RGMII) Specification, v1.3*
3. Hewlett-Packard Company. 2002. *Reduced Gigabit Media Independent Interface (RGMII) Specification, v2.0*
4. Xilinx IP Center Design Example, *1-Gigabit Ethernet MAC FIFO v2.0*

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/31/03	1.0	Initial Xilinx Release.
09/28/06	1.0.1	Miscellaneous typographical edits.