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High-Performance DDR2 SDRAM Interface Data Capture Using ISERDES and OSERDES

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Summary

This application note describes a data capture technique for a high-performance DDR2 SDRAM interface. This technique uses the Input Serializer/Deserializer (ISERDES) and Output Serializer/Deserializer (OSERDES) features available in every Virtex®-4 FPGA I/O.

Introduction

A DDR2 SDRAM interface is source-synchronous where the read data and read strobe are transmitted edge aligned. To capture this transmitted data using Virtex-4 FPGAs, either the strobe or the data can be delayed. In this design, the read data is captured in the delayed strobe domain and recaptured in the FPGA clock domain in the ISERDES. The received serial, double data rate (DDR) read data is converted to 4-bit parallel data at the frequency of the interface using the ISERDES. The 4-bit parallel data has the same frequency of the interface because the OCLK and CLKDIV inputs of the ISERDES in the memory mode are clocked by the same fast clock.

The differential strobe is placed on a clock-capable I/O pair to access the BUFIO clock resource. The BUFIO clocking resource routes the delayed read DQS to its associated data ISERDES clock inputs. The write data and strobe transmitted by the FPGA use the OSERDES during write transactions. The OSERDES converts 4-bit parallel data at half the frequency of the interface to DDR data at the interface frequency. The following are clocked at half the frequency of the interface, resulting in improved design margin at frequencies of 267 MHz and above: controller, datapath, user interface, and all other FPGA slice logic.

Clocking Scheme

Figure 1 shows the clocking scheme for this design, which includes one digital clock manager (DCM) and one phase-matched clock divider (PMCD). The controller is clocked at half the frequency of the interface using CLKdiv_0. Therefore, the address, bank address, and command signals (RAS_L, CAS_L, and WE_L) are asserted for two clock cycles (known as *2T* timing) of the fast memory interface clock. The control signals (CS_L, CKE, and ODT) are twice the rate (DDR) of the half frequency clock CLKdiv_0, ensuring that the control signals are asserted for just one clock cycle of the fast memory interface clock. The clock is forwarded to the external memory device using the Output Dual Data Rate (ODDR) flip-flops in the Virtex-4 FPGA I/O. This forwarded clock is 180° out of phase with CLKfast_0.

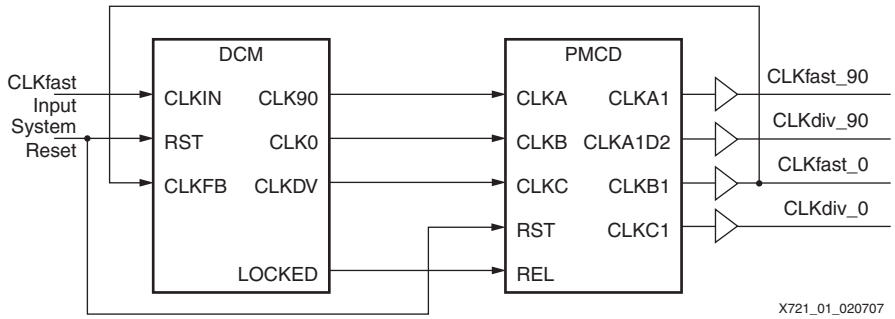

Figure 1: **Clocking Scheme for the High-Performance Memory Interface Design**

Figure 2 shows the command and control timing diagram.

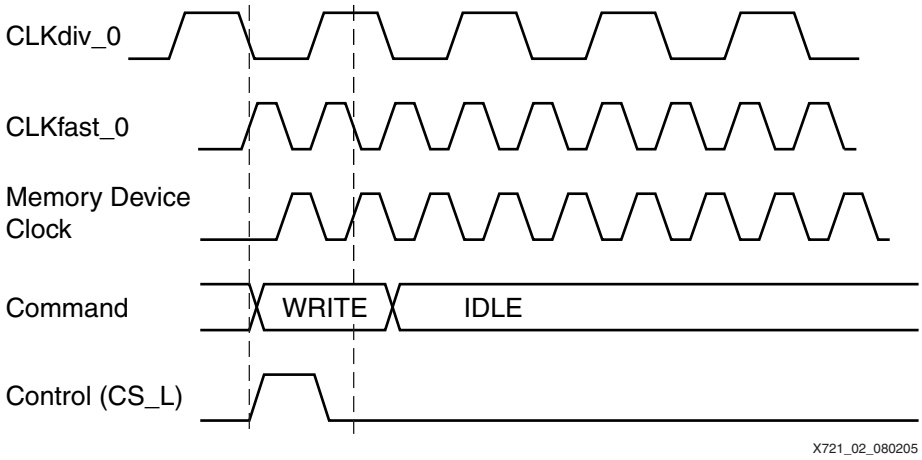

Figure 2: **Command and Control Timing**

Write Datapath

The write datapath uses the built-in OSERDES available in every Virtex-4 FPGA I/O. The OSERDES transmits the data (DQ) and strobe (DQS) signals. The memory specification requires DQS to be transmitted center aligned with DQ. The strobe (DQS) forwarded to the memory is 180° out of phase with CLKfast_0. Therefore, the write data transmitted using OSERDES must be clocked by CLKfast_90 and CLKdiv_90 as shown in Figure 3.

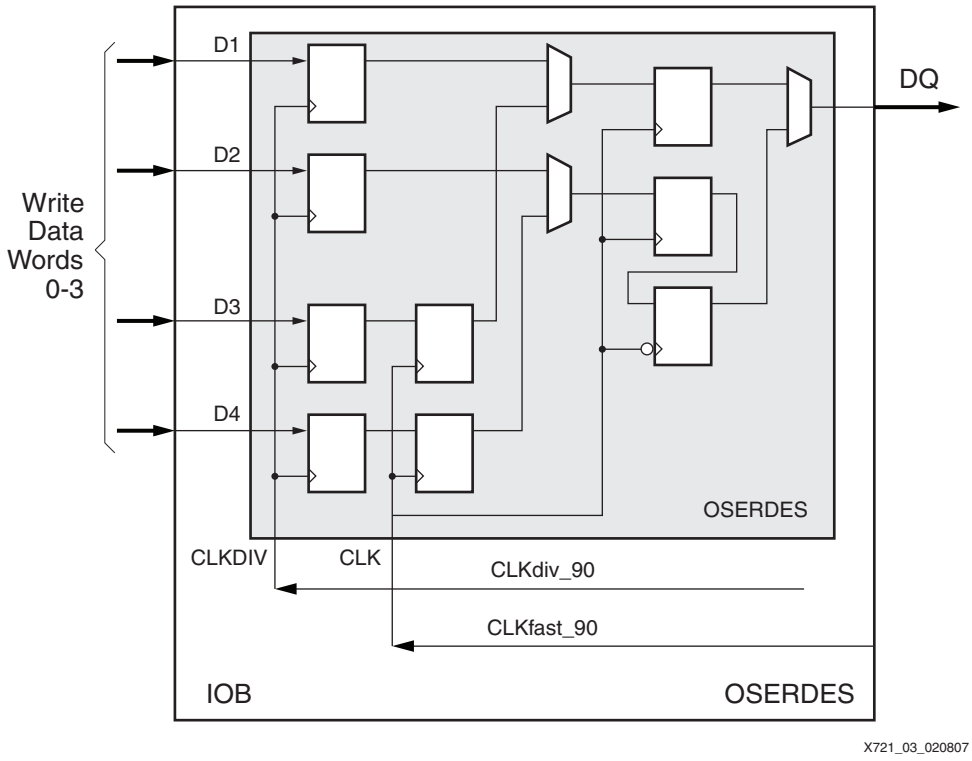

Figure 3: **Write Data Transmitted Using OSERDES**

Figure 4 shows the timing diagram for write DQS and DQ signals.

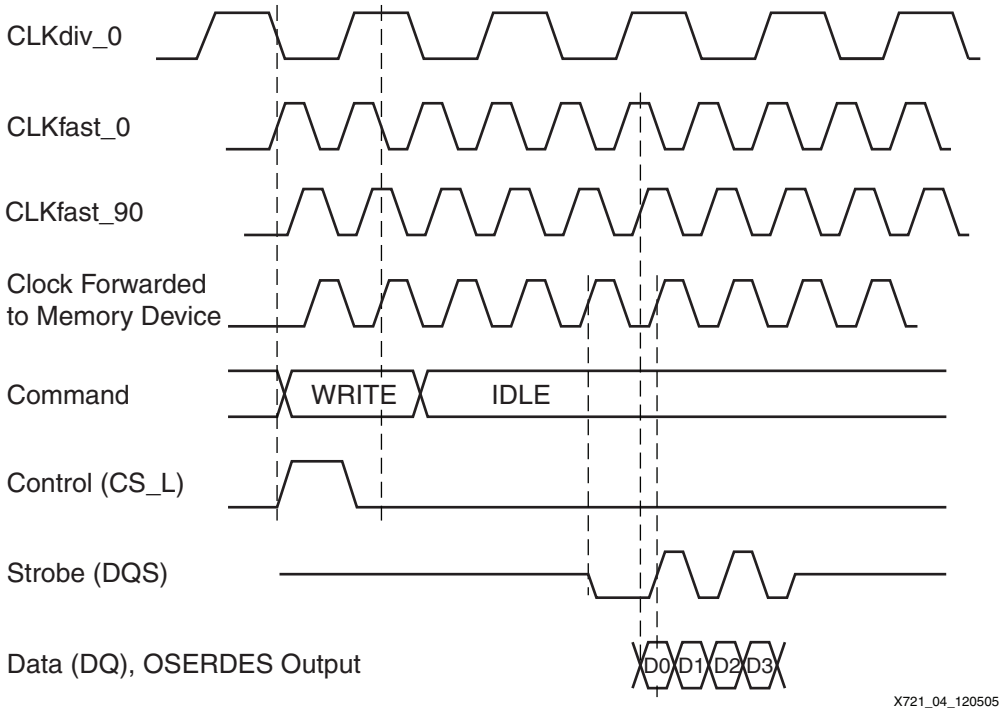

Figure 4: **Write Strobe (DQS) and Data (DQ) Timing for a Write Latency of Four**

Write Timing Analysis

Table 1 shows the write timing analysis for an interface at 300 MHz (600 Mb/s).

Table 1: **Write Timing Analysis at 300 MHz**

Uncertainty Parameters	Value (ps)	Uncertainties before DQS (ps)	Uncertainties after DQS (ps)	Meaning
T_{CLOCK}	3,333			Clock period.
$T_{MEMORY\_DLL\_DUTY\_CYCLE\_DIST}$	150	150	150	DCM duty-cycle distortion.
T_{DATA_PERIOD}	1,666			Data period is half the clock period with duty-cycle distortion subtracted from it.
T_{SETUP}	300	300	0	Specified by memory vendor.
T_{HOLD}	300	0	300	Specified by memory vendor.
$T_{PACKAGE\_SKEW}$	20	20	20	PCB trace delays for DQS and its associated DQ bits are adjusted to account for package skew. The listed value represents dielectric constant variations.
T_{JITTER}	0	0	0	Same DCM used to generate DQS and DQ.
$T_{CLOCK\_SKEW-MAX}$	100	100	100	Clock skew between DQ bits within a byte.
$T_{PMCD\_CLK\_SKEW}$	150	150	150	Phase offset error between different clock outputs of the same PMCD.
$T_{PCB\_LAYOUT\_SKEW}$	50	50	50	Skew between data lines and the associated strobe on the board.
Total Uncertainties		770	770	
Start and End of Valid Window		770	896	
Final Window			126	Final window equals 896–770.

Notes:

1. Skew between output flip-flops and output buffers in the same bank is considered to be minimal over voltage and temperature.

Controller to Write Datapath Interface

Table 2 lists the signals required from the controller to the write datapath.

Table 2: **Controller to Write Datapath Signals**

Signal Name	Signal Width	Signal Description	Notes
ctrl_WrEn	1	Output from the controller to the write datapath. Write DQS and DQ generation begins when this signal is asserted.	Asserted for two CLKDIV_0 cycles for a burst length of 4 and three CLKDIV_0 cycles for a burst length of 8. Asserted one CLKDIV_0 cycle earlier than the WRITE command for CAS latency values of 4 and 5. Figure 5 and Figure 6 show the timing relationship of this signal with respect to the WRITE command.
ctrl_wr_disable	1	Output from the controller to the write datapath. Write DQS and DQ generation ends when this signal is deasserted.	Asserted for one CLKDIV_0 cycle for a burst length of 4 and two CLKDIV_0 cycles for a burst length of 8. Asserted one CLKDIV_0 cycle earlier than the WRITE command for CAS latency values of 4 and 5. Figure 5 and Figure 6 show the timing relationship of this signal with respect to the WRITE command.
ctrl_Odd_Latency	1	Output from controller to write datapath.	Asserted when the selected CAS latency is an odd number (such as 5). Required for generation of write DQS and DQ after the correct write latency (the number of clock cycles after a write command is issued). (Write latency = CAS latency – 1.)

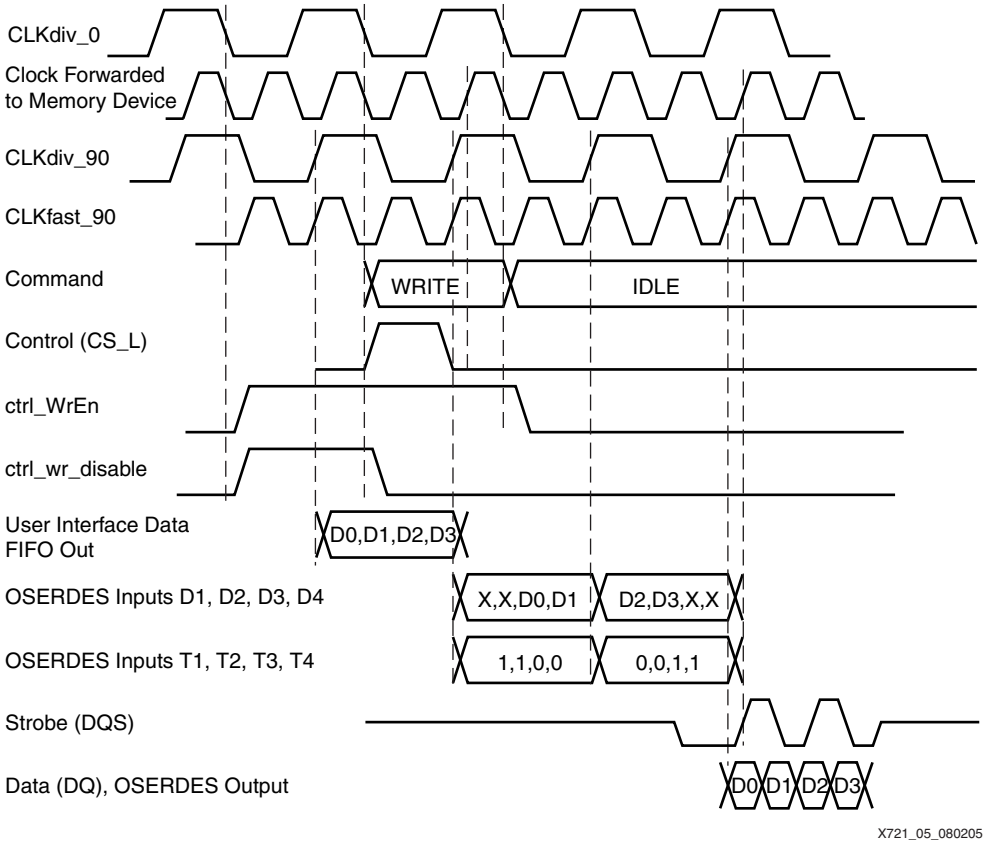

Figure 5: **Write DQ Generation for a Write Latency of 4 and a Burst Length of 4**

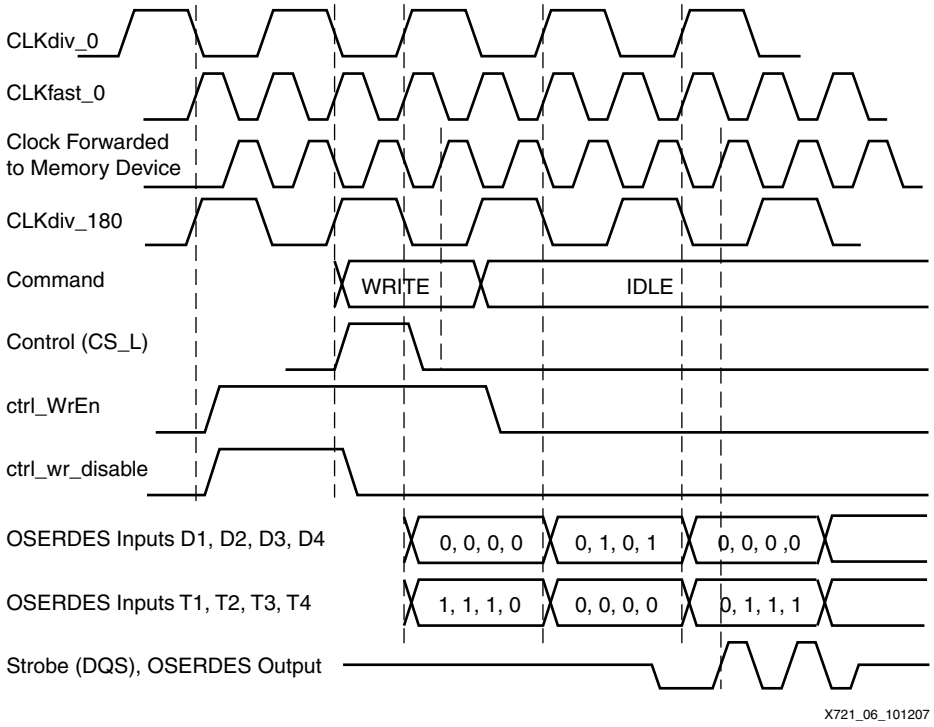

Figure 6: **Write DQS Generation for a Write Latency of 4 and a Burst Length of 4**

Read Datapath

The read datapath comprises the read data capture and recapture stages. Both stages are implemented in the built-in ISERDES available in every Virtex-4 I/O. In the memory mode, ISERDES has three clock inputs: CLK, OCLK, and CLKDIV. For the earlier version of this design (MIG1.6), these three clock inputs were provided as follows:

- CLK: Read DQS routed on the BUFIO was provided as the CLK input of the ISERDES.
- OCLK: The CLKfast_90 clock was provided as the OCLK input of the ISERDES.
- CLKDIV: The CLKDIV input of the ISERDES was provided as a selection between CLKdiv_90 or its inverted version from a BUFGMUX. The BUFGMUX enabled selection of either the rising or falling edge of the divided clock during calibration, based on the number of IDELAY taps required. The CLKDIV edge that yielded the lower tap count was selected.

Also, for the earlier version of this design, the total number of taps required for data in the worst case was three-quarters of a fast clock period. This scheme required one additional DCM to invert the divided clock because the PMCD cannot invert clocks. The result of this clocking scheme was additional jitter on the CLKDIV input of the ISERDES compared to OCLK input.

In the latest version of this design (MIG1.7), to avoid using the additional DCM and reduce clock jitter, the divided clock is not input to the ISERDES. The OCLK and CLKDIV inputs of the ISERDES are clocked by the fast clock, CLKfast_90, that has the same frequency as the interface. In the worst case, the total number of IDELAY taps required to align read strobe (DQS) and read data (DQ) to the rising edge of the FPGA clock (CLKfast_90) remains three-quarters fast clock period. The advantage of this design is the savings in resources, namely one DCM, one BUFGMUX, and lower jitter clocks. For the latest version of this design, the clock inputs are as follows:

- CLK: The read DQS routed using BUFIO provides the CLK input of the ISERDES as shown in Figure 7.
- OCLK: The OCLK input of ISERDES is connected to the CLK input of OSERDES in hardware. In this design, the CLKfast_90 clock is provided to the ISERDES OCLK input and the OSERDES CLK input. The clock phase used for OCLK is dictated by the phase required for write data.
- CLKDIV: The CLKDIV input is also provided with CLKfast_90.

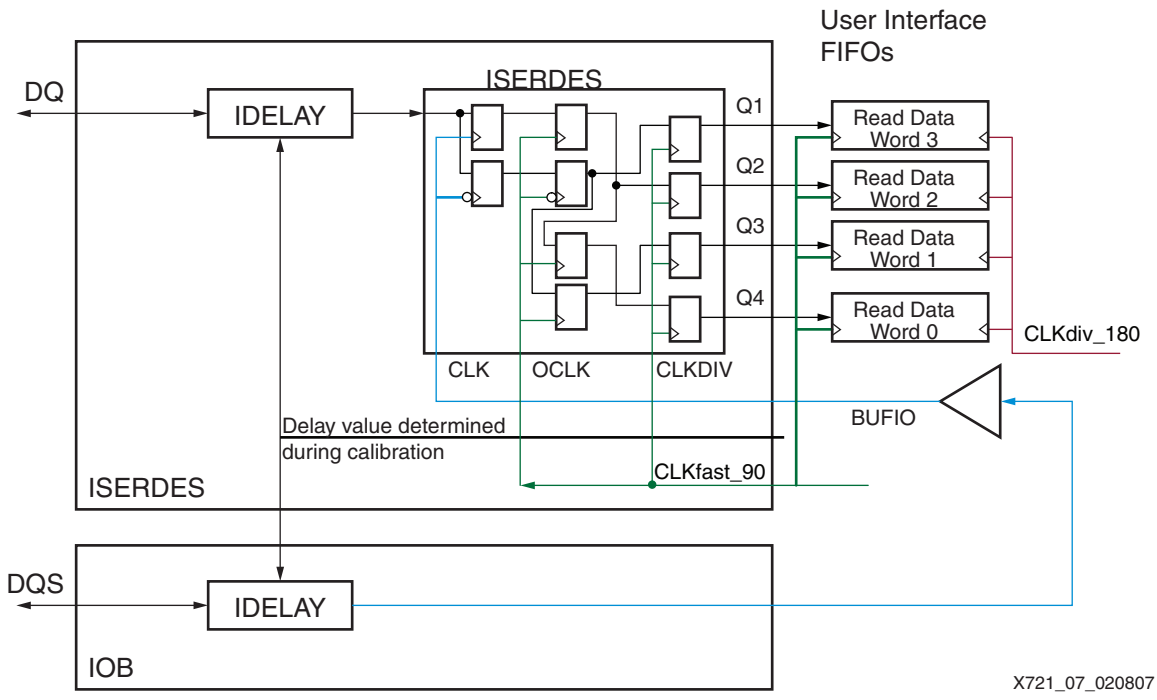

Figure 7: **Read Data Capture Using ISERDES**

Read Timing Analysis

To capture read data without errors in the ISERDES, read data and strobe must be delayed to meet the setup and hold times of the flip-flops in the FPGA clock domain. Read data (DQ) and strobe (DQS) are received edge aligned at the FPGA. The differential DQS pair must be placed on a clock-capable I/O pair in order to access the BUFIO resource. The received read DQS is then routed through the BUFIO resource to the CLK input of the ISERDES of the associated data bits. The delay through the BUFIO and clock routing resources shifts the DQS to the right with respect to data. The total delay through the BUFIO and clock resource is 595 ps in a -11 speed grade device and 555 ps in a -12 speed grade device.

Table 3 lists the read timing analysis that is required to determine the data margin at 300 MHz.

Table 3: **Read Timing Analysis at 300 MHz**

Parameter	Value (ps)	Meaning
T_{CLOCK}	3,333	Clock period.
T_{PHASE}	1,667	Data period for DDR data.
T_{SAMP_BUFIO}	350	Sample Window from Virtex-4 FPGA data sheet for a -12 device. It includes setup and hold for an IOB FF, clock jitter, and 150 ps of tap uncertainty.
T_{BUFIO_DCD}	100	BUFIO clock resource duty-cycle distortion.
$T_{DQSQ} + T_{QHS}$	580	Worst-case memory uncertainties that include VT variations and skew between DQS and its associated DQs.
IDELAY Tap Jitter	348	Total tap jitter when using 29 taps. The worst-case jitter through each tap is 12 ps.
Total Uncertainties	1,378	
Window	289	Worst-case window.

Notes:

1. T_{SAMP_BUFIO} is the sampling error over VT for a DDR input register in the IOB when using the BUFIO clocking resource and the IDELAY.
2. All the parameters listed are uncertainties to be considered when using the per bit calibration technique.
3. Parameters such as BUFIO skew, package_skew, pcb_layout_skew, and part of TDQSQ and TQHS are calibrated out with the per bit calibration technique. Inter-symbol interference, crosstalk, and contributors to dynamic skew are not considered in this analysis.

Per Bit Deskew Data Capture Technique

To ensure reliable data capture in the OCLK and CLKDIV domains in the ISERDES, a training sequence is required after memory initialization. The controller issues a WRITE command to write the following known data pattern: First Rising data = FF, First Falling Data = 00, Second Rising Data = AA, Second Falling Data = 55. The controller then issues back-to-back read commands to read back the written data from this specified location. The DQ bus ISERDES outputs Q1, Q2, Q3, and Q4 are then compared with the known data pattern.

The DQS is delayed more than DQ because of the propagation delay through the BUFIO and the clock resource. The DQS is delayed by two additional taps to push it further in the DQ valid window. The flow diagram of the calibration algorithm is shown in Figure 8.

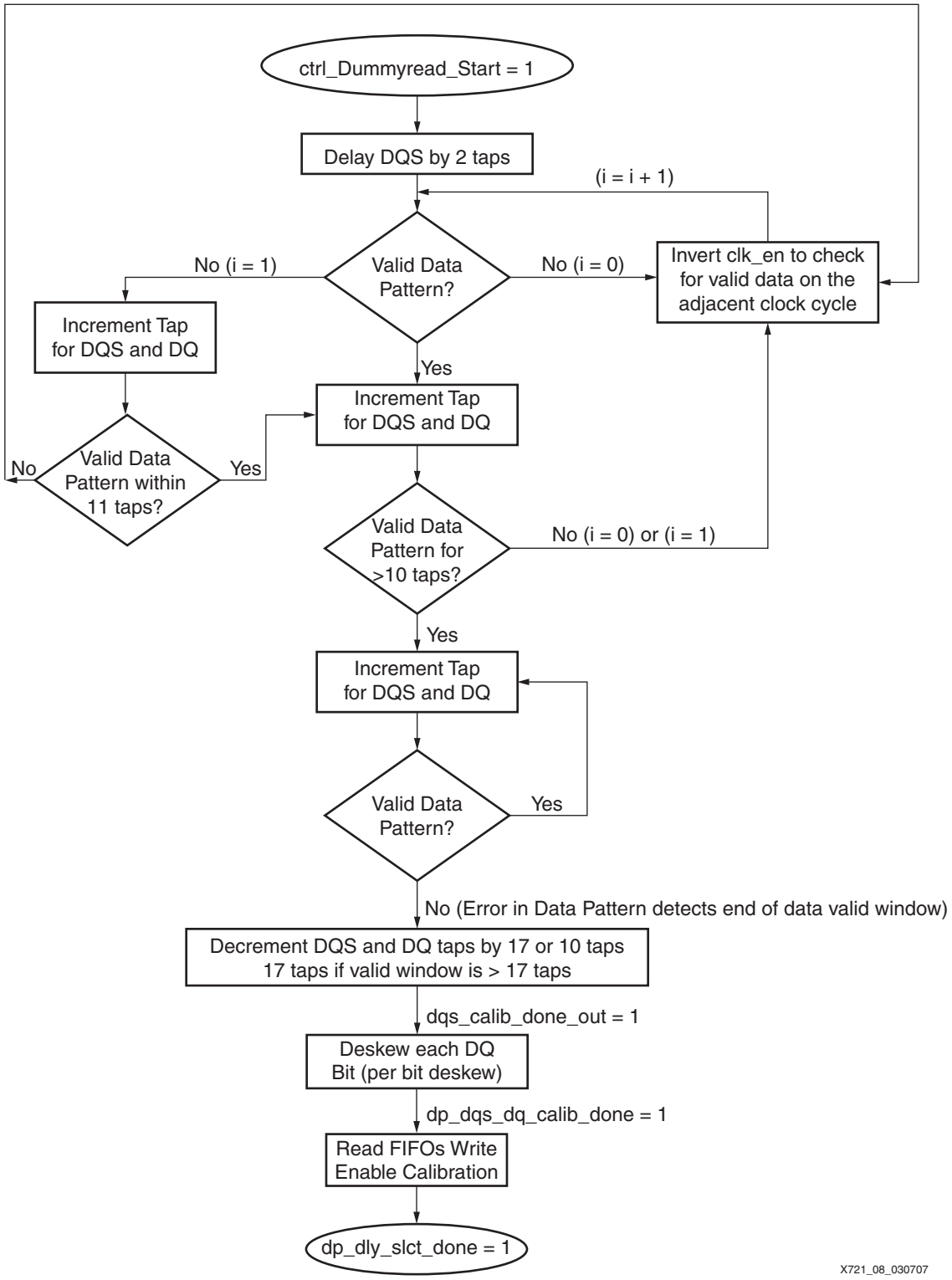

Figure 8: **Read Data and Strobe Delay Calibration Flow**

Figure 9 shows the read timing waveform for a burst length of 8. The read data, DQ, is first captured in the DQS domain and then transferred to the FPGA fast clock domain (CLKfast_90). The waveform shows a case where the DQS and DQ are aligned correctly to the FPGA clock domain, and the correct data sequence is available at the output of the ISERDES. For a burst length of 8, valid data is available every alternate clock cycle. The lower end of the frequency range for this design is limited by the number of available taps in the IDELAY block, the PCB trace delay, and the CAS latency of the memory device.

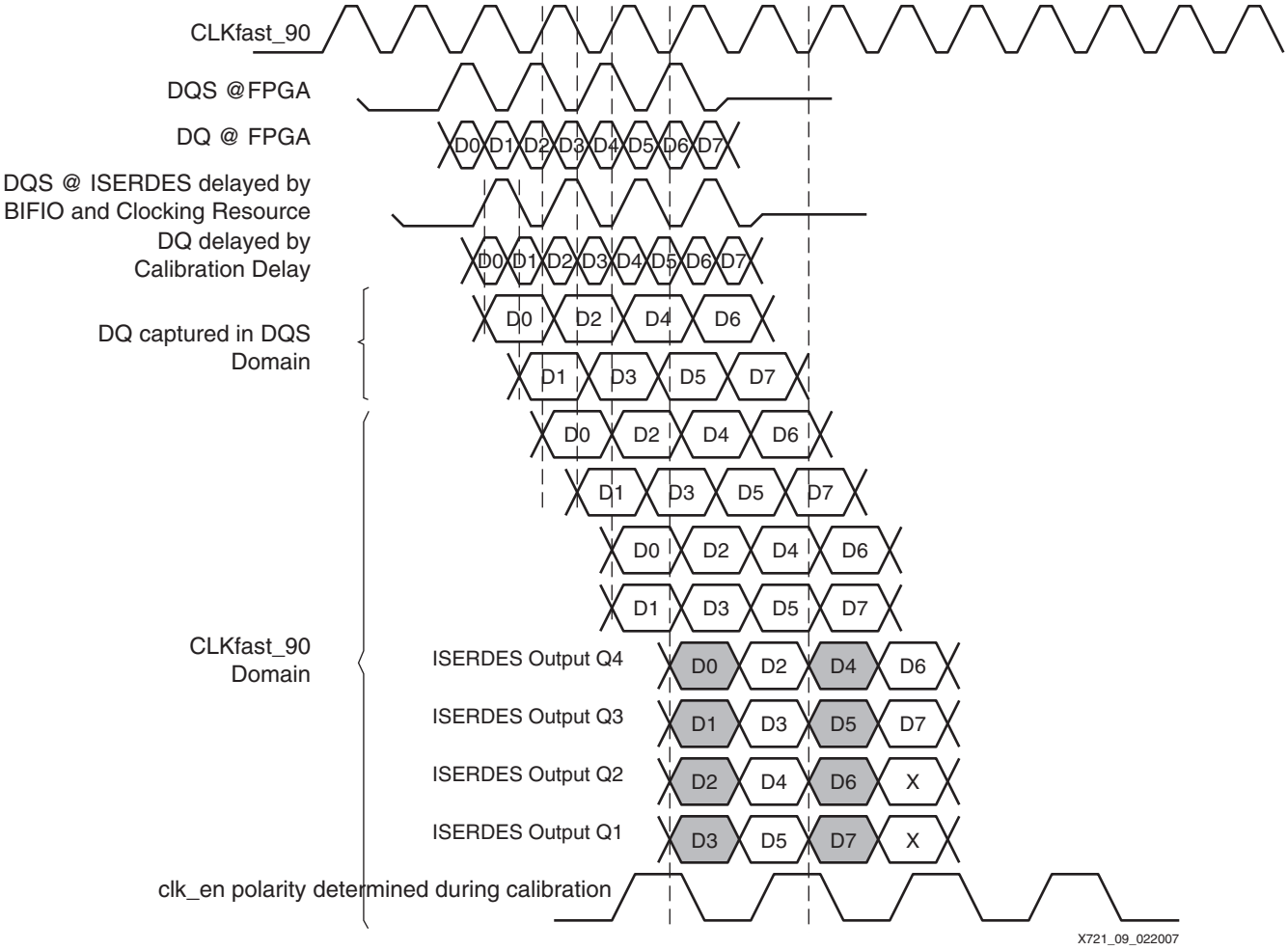

Figure 9: **Read Data and Strobe Capture Timing for Burst Length of 8**

Controller to Read Datapath Interface

Table 4 lists the control signals between the controller and the read datapath.

Table 4: **Signals between Controller and Read Datapath**

Signal Name	Signal Width	Signal Description	Notes
ctrl_Dummyread_Start	1	Output from the controller to the read datapath. When this signal is asserted, the strobe and data calibration begin.	This signal must be asserted when valid read data is available on the data bus. This signal is deasserted when the dp_dly_slct_done signal is asserted.
dp_dly_slct_done	1	Output from the read datapath to the controller indicating the strobe and data calibration are complete.	This signal is asserted when the data and strobe have been calibrated. Normal operation begins after this signal is asserted.
ctrl_RdEn_div0	1	Output from the controller to the read datapath used as the write enable to the read data capture FIFOs.	This signal is asserted for one CLKdiv_0 clock cycle for a burst length of 4 and two clock cycles for a burst length of 8. The CAS latency and additive latency values determine the timing relationship of this signal with the read state. Figure 10 shows the timing waveform for this signal with a CAS latency of 5 and an additive latency of 0 for a burst length of 4.

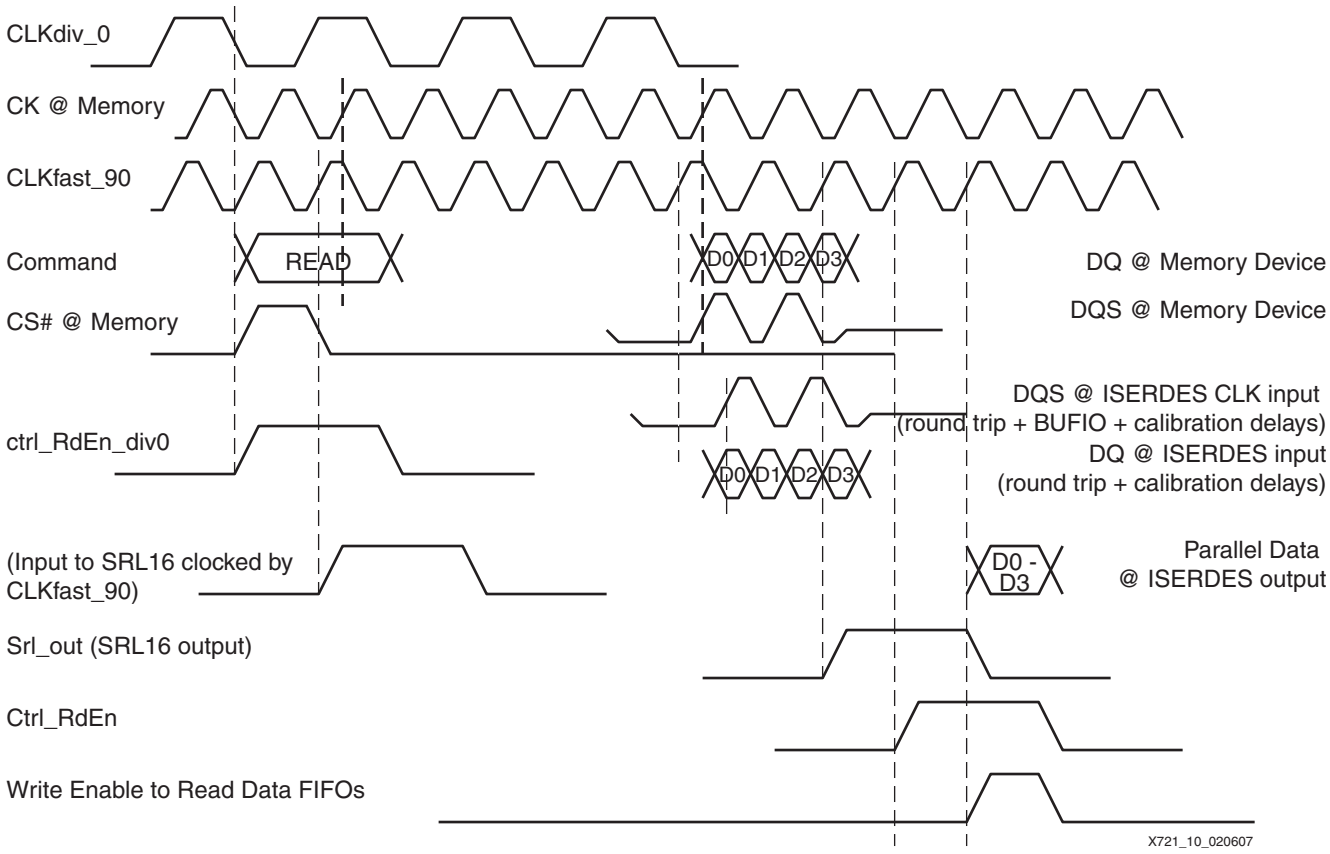

Figure 10: **Write-Enable Timing for CAS Latency of 5 and Burst Length of 4**

The ctrl_RdEn signal is required to validate read data because the DDR2 SDRAM devices do not provide a read valid or read-enable signal along with read data. The controller generates this read-enable signal based on the CAS latency and the burst length. This read-enable signal is input to an SRL16 (LUT-based shift register). The number of register stages required to align the read-enable signal to the ISERDES read data output is determined during calibration. One read-enable signal is generated for each data byte.

Figure 11 shows the read-enable logic block diagram.

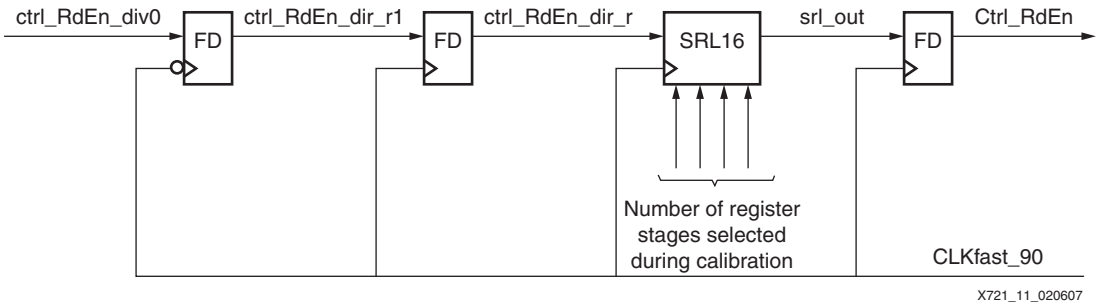

Figure 11: **Read Data FIFO Write-Enable Logic**

Reference Design

Figure 12 shows the hierarchy of the reference design. The mem_interface_top is the top-level module. The reference design for the DDR2 SDRAM interface is integrated with the MIG tool. This tool has been integrated with the Xilinx CORE Generator™ software. For the latest version of the design, download the IP update on the Xilinx website at: http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp.

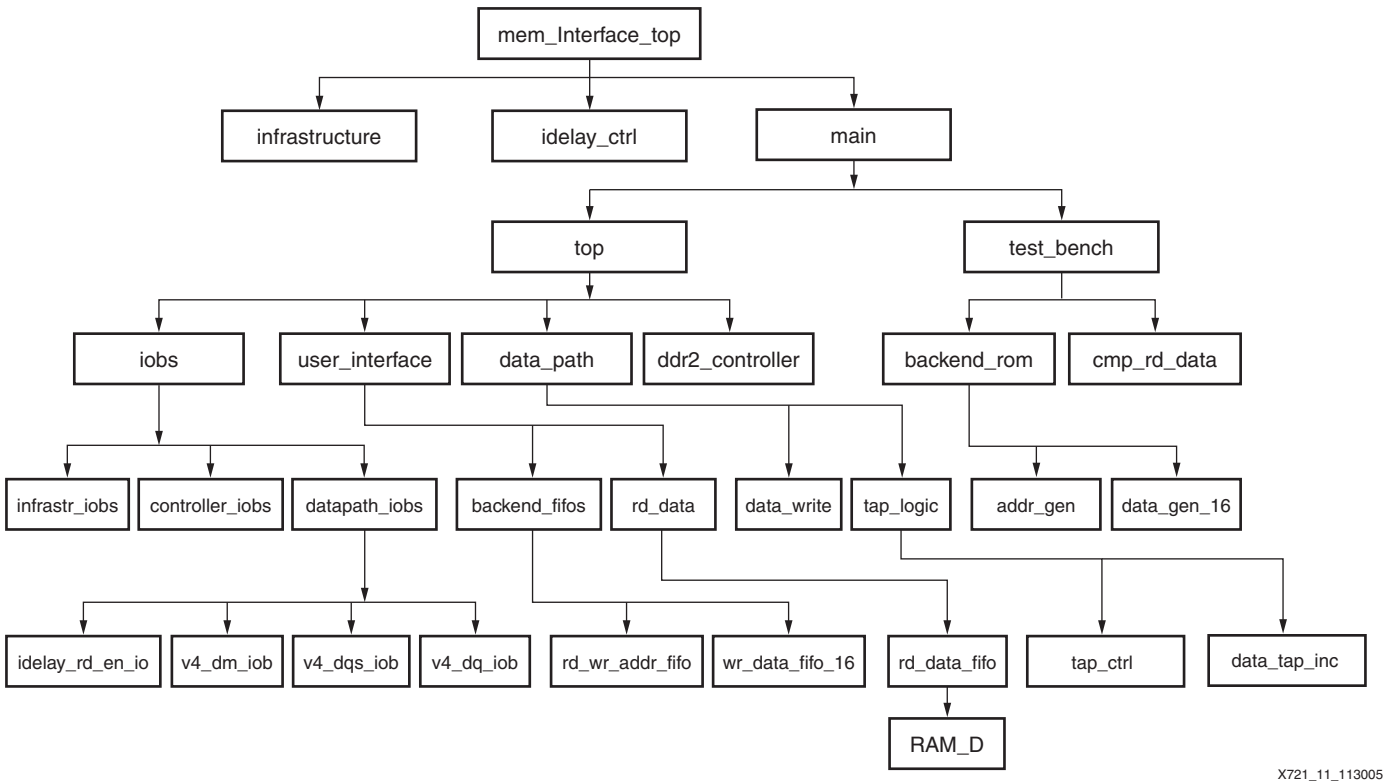

Figure 12: **Reference Design Hierarchy**

Reference Design Summary

Table 5 lists the maximum frequency by speed grade for a 72-bit interface.

Table 5: **Maximum Frequency by Speed Grade for a 72-Bit Interface**

Speed Grade	Maximum Frequency by Speed Grade (MHz)
-10	230
-11	267
-12	300

Table 6 lists the reference design summary for a 72-bit interface.

Table 6: **Reference Design Summary for a 72-Bit Interface**

Parameters for Design Details	Design Details / Notes
Device Utilization	6,714 slices. Includes the controller, synthesizable testbench, the user interface, and the physical layer.
	6 BUFGs. Includes one BUFG for the 200 MHz reference clock for the IDELAY block.
	9 BUFIOs. Equals the number of strobes in the interface.
	1 DCM
	1 PMCD
	72 ISERDES. Equals the number of data bits in the interface.
	99 OSERDES. Equals the sum of the data bits, strobes, and data mask bits.

Conclusion

This application note explains a technique for using ISERDES to capture data for high-performance memory interfaces. This design provides a high margin because the logic in the FPGA fabric (excluding the calibration logic) is clocked at half the frequency of the interface, eliminating critical paths.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/15/05	1.0	Initial Xilinx release.
12/20/05	1.1	Updated Table 1.
01/04/06	1.2	Updated link to reference design file.
02/02/06	1.3	Updated Table 4.
05/25/06	1.4	Updated “Clocking Scheme ,” “Read Datapath,” and “Per Bit Deskew Data Capture Technique,” sections, Figure 1, Figure 7, Table 3, and Table 6. Also updated the link to the reference design file.

Date	Version	Revision
03/12/07	2.0	• Revised "Summary." • Revised "Introduction." • Revised "Clocking Scheme " text and Figure 1. • Revised "Write Timing Analysis" text and Table 1. • Revised Table 2. • Revised "Read Datapath" text and Figure 7. • Revised "Read Timing Analysis" and Table 3. • Revised "Per Bit Deskew Data Capture Technique" text and Figure 8. • Added new Figure 9 and explanatory text. Renumbered remaining figures. • Old Figure 9 replaced with new figure, Figure 10. • Old Figure 10 replaced with new figure, Figure 11. • Old Figure 11 renumbered to Figure 12. • Retitled old section "Reference Design Utilization" to "Reference Design Summary." • Retitled old Table 6 from "Resource Utilization for a 64-Bit Interface" to "Reference Design Summary for a 72-Bit Interface." Revised text in Table 6. • Revised "Conclusion."
10/12/07	2.1	• Figure 6: Corrected clock phase relationship between CLKdiv_0 and CLKdiv_180.
07/29/09	2.2	• Revised headings in Table 1 to include picoseconds (ps) unit of measure in columns 2, 3, and 4.