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PowerPC 405 Clock Macro for -7(C) and -6(I) Speed Grade Dual-Processor Devices

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Summary

The embedded PowerPC™ 405 processor blocks in Virtex-II Pro™ devices with -7 speed grades can achieve speeds to 400 MHz, and -6 speed grades can achieve speeds to 350 MHz. Special considerations are necessary when using the left processor in dual-processor devices. This application note describes these considerations and provides a necessary macro when operating the left processor at speeds greater than 350 MHz in the -7 commercial speed grade devices and greater than 300 MHz in the -6 industrial speed grade devices.

Note that clock macros are *not* required for the -6 commercial speed grade devices.

Introduction

The following Virtex-II Pro devices in the -7 commercial and -6 industrial speed grades contain two PowerPC 405 embedded processor blocks:

- 2VP20
- 2VP30
- 2VP40
- 2VP50
- 2VP70
- 2VP100

The 2VP100 device is not available in a -7 commercial speed grade.

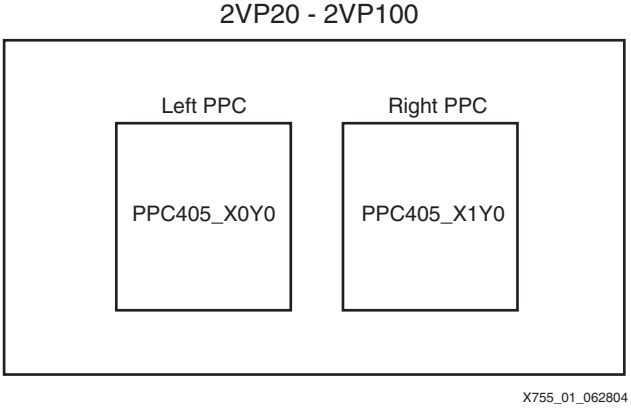

Figure 1: **Left and Right Processors**

The Virtex-II Pro Platform FPGA data sheet (DS083) specifies that the maximum CPMC405CLOCK operating frequency for -7 and -6 speed grade devices is 400 MHz and 350 MHz, respectively. Table 1 lists the AC characteristics for the processor clocks. It assumes a high-quality clock input, such as from a DCM output or onboard oscillator. Table 1 is taken from the Virtex-II Pro data sheet.

Table 1: **Absolute AC Characteristics for Virtex-II Pro Processor Clocks**

Description	Speed Grade						Units
	-7		-6		-5		
	Min	Max	Min	Max	Min	Max	
CPMC405CLOCK frequency	0	**400**	0	**350**	0	300	MHz
JTAGC405TCK frequency(1)	0	200	0	175	0	150	MHz
PLBCLK frequency(2)	0	400	0	350	0	300	MHz
BRAMDSOCMCLK frequency(2)	0	400	0	350	0	300	MHz
BRAMISOCMCLK frequency(2)	0	400	0	350	0	300	MHz

Notes:

1. The theoretical maximum frequency of this clock is one-half the CPMC405CLOCK. However, the achievable maximum is dependent on the system and is much less.
2. The theoretical maximum frequency of these clocks is equal to the CPMC405CLOCK. However, the achievable maximum is dependent on the system. Refer to *PowerPC 405 Processor Block Reference Guide* and XAPP640 for more information.

For the devices listed in the bulleted list above, the left PowerPC block requires special implementation guidelines to achieve speeds greater than 350 MHz or 300 MHz, for -7 and -6 speed grade devices, respectively. There are slight differences between the right and left processor blocks. Designs that do not use the PLB interface, such as OCM-only designs, are not required to use this macro.

Xilinx provides a special macro in EDIF netlist format, which can be inserted into the clock path of a design utilizing the left processor at rates faster than 350/300 MHz for the -7C or -6I speed grade devices. The full set of conditions under which this macro should be used are listed below:

- Devices: 2VP20, 2VP30, 2VP40, 2VP50, 2VP70, and 2VP100

  The 2VP100 is not available in a -7 speed grade.
- Speed grades: -7C (commercial) and -6I (industrial)
- Left processor utilized

  Single processor designs should use the right processor.
- CPMC405CLOCK:

  - Greater than 350 MHz for -7 commercial grade devices.

  - Greater than 300 MHz for -6 industrial grade devices.

  - Note that -7 industrial grade devices are not available.
- The Processor Local Bus (PLB) or the On-Chip Peripheral Bus (OPB) is utilized.

Implementation Guidelines

To use the provided macros, the guidelines in this section must be followed. In addition to these guidelines, several use models are given to show how the macro(s) can be used successfully.

EDK Usage

When using EDK, the clock module should be built separately from the system. The EDK project can be imported into the ISE design flow, which contains the clocking circuits. Alternatively, the user can generate a custom PCORE, which contains this clocking circuitry.

Macro Placement

The placement of the macro must be between the digital clock manager (DCM) and the global clock buffers (BUFGs). Figure 2 gives an example of this placement.

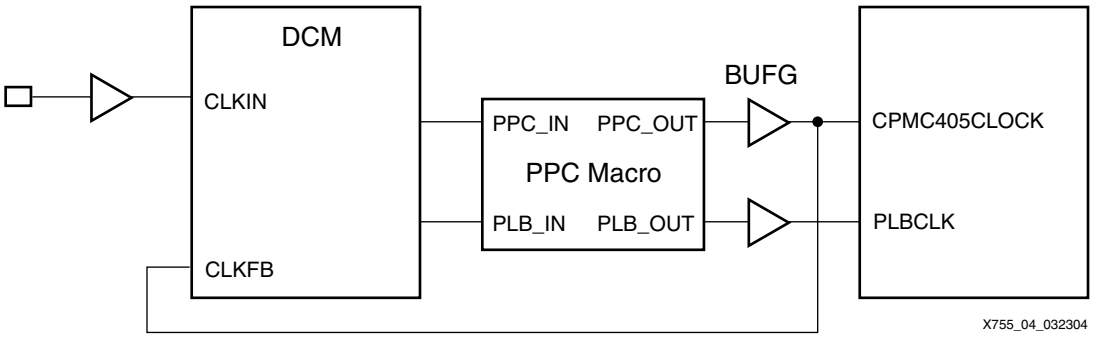

Figure 2: **Macro Usage Example**

DCM Placement

Only certain DCMs can be used with the macros. Table 2 shows which DCMs must be used in certain devices.

Table 2: **DCMs to Use With Virtex-II Pro Devices**

Device	DCM
2VP20	X0Y1
2VP30	X0Y1
2VP40	X1Y1
2VP50	X0Y1
2VP70	X1Y1
2VP100	X4Y1

The DCMs can be LOC'ed in the UCF file or embedded in the HDL code. Refer to the "Constraint Requirements" section for an example of the LOC attribute in the UCF.

GCLK Pin Usage

Because the DCM specified in each device is located on the top of the chip, it is recommended to bring the clock in on the same side of the chip. Specifically, these are the GCLK pins located in Banks 0 and 1. Please see the Virtex-II Pro Pinout Tables in Module 4 of the Virtex-II Pro Platform FPGA data sheet (DS083) for the specific pin number.

DCM Clock Outputs

Only two output clocks from the DCM are recommended for use with these macros. If a third clock needs to be phase-aligned, a second DCM is needed to provide this clock. In most cases it is necessary to use a 200 MHz oscillator as the input clock. Figure 3 and Figure 4 provide example circuits that Xilinx recommends for these macros.

Note: CLKFX cannot be used to generate CPMC405CLOCK because the maximum CLKFX frequency for -7 speed grade devices is 320 MHz.

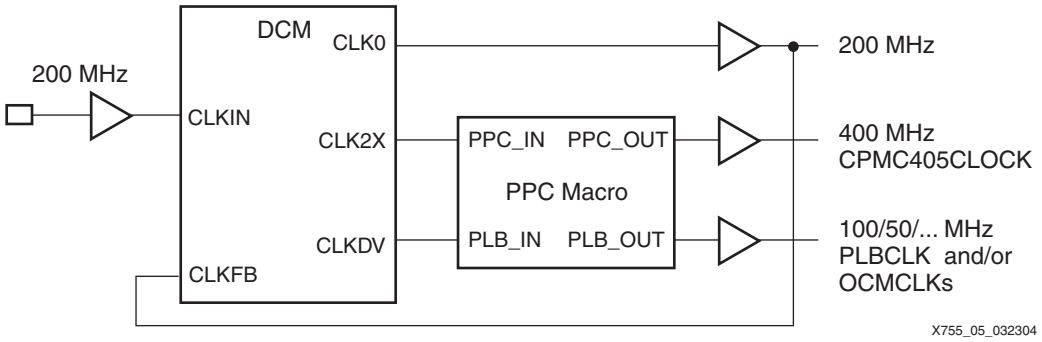

Figure 3: **Example Circuit 1**

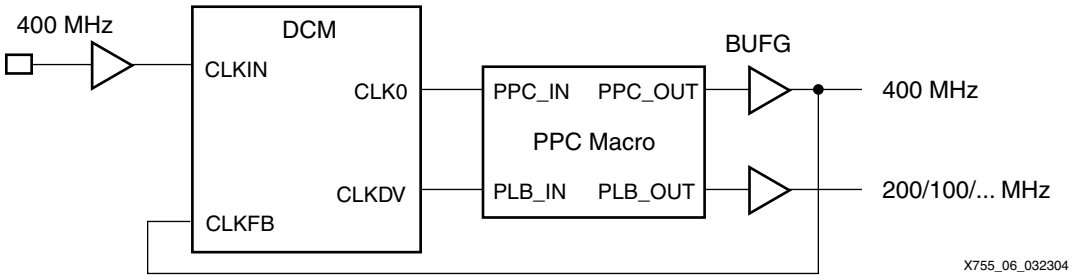

Figure 4: **Example Circuit 2**

Constraint Requirements

This section lists the constraint requirements that are mandatory for using the EDIF macros successfully. The DCM, BUFGs, and PPC405 must be LOC'ed in the UCF file or embedded in the HDL code. It is also necessary to place MAXDELAY constraints of 0.45 ns on the net from the DCM to the macro. A MAXDELAY constraint of 0.755 ns is necessary for the nets between the macro and the BUFGMUX.

On rare occasions, place and route (PAR) issues an error on the MAXDELAY timing constraints. This situation might occur due to congested routing on the routes near the BUFGMUXs, for instance, if several macros are all used on the same side of the chip. There are two simple workarounds for this situation:

1. Change the pin on the BUFGMUX, that is, I0 --> I1
2. Choose another BUFGMUX location

Here is an example of a UCF file syntax with these constraints:

```
################################
##### DCM CONSTRAINTS ####
################################
# Note: must place location constraint on the DCM(s) with left PowerPC
solutions.
INST powerpc405_dcm LOC=DCM_X0Y1;

# Note: select 2 of 8 BUFGMUXs to go with DCM location on TOP of chip
INST bufg0 LOC=BUFGMUX7P;
INST bufg1 LOC=BUFGMUX6S;

#Note: LOC the left PowerPC 405
INST powerpc405_instance LOC=PPC405_X0Y0;

# Place maximum delay specifications on the Macro input/output routes.
# Macro input nets(DCM to macro input):
net "cpmc405clock_i" MAXDELAY = 0.450 NS;
net "plbclk_i" MAXDELAY = 0.450 NS;

# Macro output nets(macro to BUFG):
net "cpmc405clock_o" MAXDELAY = 0.755 NS;
net "plbclk_o" MAXDELAY = 0.755 NS;
```

Reference Design

The reference design files are located at http://www.xilinx.com/bvdocs/appnotes/xapp755.zip.

Conclusion

The left processor in Virtex-II Pro -7 commercial speed grade, dual-processor devices requires a special macro to operate at speeds greater than 350 MHz. The left processor in Virtex-II Pro -6 industrial speed grade, dual-processor devices requires a special macro to operate at speeds greater than 300 MHz. This application note provides this macro, describes the conditions under which it is necessary, and provides guidelines for implementing the macro.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/05/04	1.0	Initial Xilinx release.
06/28/04	1.1	Added information pertaining to devices that are available in -7 commercial and -6 industrial speed grades.
02/08/06	1.2	Added DCM location data to Table 2 for XC2VP100 device.