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Transmitting DDR Data Between LVDS and RocketIO CML Devices

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Summary

The serial transfer of data between devices on a board or cards on a backplane using the LVDS differential standard is well established. Existing cards need to be able to interface to newer technologies. This application note discusses two possible ways to interconnect standard LVDS transceivers with the Current Mode Logic (CML) technology used in Xilinx RocketIO™ multi-gigabit transceivers (MGTs) through AC coupling and DC coupling.

Introduction

This application note discusses the transmission between LVDS-based and CML-based interfaces. Analog example simulations show the principal interoperability between those two kinds of devices. Additionally, a design transmitting data from LVDS to CML using Xilinx technology is available.

AC-Coupled Data Transmission

For data transmission between two transceivers where the differential voltage matches but the common mode voltage does not, AC coupling is usually used. This is accomplished by putting a capacitor in series into the signal path. Because no galvanic connection exists between sender and receiver, the transmitted signal must be DC-balanced, meaning the number of transmitted ones and zeros must be equal over time. The 8B10B coding scheme used in many high-speed transmission protocols guarantees this DC balance and avoids charging or discharging the transmission line.

Choosing the correct value for the AC coupling depends on the maximum run length occurring in a chosen protocol and the data-dependent jitter caused by discharge effects. Generally, a 10 nF capacitor is appropriate for run lengths of 40 consecutive non-changing bits at data rates of several 100 Mbits/sec.

For a good explanation of the calculations necessary in choosing the correct value of the AC capacitor, refer to Maxim's application note HFAN-1.1: "Choosing AC-Coupling Capacitors".

DC-Coupled Data Transmission

For data transmission between devices that are fully electrically compliant (the common mode voltage and the differential voltage match), DC-coupled transmission is preferable. In this case, the two transceivers are directly connected without any galvanic interruption.

For DC-coupled transmission to work, the following requirements must be met:

- The LVDS driver must see a 100Ω differential termination.
- The LVDS receiver must have a common mode voltage of typically 1.25V and a voltage swing between 100 mV and 350 mV.

100 Ohm Termination Voltage for the LVDS Transmitter

The CML receiver in the RocketIO MGT has a simplified circuit shown in Figure 1. Each of the two differential transmission lines is internally terminated via an adjustable terminator (50Ω / 75Ω) against the termination voltage VTRX (typically set to 1.8V). Leaving VTRX unconnected

on the FPGA results in a resistance of 100Ω between RXP and RXN (150Ω with a 75Ω termination). So setting the termination on the RocketIO transceiver to 50Ω via the attribute TERMINATION_IMP=50 and leaving VTRX unconnected generates the necessary termination for the LVDS driver.
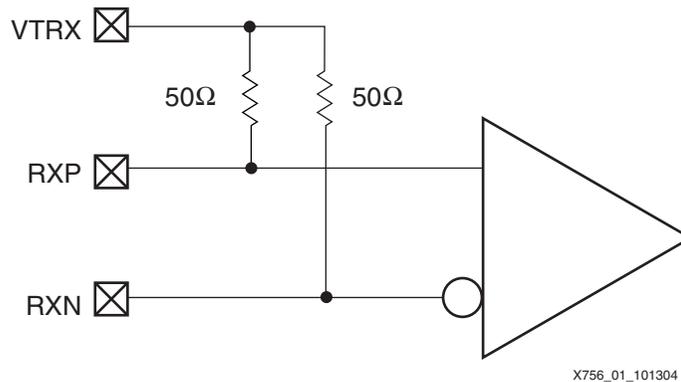

Figure 1: **Simplified CML Input Circuit**

Common Mode Voltage for LVDS Receiver

The CML output driver has a simplified circuit as shown in Figure 2. VTTX is typically set to 2.5V and generates a common mode voltage of approximately 1.5V. The common mode voltage can be lowered to standard LVDS level by decreasing the voltage on VTTX. Through HSPICE simulation, a value of 1.8V for VTTX was determined to be suitable.
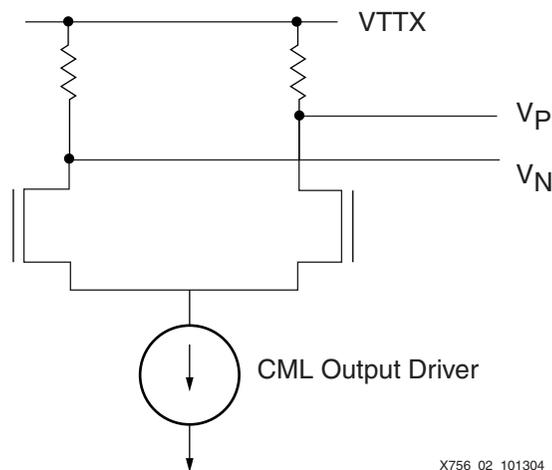

Figure 2: **Simplified CML Output Circuit**

HSPICE Simulation of RocketIO Transceiver to LVDS (DC-Coupled)

The suggested circuits for DC-coupled transmission are simulated with a setup as shown in Figure 3 and Figure 11.

To rerun the simulation yourself, you need to download the HSPICE models for the RocketIO driver and the LVDS pins from the SPICE suite. The appropriate wrappers and topologies are located in the `simulation` directory in xapp756.zip. For the transmission line, a 12 mil wide stripline on FR4 is chosen. The HSPICE model for this is found in the signal integrity kit in the SPICE Suite. For the RocketIO transceiver to LVDS transmission, a distance of 2 cm is assumed between the LVDS pins on the FPGA and the termination resistor.
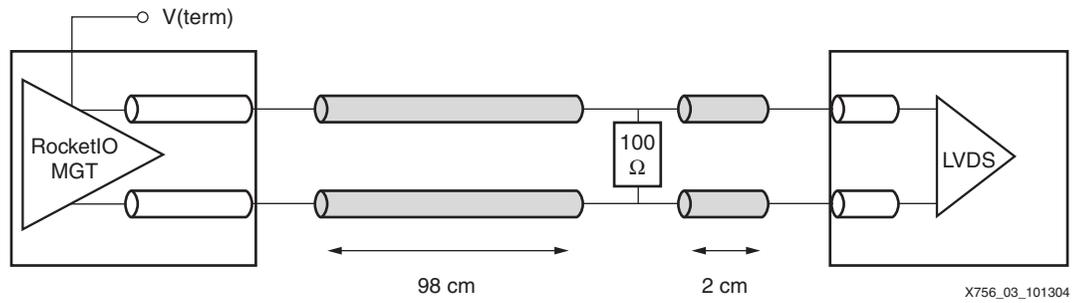
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*Figure 3:* **Topology for DC-Coupled Transmission (CML to LVDS)**

Several simulations have been performed for this setup using HSPICE 2003.03.

The first simulation uses a pulse response to find the worst-case eye pattern for a 500 mV swing with 10% pre-emphasis. By placing cursors on the resulting waveform and overlaying, a worst-case bit pattern of 110100000000010 has been found, which creates the worst-case eye diagram (see Figure 4).
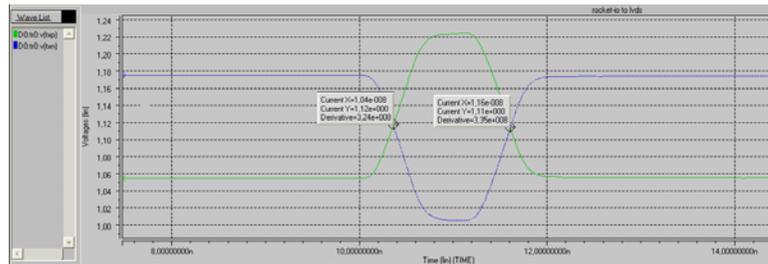
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Figure 4: **Stimulus for Pulse Response**
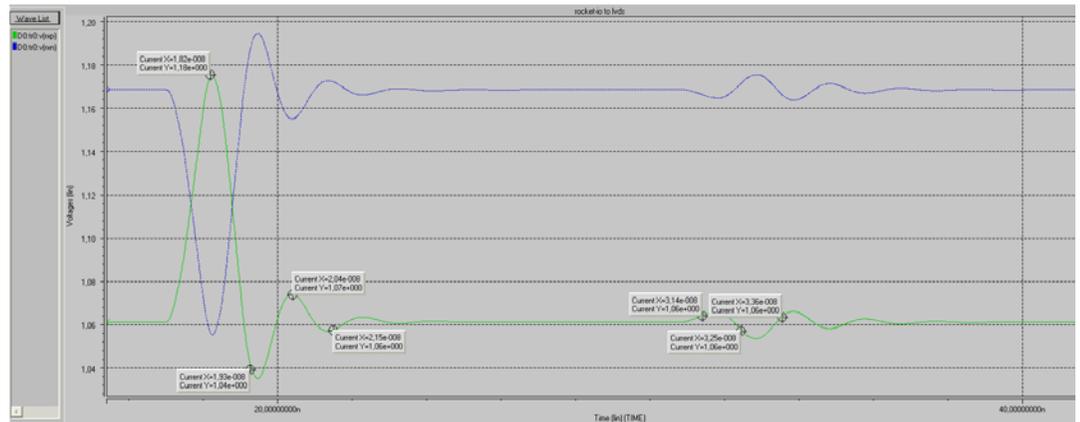
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Figure 5: **Result of the Pulse Response at the LVDS Receiver**

To get the worst-case eye diagram, the pulses must overlap in a way to minimize the interior of the eye. To find the necessary bit pattern to achieve this, the pulse response has to be added multiple times onto itself so that the initial pulse is minimized. Shifting the pulse by one bit period to the right brings the logic level 1 pulse into the middle of reflection's ditch. Shifting the response by another bit does not decrease the size of the eye center. So the pulse is shifted multiple times until no significant dip in the response is seen anymore. If during shifting the initial logic level 1 pulse falls into one of the ditches caused by reflections, a '1' is added to the bit pattern, otherwise a '0' is added.

Applying this method results in the bit pattern of 110100000000010, which is transmitted into the line. This pattern closes the eye from the bottom. To also close the eye from the top, the bit pattern is inverted and transmitted afterwards, leading to the eye diagram shown in Figure 6.
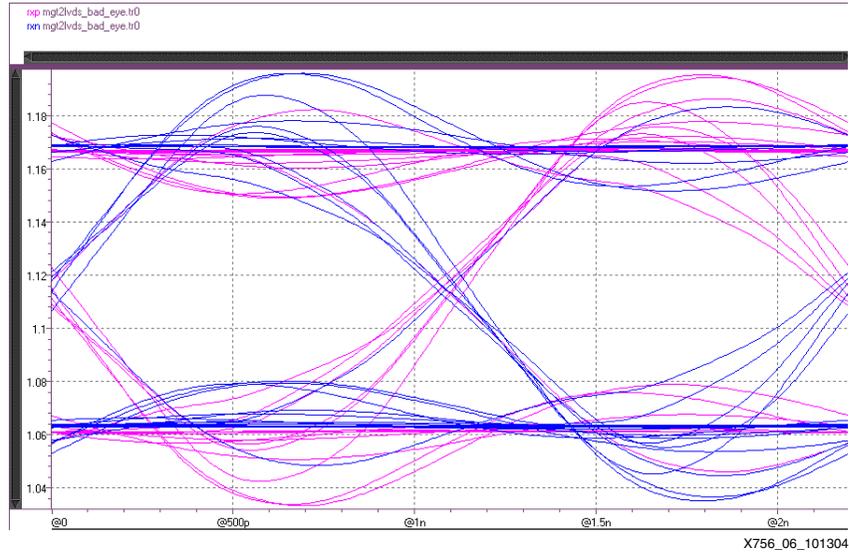

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Figure 6: **Worst-Case Eye Diagram for Given System**

Even though the eye is worst case, the bit pattern is still properly received as shown in Figure 7.
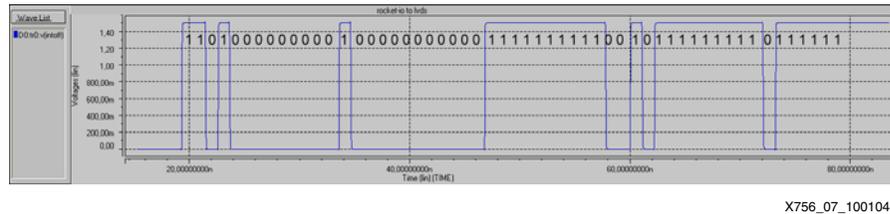

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Figure 7: **Worst-Case Bit Pattern after the RocketIO Transceiver**

Virtex-II Pro™ devices also feature a differential internal termination of 100Ω for LVDS. Using this feature simplifies the traces from a layout perspective and also improves the impedance matching with less impedance discontinuities.

Simulating a system as shown in Figure 8 results in an improved eye at the receiving device.
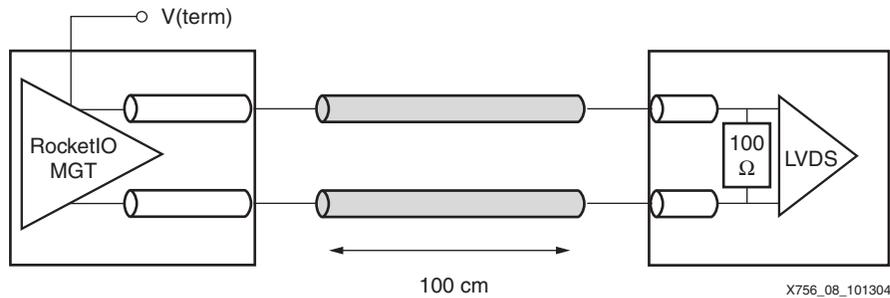

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Figure 8: **Topology for DC-Coupled Transmission (CML to LVDS_DT)**

The pulse response and resulting eye diagram for the CML to LVDS_DT example are shown in Figure 9 and Figure 10, respectively.

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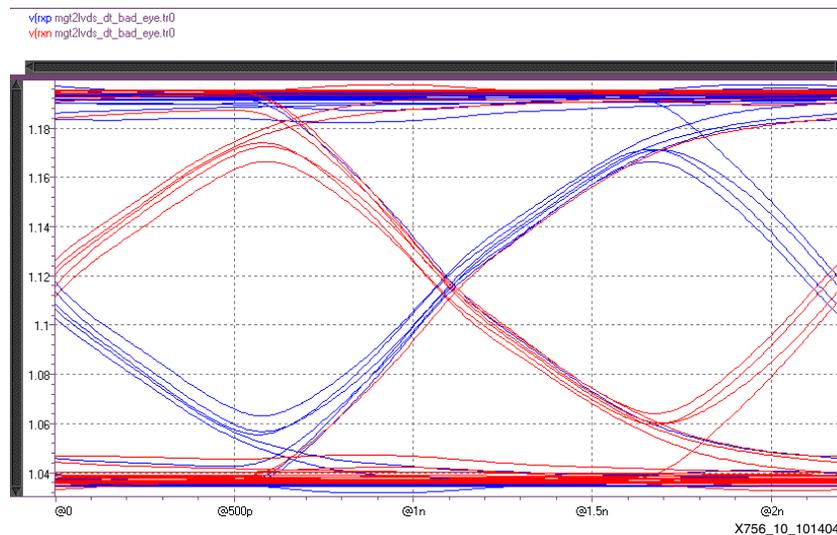*Figure 9:* **Pulse Response for Example CML to LVDS_DT**

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Figure 10: **Resulting Eye Diagram**

Comparing the results clearly shows the advantage of the internal LVDS_DT (differential termination) for systems like this.

Similar simulations have been performed on LVDS driving the RocketIO transceiver. For this simulation the termination is inside the RocketIO transceiver. Hence there are no external components. The topology (as shown in Figure 11) is simpler and has fewer impedance discontinuities that decrease the signal quality.
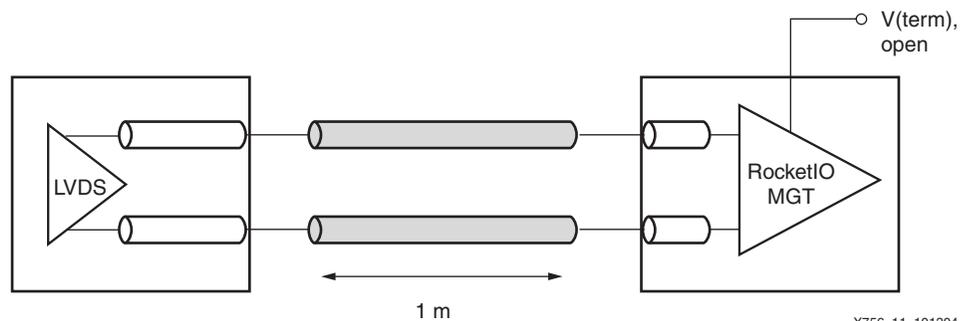
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Figure 11: **Topology for DC-Coupled Transmission (LVDS to CML)**

The result of the pulse response (Figure 12) for the LVDS to CML topology shows the benefit of the internal termination. Few reflections occur anymore.
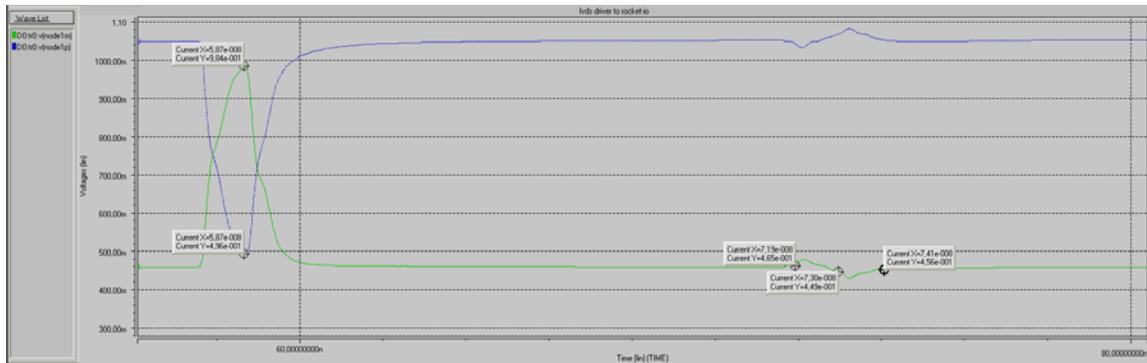

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Figure 12: **Pulse Response for Example CML to LVDS Circuit**

Looking at the positions when the reflection occurs, the resulting bit pattern for the worst-case eye pattern is 100000000000011, which results in edges in the transmitted signal right at the reflections. This bit pattern is changed to 100000100000011 to get more edges in the datastream.
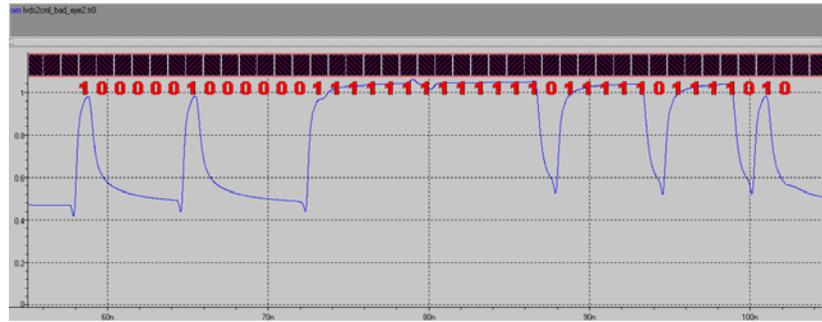
The resulting eye is shown in Figure 13. Comparing it to the eye diagram with the external termination in Figure 6 shows a big improvement in its quality.
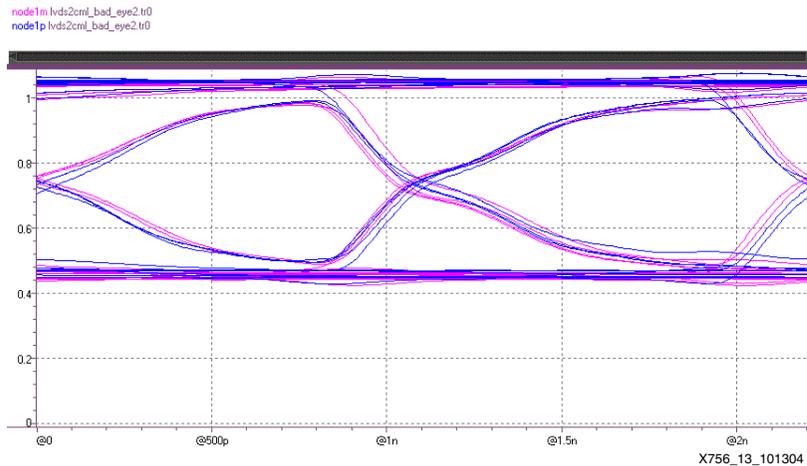
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Figure 13: **Resulting Worst-Case Eye Diagram**

The data is received correctly, as shown in Figure 14.

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Figure 14: **Resulting Worst-Case Bit Pattern after the LVDS Transceiver**

Conclusion

The discussed circuits allow AC- and DC-coupled transmission of data between the LVDS and the CML circuits used in the Virtex-II Pro devices at speeds down to 640 Mbits/sec.

The designs described in the appendices have been created to prove the concept in hardware. The target boards for those designs are the ML321 Evaluation Board for the RocketIO design and the XLVDSPro Demonstration Board for LVDS.

Appendix A: LVDS TX Design

The LVDS design consists of two main parts, data generation and serialization.

Data generation runs at a slower system clock of 64 MHz and generates an 8-bit wide PRBS pattern. This pattern goes into a 8B10B encoder, generated with the CORE Generator™ system.

Every 64 clock cycles, a comma character is inserted into this PRBS pattern and encoded as a K character. The 10-bit output of the encoder is fed into the second main block, the LVDS_10:1 block, and is then transmitted out of the FPGA.
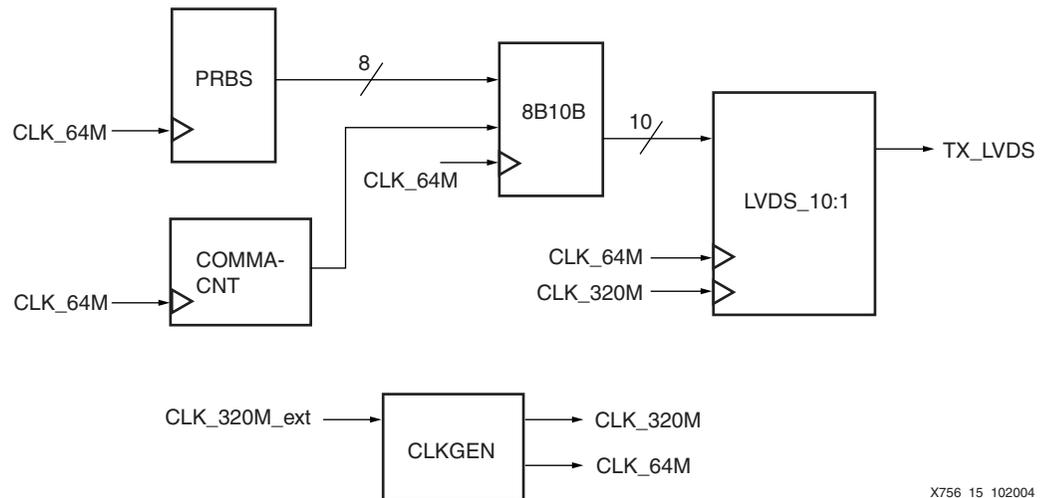
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Figure 15: **Block Diagram for LVDS TX System**

The 10:1 serializer takes in 10-bit wide data at the 64 MHz system clock, splits the data into two 5-bit sections, and transfers this data into the 320 MHz domain. A 3-bit counter in each path generates the select signal for a 5:1 MUX. This MUX is built in three stages: the first stage out of LUTs, a MUXF5 between those two LUTs, and a MUXF6 for the fifth bit. Figure 16 shows a block diagram for this serializer.
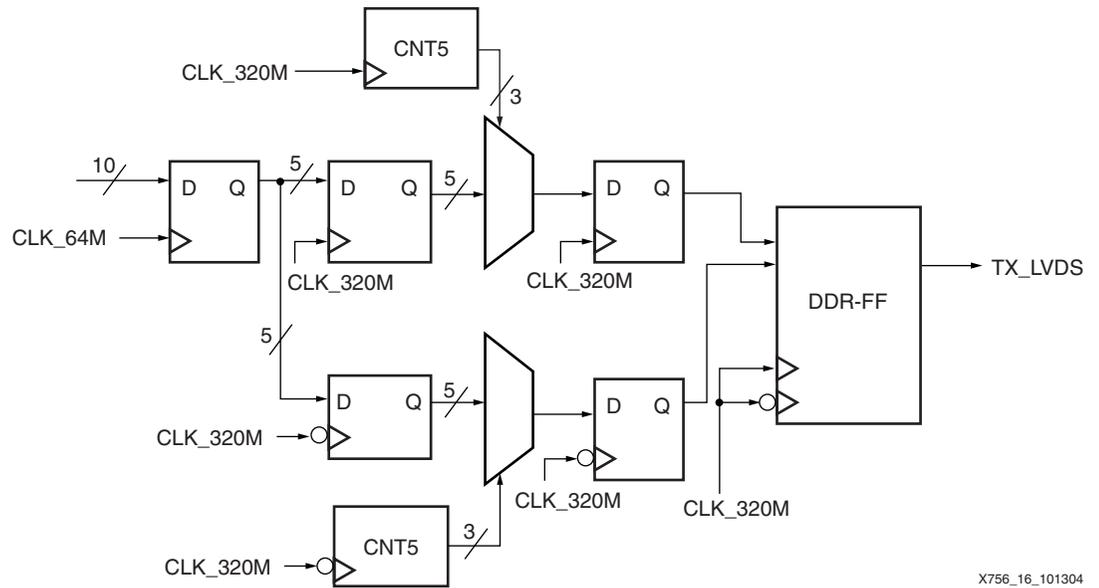
Figure 16: **Block Diagram for 10:1 Serializer**

Appendix B: RocketIO Design

The RocketIO design (see Figure 17) is a simple feasibility design. It works on the recovered clock for the RX side using a digital clock manager (DCM). For production designs, you are advised to not directly use the RXRECCLK with a DCM, but to either clean it up with an external PLL or have a protocol that utilizes clock correction.
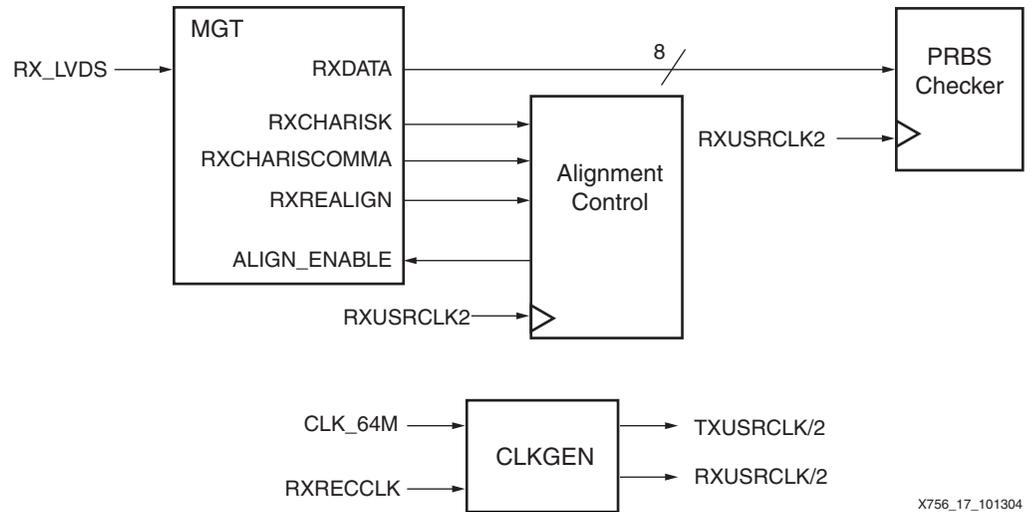

Figure 17: **RocketIO Block Diagram**

The design checks for detected commas in the received datastream. Once a comma is detected, a state machine checks for three additional commas that are 64 words apart. As soon as those commas are found, the link is considered aligned and the incoming data is checked against bit errors. If errors are found, a counter is incremented and displays its value on the board.

The TX side is very similar to the LVDS design. The PRBS generator and comma-count logic are identical. However, for 8B10B encoding and serialization, the dedicated functions of the RocketIO transceiver are used. Because the receiving SelectIO inputs do not have the capability of recovering a clock embedded in the datastream, an additional RocketIO transceiver is used to transmit a constant 1-0 pattern as a source-synchronous clock.

Appendix C: LVDS RX Design

For the LVDS inputs to receive the data correctly the source-synchronous clock must initially be aligned into the middle of the incoming data eye. The reference design in XAPP268 is used for this function.

When the clock-data alignment is finished, the data is deserialized in the circuit shown in Figure 18. Initially the data is split up into one path for the data received on the positive clock edge and a second one for the negative clock edge. Only the positive path is shown for simplicity. A one-shot encoded enable circles a pulse of one clock-cycle length that enables the flip-flops for the serial-parallel conversion. This converted data is stored in ten flip-flops. Every five clock cycles either the five top or bottom flip-flops are read out, controlled by a second one-shot encoded read enable.
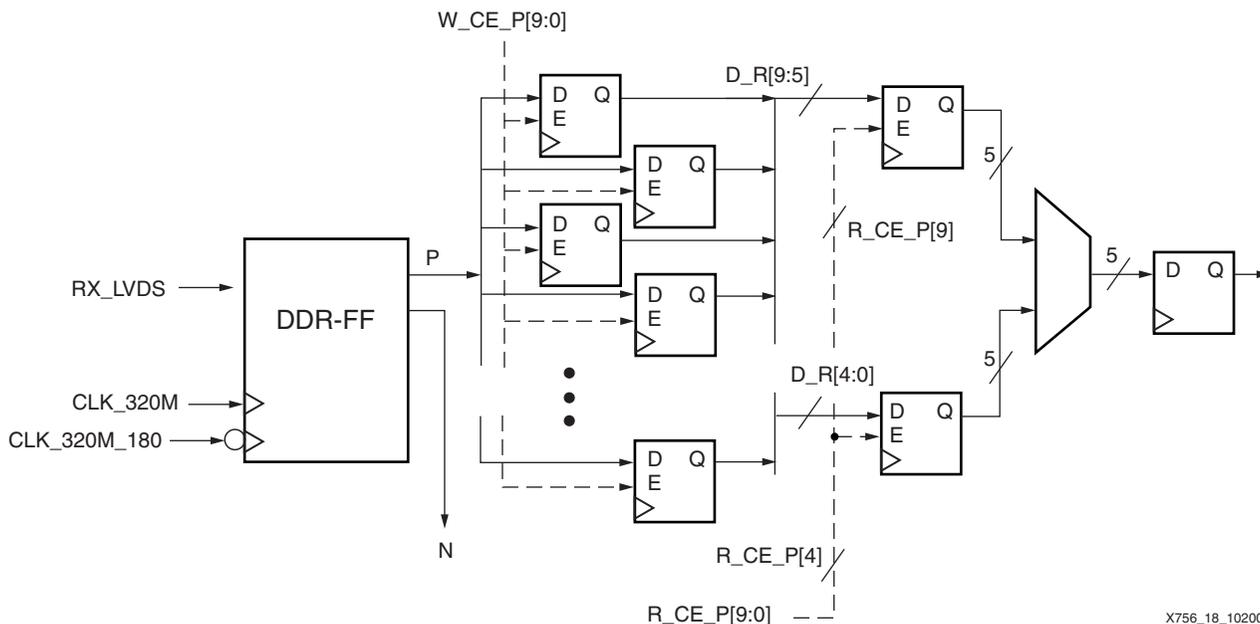

Figure 18: **LVDS Deserializer**

Writing and reading takes place in opposite halves of this serial-in, parallel-out (SIPO) circuit, hence no data corruption can happen. The read data is MUXed together and then presented to the rest of the design.

After the deserializer, the data is comma-aligned and then checked as in the MGT design.

Appendix D: Hardware and Configuration

The boards used for LVDS and RocketIO MGT transmission are listed below:

- LVDS Transmission

  Xilinx XLVDSPro demonstration board with XC2VP20-FF896

- MGT Transmission

  Xilinx ML321 evaluation board with Virtex-II Pro XC2VP7-FF672

All designs were done in VHDL, simulated with Modelsim 5.8D, synthesized using XST, and implemented using ISE 6.2i SP3.

Table 1 and Table 2 provide the design sizes for the LVDS transceiver and MGT transceiver, respectively.

Table 1: **LVDS Transceiver (XC2VP20)**

Parameter	Total Number	Percent
Occupied slices	462 out of 9,280	4%
MULT18X18s	1 out of 88	1%
GCLKs	5 out of 16	31%
DCMs	2 out of 8	25%

Table 2: **MGT Transceiver (XC2VP7)**

Parameter	Total Number	Percent
Occupied slices	72 out of 4,928	1%
GCLKs	5 out of 16	31%
DCMs	2 out of 4	50%
GTs	2 out of 8	25%

The reference design uses standard SMA connectors. It uses a 50Ω SMA cable manufactured by Florida RS Technology.

The voltages for the reference are:

- DC-coupled
  - VTRX = open
  - VTTX = 1.8V
- AC-coupled
  - VTRX = 1.8V
  - VTTX = 2.5V

References

The following documents provide additional information relevant to this application note:

- Xilinx XAPP230: "The LVDS I/O Standard"
- Xilinx XAPP268: "Active Phase Alignment"
- Xilinx UG024: *RocketIO Transceiver User Guide*
- HFAN-1.1: "Choosing AC-Coupling Capacitors"

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/04/04	1.0	Initial Xilinx release.