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## Local Clocking for MGT RXRECCLK in Virtex-II Pro Devices

Author: Matt Dipaolo and Lyman Lewis

### Summary

This application note describes the local clocking resources available in the Virtex-II Pro™ architecture for the RXRECCLK of 3.125 Gb/s RocketIO™ multi-gigabit transceivers (MGTs). Using RXRECCLK with local clock routing can enable applications to bypass the MGT's elastic buffer, thus reducing latency without consuming global clock resources. Along with a reference design, this application note explains how to use the local clocking resources.

### Introduction

For the Virtex-II Pro device, it is recommended that the RX elastic buffer never be bypassed. This recommendation is based on the uncertain phase relationship between the RXRECCLK and RXUSRCLK or RXUSRCLK2 inside the MGT, when RXUSRCLK and RXUSRCLK2 are derived from RXRECCLK in the fabric. This relationship could cause setup/hold issues at certain process, voltage, and temperature (PVT) corners. The local clocks discussed in this application note create a known phase relationship over PVT, which ensures that all setup/hold values are met.

These local clocks also allow users to save a BUFG. This becomes significant in designs containing large numbers of MGTS (in some cases, 16-20), where having a BUFG for each RXRECCLK is not practical. Bypassing the RX FIFO and crossing the clock domains in the fabric with a FIFO in the fabric (using either block RAMs or distributed RAM) reduce the latency from approximately 18 USRCLKs to approximately 3 or 4 (depending on the design of the FIFO).

For specific information on Local clocking resources, refer to [XAPP609](#) (*Local Clocking Resources in Virtex-II™ Devices*).

### Design

The MGT local clock route is a 5 x 12 Configurable Logic Block (CLB) array on the top of the device and a 5 x 11 CLB array on the bottom.

The top loads the five columns to the left of the MGT and down 12 rows of CLBs. This allows 480 flip-flops plus two block SelectRAMs below the MGT included in this clock domain. [Figure 1](#) shows this configuration.

The bottom loads the five columns to the left of the MGT and up 11 rows of CLBs. This allows 440 flip-flops plus two block SelectRAMs above the MGT included in this clock domain.

The block RAMs can be used to cross the RXRECCLK domain to another clock domain, which the user logic utilizes for the protocol MAC or other high-level circuitry.

The local clock routes are automatically routed when the array coordinates are defined. See the *Constraints* section for the 3.125 Gb/s capable Virtex-II Pro devices (XC2VP2, XC2VP4, XC2VP7, XC2VP20, XC2VP30, XC2VP40, XC2VP50, XC2VP70, and XC2VP100).

Saving a BUFG can occur when the RXUSRCLK/RXUSRCLK2 are driven by the RXRECCLK. The local clock route removes the need to distribute the clock with global clocking resources, including a BUFG.

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## Constraints

Several constraints are used to define the array coordinates. First, it is not recommended to use MAXDELAY and MAXSKEW, because the implementation tools might try to satisfy an unrealistic MAXDELAY or MAXSKEW constraint, thus causing the routes to jump off the local clock routes.

The following UCF snippet shows an example of defining an AREA\_GROUP for one local clock route for all the synchronous elements. Because the block RAM is not included in the AREA\_GROUP, a location constraint needs to be added for the block RAMs.

```
NET                "clk_i" TNM_NET = "clk";
TIMESPEC          "TS_clk" = PERIOD "clk" 8 ns HIGH 50%;
TIMEGRP          "clk" AREA_GROUP = "LOCAL_CLK";
AREA_GROUP "LOCAL_CLK" RANGE = SLICE_X6Y88:SLICE_X15Y111;
```

Here are a few example block RAM location constraints to go with this area constraint:

```
INST "FIFO/B7" LOC = RAMB16_X1Y12;
INST "FIFO/B8" LOC = RAMB16_X1Y11;
```

## Array Examples

Several applications exist where the RX elastic buffer of the MGT must be bypassed, such as reducing latency or implementing different types of clock correction or channel bonding techniques. Bypassing the RX elastic buffer creates a clock domain crossing, requiring the RXRECCLK to clock the MGT's RX fabric interface and CRC logic via connections from the RXRECCLK to RXUSRCLK and RXUSRCLK2 in the fabric. If the resulting phase relationship between the RXRECCLK and RXUSRCLK or RXUSRCLK2 inside the MGT is not correct, there is a potential for setup and hold errors. However, the user of local clock routes for RXRECCLK can provide a consistent skew and delay over PVT. These routes have been proven to run at 125 MHz on hardware with 16 MGTs all running their own independent local clock. [Figure 1](#) shows this local clock for a top MGT.

[Table 1](#) and [Table 2](#) show the estimated delays for a fully populated array using speed file version 1.84 for these local routes.

**Table 1: Estimated Delays of the RXRECCLK<sup>(1)</sup> (Top)**

Speed Grade	IOB_REG	IOB_O_REG	BRAM/Multiplier	CLB_REG	MGT RXUSRCLK
-5	1.547 - 1.559	1.557 - 1.569	1.662 - 1.630	1.660 - 1.729	2.165
-6	1.385 - 1.400	1.395 - 1.405	1.455 - 1.485	1.480 - 1.540	1.950
-7	1.270 - 1.275	1.275 - 1.280	1.310 - 1.335	1.345 - 1.390	1.780

**Notes:**

1. Best/worst case for a given route.

**Table 2: Estimated Delays of the RXRECCLK<sup>(1)</sup> (Bottom)**

Speed Grade	IOB_REG	IOB_O_REG	BRAM/Multiplier	CLB_REG	MGT RXUSRCLK
-5	1.551 - 1.564	1.694 - 1.697	1.615 - 1.657	1.625 - 1.694	2.330
-6	1.390 - 1.405	1.500 - 1.515	1.440 - 1.480	1.450 - 1.515	2.090
-7	1.265 - 1.270	1.350 - 1.355	1.300 - 1.330	1.305 - 1.350	1.890

**Notes:**

1. Best/worst case for a given route.

Another consideration is the internal path delays of the MGT itself to complete the timing analysis. An analysis of the setup/hold and signal delays was calculated. All of these delays were taken into consideration, as well as delay requirements between the RXRECCLK output of the MGT and the RXUSRCLK and RXUSRCLK2 inputs. Table 3 shows the delay requirements of the RXRECCLK delay through the fabric to the RXUSRCLK or RXUSRCLK2. The worst case numbers take into account slower silicon, while the best case is faster silicon.

When comparing Table 1 and Table 2 with Table 3, the delay requirement is always met by the local routes as long as the CRC logic is disabled.

**Note:** These numbers do not have a direct correlation to speed grades.

Along with this timing analysis, this local clock route solution has been proven in the hardware at 125 MHz for most of the MGTs in an XC2VP70 device.

Table 3: RXRECCLK Worst-Case Delay Requirements

Condition	Min	Max
Worst case	1.4909	5.331
Typical case	1.054	5.587
Best case	0.764	5.813

**Notes:**

1. These requirements apply only when the CRC logic is disabled. CRC is not supported with these local clock routes.

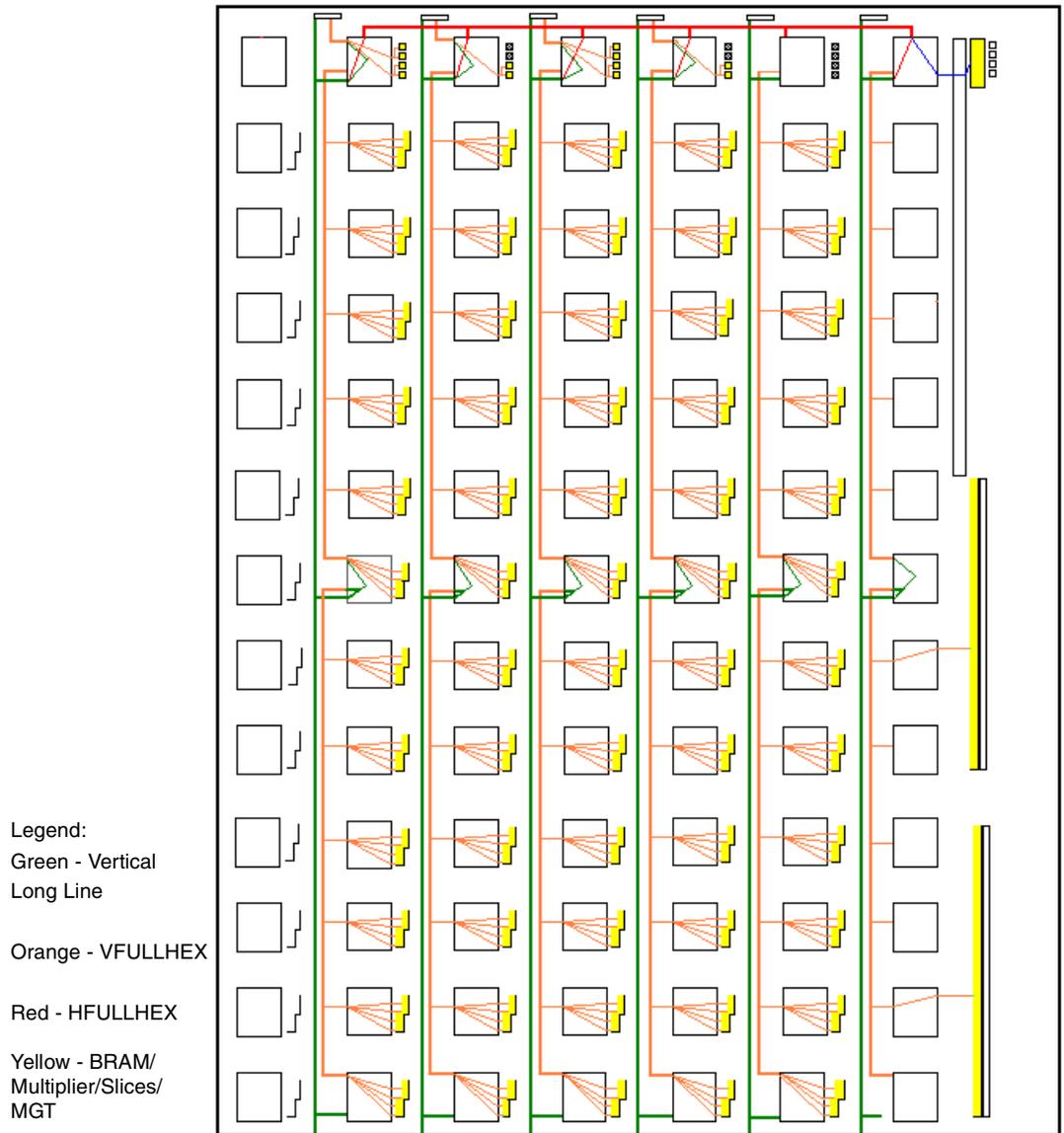


Figure 1: Local Clock Placement and Route for Top MGT

### Software Examples

These local clock routes are supported by ISE 6.1 SP3 and ISE 6.3, but they are not supported by ISE 6.2 or its service packs.

### Reference Design

The reference design contains three state machines. See [Figure 2](#).

One state machine generates transmit data that is clocked off the BREFCLK global resource.

The second state machine is also clocked off the BREFCLK and checks the data out of the CORE Generator™ FIFO. The CORE Generator FIFO represents a clock domain crossing that would be present in an asynchronous system. This FIFO could also contain clock correction/channel bonding functionality.

The third state machine checks the data being written into the FIFO. All this logic (including the Write side of the FIFO) is clocked with RXRECCLK and the local clock resources.

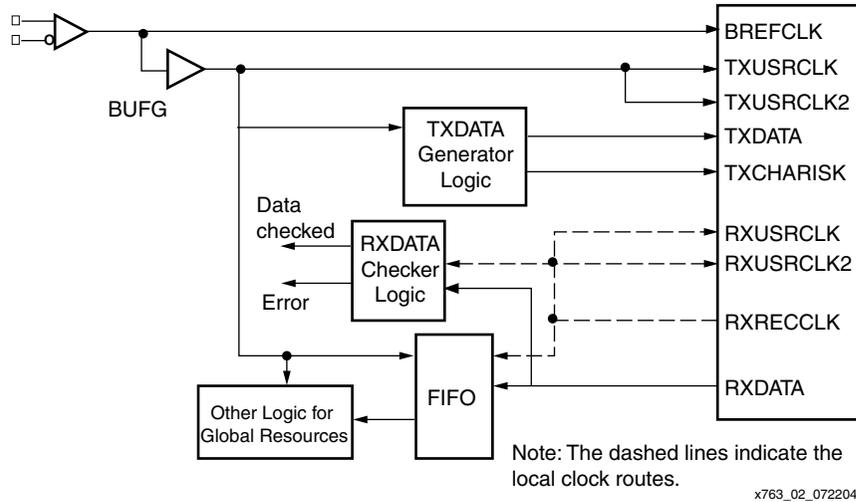


Figure 2: Reference Design Block Diagram

The reference design utilizes the Architecture Wizard to generate the code for the MGT instantiation. However, the Architecture Wizard does not allow the option to bypass the RX elastic buffer. To use the bypass option, modify the generated code so that the RX\_BUFFER\_USE attribute is set to False.

The reference design file is available on the Xilinx website at: [xapp763.zip](http://www.xilinx.com/xapp763.zip).

## Conclusion

The local clocking resources available in the Virtex-II Pro architecture for the MGT RXRECCLK allow bypassing of the RX elastic buffer, thereby decreasing RX latency without consuming global clock resources.

## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/04/04	1.0	Initial Xilinx release.
11/18/04	1.1	Changed title of <a href="#">Table 3</a> .