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16-Channel, DDR LVDS Interface with Per-Channel Alignment

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Summary

This application note describes a 16-channel, source-synchronous LVDS interface operating at double data rate (DDR). The transmitter (TX) requires 16 LVDS pairs for data and one LVDS pair for the forwarded clock. The transmitter operates at 8:1 serialization on each of the 16 data channels. The receiver (RX) also requires 16 LVDS pairs for data and one LVDS pair for the source-synchronous clock input. The receiver operates at 1:8 deserialization on each of the 16 data channels. The timing of the receiver is described in depth and characterized in hardware.

Introduction

The design described in the application note targets a Virtex™-5 FPGA, taking advantage of the ChipSync™ features available in every I/O of all Virtex-5 devices. These features include the ability to dynamically adjust the delay of the datapaths in the receiver with 75 ps resolution. Using this dynamic delay feature, the receiver in this application note escapes the limitations of static setup/hold timing by creating its own dynamic setup/hold timing. The interface calibrates out process variations by finding the optimal setup/hold timing for each individual device.

Figure 1 shows a Virtex-5 DDR interface talking to a DDR interface in another device that can be either an ASIC or an FPGA with support for a 16-channel DDR interface. Since this is a source-synchronous link, the receivers of both devices receive their clock from the TX side of the other device. The clock sources for the transmitters could come from a number of places in the backend systems, such as an oscillator on the PCB. Since each of the 16 data channels on the serial side of the interface runs at 8:1 serialization, the data on the parallel side of the DDR interface is 128 bits.

The stand-alone DDR interface described in this application note does not include user constraints (includes no UCF file). To evaluate the performance of this DDR interface in hardware, a separate bit error rate tester (BERT) is also available for download (Figure 2, page 2).

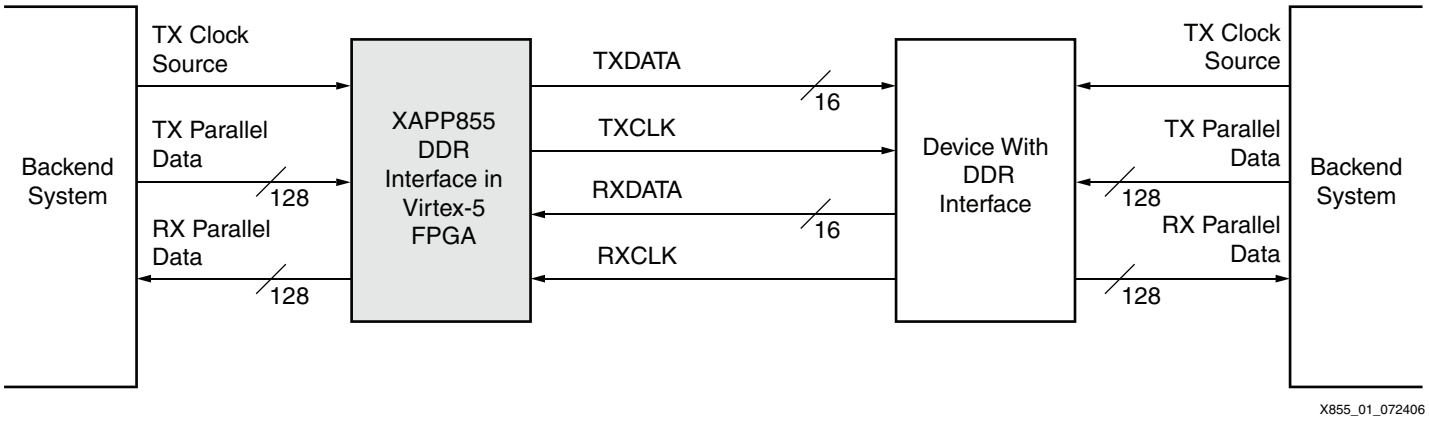


Figure 1: **Full-Duplex, 16-Channel DDR Link between a Virtex-5 Device and Another Device with a 16-Channel DDR Interface**

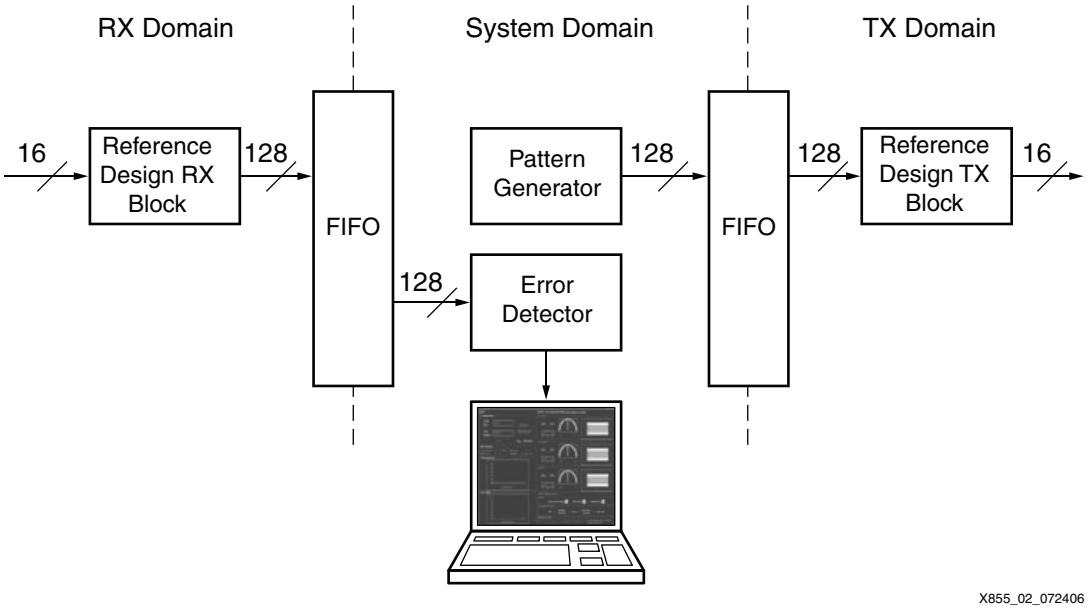


Figure 2: **BERT Testbench for Hardware Verification of the DDR Interface**

The BERT is a revision-controlled testbench and includes the latest version of the DDR interface. The Virtex-5 DDR transmitter is looped back to the DDR receiver in the same Virtex-5 device on an ML550 Networking Interfaces Board. The BERT communicates statistics about the interface performance to a graphical user interface on a PC. The BERT statistics are used extensively in the sections of this document concerned with hardware performance.

The design hierarchy of the interface itself is shown in Figure 3. The transmitter is very simple and contains almost no logic. The receiver contains logic that performs dynamic alignment on the 16 data channels.

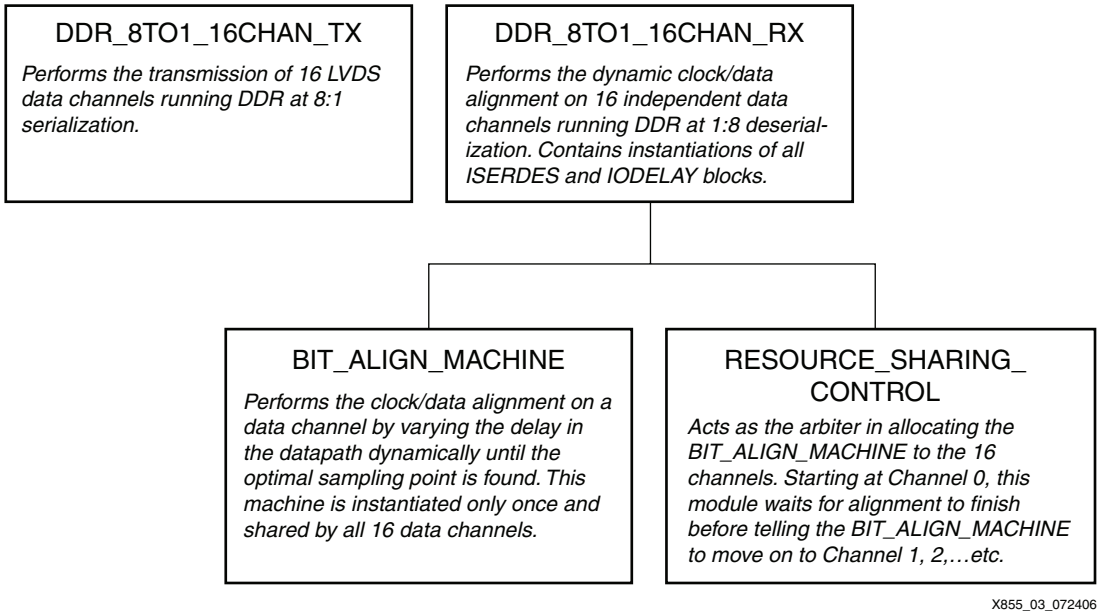


Figure 3: **Design Hierarchy of the Interface (TX and RX)**

DDR Transmitter

The DDR transmitter consists of only one module: DDR_8TO1_16CHAN_TX. The module takes 128 bits of data on the parallel side, performs an 8:1 serialization, and transmits 16 channels of LVDS data on the serial side. The port list is shown in Table 1.

Table 1: **DDR_8TO1_16CHAN_TX Module Port Definitions**

Port Name	I/O	Definition
DATA_TX_P [15:0]	Output	16 data channels (P)
DATA_TX_N [15:0]	Output	16 data channels (N)
CLOCK_TX_P	Output	Forwarded clock (P)
CLOCK_TX_N	Output	Forwarded clock (N)
TXCLK	Input	TX clock source
TXCLKDIV	Input	TX clock source divided by 4
DATA_TO_OSERDES [127:0]	Input	Parallel side data from backend system
RESET	Input	Reset synchronous to the TX domain
TRAINING_DONE	Input	Control signal telling the transmitter that receiver alignment is complete and user data can begin transmitting

Virtually no logic is used in the transmitter because all required functionality is contained within the OSERDES. The OSERDES is part of the ChipSync technology and is found in every I/O of all Virtex-5 devices. The OSERDES can be programmed to perform any serialization up to 10:1 and do single or double data rate transmission. For serializations greater than 6:1, a second OSERDES is needed (taken from the second I/O in the LVDS pair). The first OSERDES is called the master, and the second OSERDES is called the slave. Figure 4 shows a single channel of the TX.

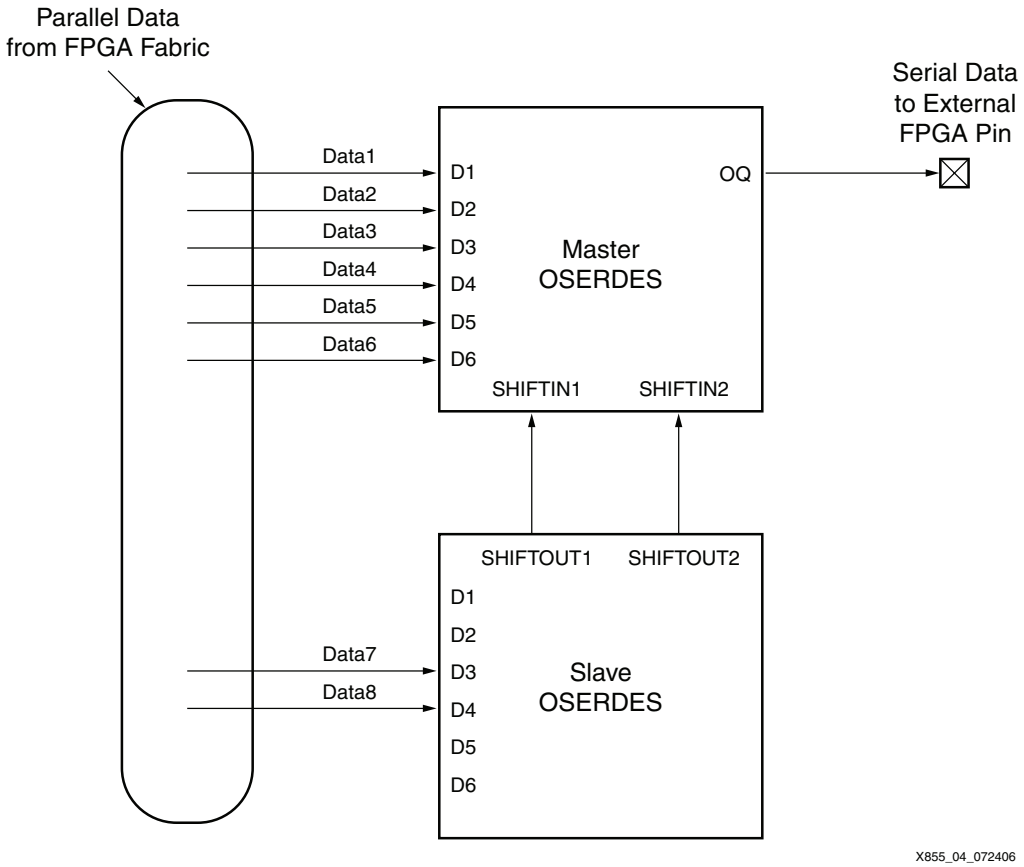
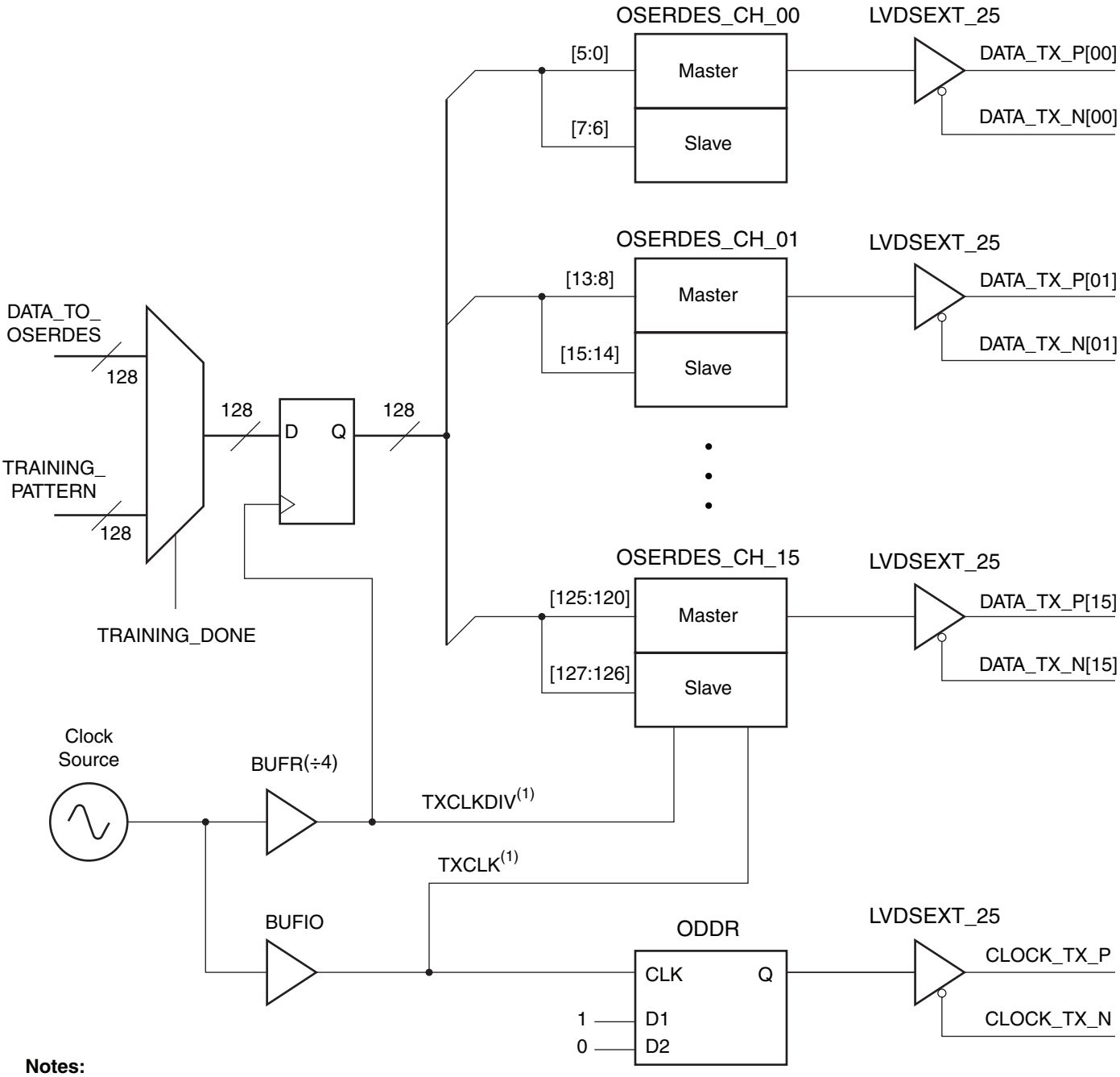


Figure 4: **Master/Slave OSERDES Pair for a Single Data Channel with 8:1 Serialization**

The transmitter interface (Figure 5) consists of 16 master/slave OSERDES pairs like the one shown in Figure 4, page 3. Since this interface is source synchronous, the clock must also be forwarded using the ODDR module.



Notes:
1. TXCLK and TXCLKDIV drive all OSERDES, both master and slave.

Figure 5: **Block Diagram of TX Interface**

The only logic in the TX Interface is the multiplexer that selects between real data and the training pattern. Since this interface depends on dynamic alignment within the receiver, the transmitter is required to send a training pattern until the receiver completes the alignment process on all 16 channels. In the design described in this application note, the select line to that multiplexer is assumed to be connected to a feedback signal from the receiver interface. If a feedback signal from the RX interface is undesirable, the MUX select line can be tied to a

timer that grants the receiver a fixed amount of time to complete alignment. For example, the transmitter can transmit the training pattern for 500 ms, after which it assumes that the receiver alignment process is complete and sends real data.

Table 2 shows the device utilization statistics for the TX interface implemented in a Virtex-5 device. Since there is no combinatorial logic in the transmitter, no look-up tables (LUTs) are used. The 128-bit MUX is implemented using only 128 flip-flops and no combinatorial logic. Table 2 also shows one BUFIO and one BUFR being used. This design can also be implemented using two BUFGs and a DCM instead. The different clocking options for this interface are discussed in "Interface Clocking."

Table 2: **DDR TX Interface Utilization Statistics**

Component	Quantity	Usage Description
Slice Flip-Flop	128	Registered MUX output of DATA_TO_OSERDES
Slice	32	128/4 FFs per slice = 32 slices
LUT	0	–
IOB	34	17 LVDS output pairs (16 data, 1 clock)
OSERDES	32	Master and slave OSERDES for every LVDS data pair
BUFIO	1	TXCLK
BUFR	1	TXCLKDIV

Interface Clocking

In the block diagram of the DDR transmitter shown in Figure 5, page 4, the clock networks are shown driven by BUFIO and BUFR. When BUFIO and BUFR are used to generate the serial and parallel clocks, the phase relationship between the two clocks is guaranteed by design to meet the input requirements of the OSERDES (and ISERDES). Another valid way of driving the clock networks in Figure 5 is to use global clocks combined with a DCM to divide by four. This scheme also provides phase-matched clock outputs, guaranteed by design to meet the input requirements of the OSERDES. The two valid clocking schemes are shown in Figure 6.

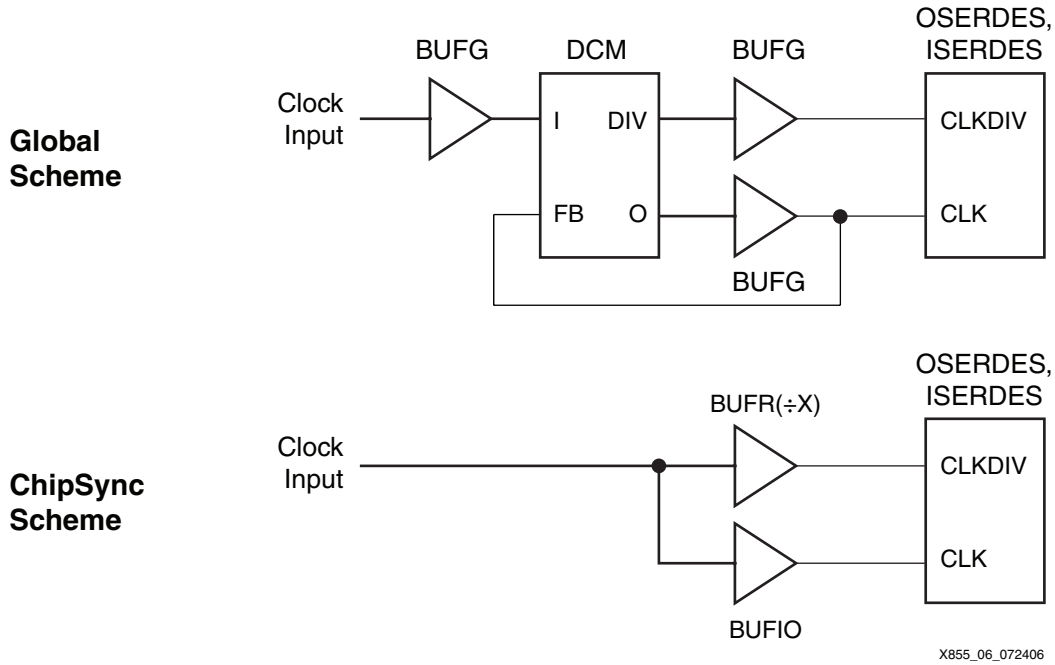


Figure 6: **Global and Regional Clocking Schemes in Virtex-5 FPGAs**

Which clocking scheme is the best to use? The BUFIO/BUFR networks maximize performance at the expense of some convenience. BUFIO and BUFR are regional clocks that cannot span the entire chip like a global clock. This difference means that transferring data between the regional and global domains must be a part of the designer's task and can simply mean adding a FIFO between the clock domains.

Global clocks have lower performance than BUFIO, but are more convenient to use. If a clock is placed on a global network, it can reach any component in the entire device. To show the performance advantage of BUFIO, Table 3 shows snapshots of several timing parameters, some of which are included in the timing budget calculations for source synchronous interfaces. In each case, BUFIO has an advantage over BUFG, and collectively those advantages are significant. These parameters are used in the timing budget calculation section, "Interface Timing Budget," page 18. For the most current specifications, always consult the data sheet on www.xilinx.com.

Table 3: **Comparison of Global and I/O Clock Performance by Speed Grade**

	-3	-2	-1	Units
Maximum Frequency				
BUFG max frequency	550	500	450	MHz
BUFIO max frequency	710	710	644	MHz
Duty Cycle Distortion				
BUFG DYCD	150	150	150	ps
BUFIO DYCD	100	100	100	ps
Sampling Error				
BUFG T_{SAMP}	450	500	550	ps
BUFIO T_{SAMP}	350	400	450	ps
Clock Tree Skew				
BUFG skew for XC5VLX50T	270	270	270	ps
BUFIO skew for all devices	50	50	50	ps

To offer the maximum performance, the interface described in this application note uses a BUFIO/BUFR clocking scheme in both the transmitter and receiver. The interface does not include the FIFO logic necessary to transfer the parallel data to/from the backend system domain. However, the BERT design discussed in "Introduction," page 1 (see Figure 2, page 2) shows how to transfer data to/from the RX and TX clock domains by using a FIFO18_36 primitive.

DDR Receiver

The DDR receiver consists of three core modules: DDR_8TO1_16CHAN_RX, BIT_ALIGN_MACHINE, and RESOURCE_SHARING_CONTROL. The receiver is more complex than the DDR transmitter because it includes a dynamic alignment algorithm implemented in the FPGA fabric. The DDR_8TO1_16CHAN_RX module takes 16 channels of data on the serial side, optimizes the timing relationship of each channel with the clock, performs 1:8 deserialization, and presents 128 bits of data on the parallel side. The port list is shown in Table 4.

Table 4: **DDR_8TO1_16CHAN_RX Module Port Definitions**

Port Name	I/O	Definition
DATA_RX_P [15:0]	Input	16 data channels (P).
DATA_RX_N [15:0]	Input	16 data channels (N).
CLOCK_RX_P	Input	Forwarded clock (P).
CLOCK_RX_N	Input	Forwarded clock (N).
INC_PAD	Input	Pulsing this pin causes the IDELAY tap setting of all data channels to increment by 1.
DEC_PAD	Input	Pulsing this pin causes the IDELAY tap setting of all data channels to decrement by 1.
DATA_FROM_ISERDES [127:0]	Output	Parallel side data to backend system.
RESET	Input	Reset synchronous to the RX domain.
IDLY_RESET	Input	Reset synchronous to the RX domain that only resets the IDELAY tap settings of all data channels.
IDELAYCTRL_RESET	Input	Reset synchronous to the TX domain that only resets the IDELAYCTRL module.
BITSLIP_PAD	Input	Pulsing this pin causes one bitslip operation on all data channels.
CLK200	Input	Reference clock to IDELAYCTRL module.
TAP_00, TAP_01, TAP_03, TAP_04, TAP_05, TAP_06, TAP_07, TAP_08, TAP_09, TAP_10, TAP_11, TAP_12, TAP_13, TAP_14, TAP_15	Output[5:0]	Each of these 6-bit signals contains the current IDELAY tap value of the sixteen data channels. Possible values: 0-63.
TAP_CLK [5:0]	Output	The 6-bit signal containing the current IDELAY tap value of the clock channel. Permanently set to zero because the clock channel is not adjusted.
TRAINING_DONE	Output	Flag indicating alignment is complete.
RXCLK	Output	RX Source Sync Clock.
RXCLKDIV	Output	RX Source Sync Clock divided by 4.
IDELAY_READY	Output	Flag indicating IDELAYCTRL is calibrated.

Most of the logic used in the receiver is contained within the ISERDES. The ISERDES is part of the ChipSync technology and is found in I/O of all Virtex-5 devices. The ISERDES can be programmed to do any deserialization up to 1:10 and do single or double data rate reception. For deserializations greater than 6:1, a second ISERDES is needed (taken from the second I/O in the LVDS pair). The first ISERDES is called the master, and the second ISERDES is called the slave. Figure 7 shows a single channel of the RX.

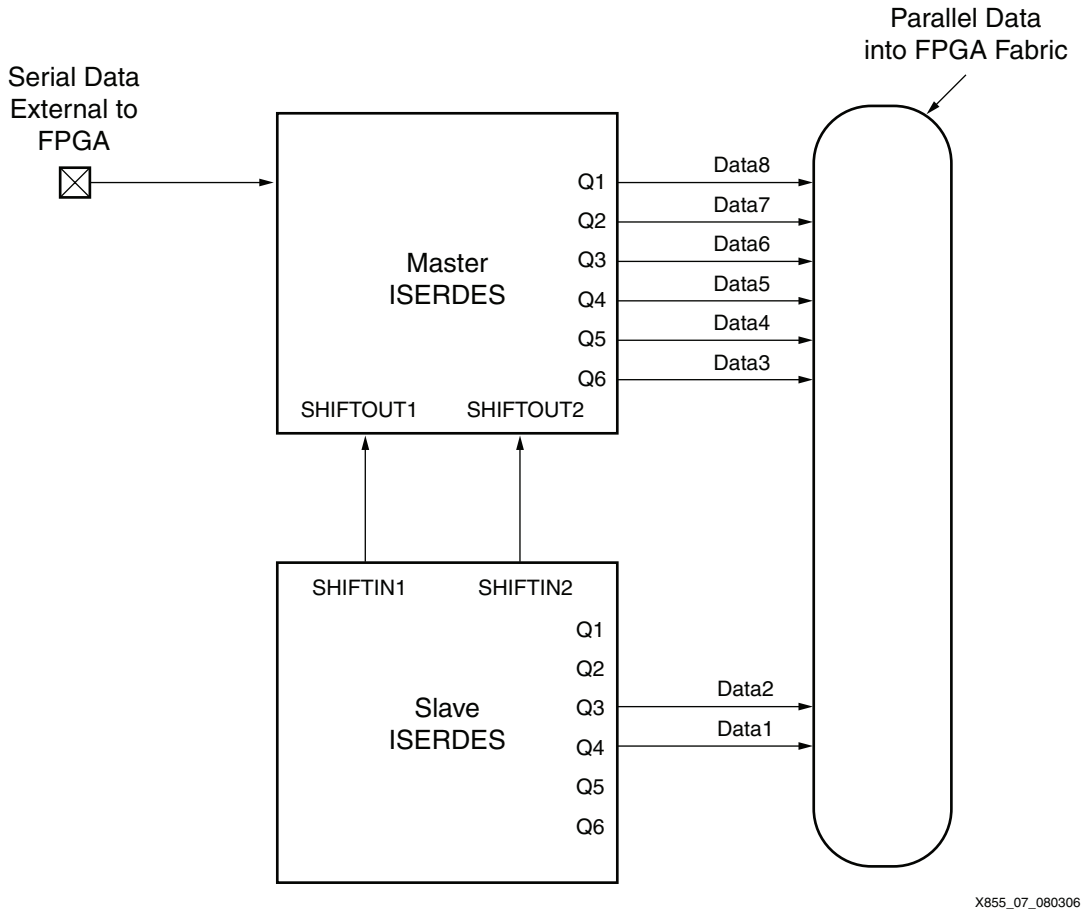
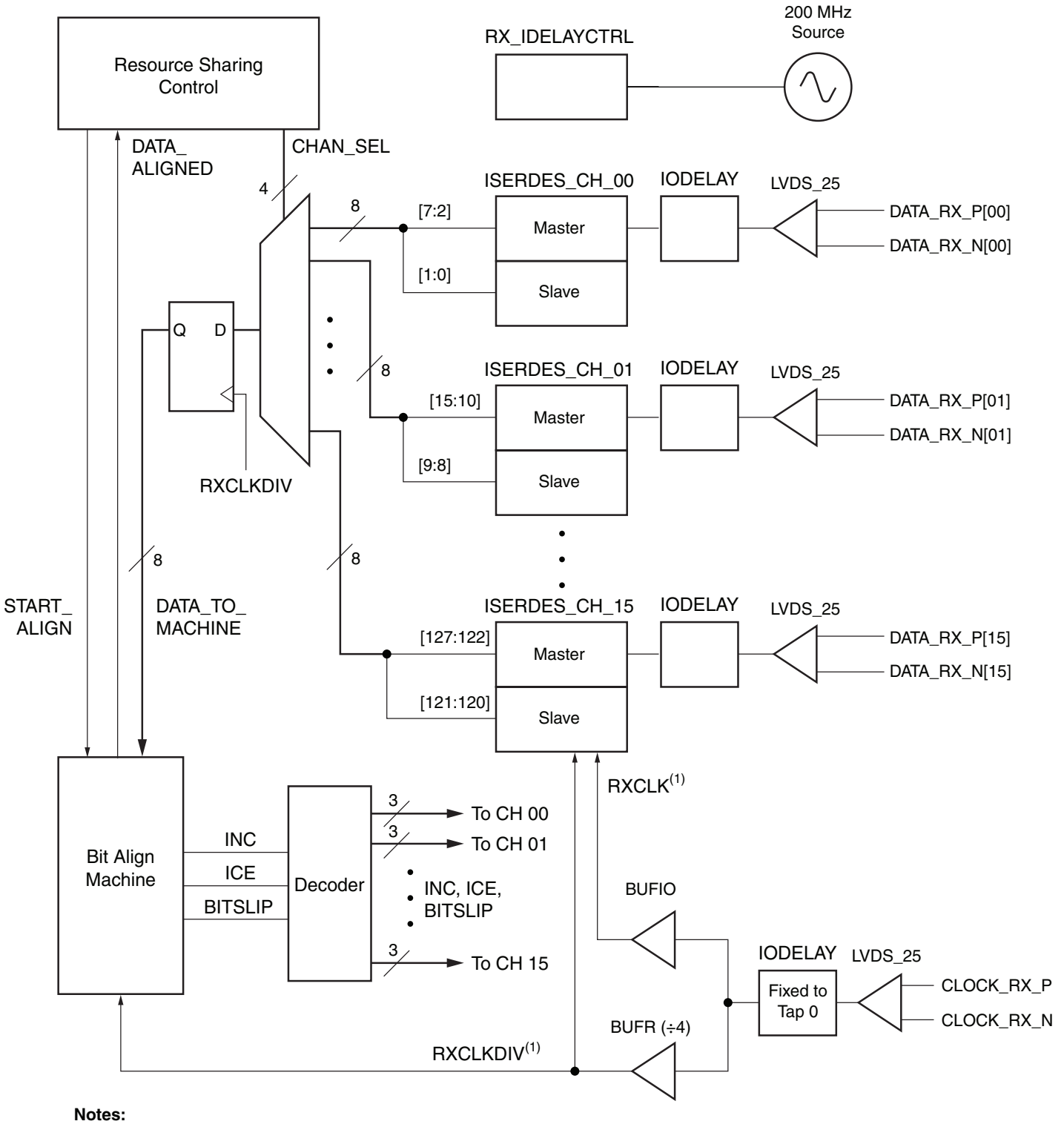


Figure 7: **Master/Slave ISERDES Pair for a Single Data Channel with 1:8 Deserialization**

The receiver interface (Figure 8) consists of 16 master/slave ISERDES pairs. Since this interface is source synchronous, the clock source comes from the transmitter. The clock is buffered in the receiver by a BUFIO component and divided to the parallel clock rate by a BUFR component.



Notes:
1. RXCLK and RXCLKDIV drive all ISERDES, both master and slave.

X855_08_082806

Figure 8: **Block Diagram of RX Interface**

Each ISERDES in Figure 8, page 9 contributes 8 bits to the 128-bit parallel data bus. Since there is only one instance of BIT_ALIGN_MACHINE in the receiver, each data channel must be aligned separately by sharing that resource. The 8-bit data buses from each ISERDES are fed into a MUX which selects which of the 16 channels has access to the BIT_ALIGN_MACHINE resource. RESOURCE_SHARING_CONTROL controls the MUX to ensure that every channel completes its alignment before the MUX switches to the next channel. The START_ALIGN signal tells the BIT_ALIGN_MACHINE that alignment can begin on the current channel because the MUX output is stable. The DATA_ALIGNED signal tells the RESOURCE_SHARING_CONTROL module that alignment on the current channel is complete.

The order of the parallel data outputs of the ISERDES is the opposite of the parallel data inputs of the OSERDES. The least significant OSERDES data inputs are fed into the master, while the least-significant ISERDES data outputs come from the slave (Figure 4, page 3 versus Figure 7).

The IDELAYCTRL module in Figure 8 is shown as having no connection to the rest of the receiver. Actually, IDELAYCTRL is required to calibrate the IODELAY blocks in the path of each data channel. A single IDELAYCTRL block is sufficient to calibrate all 16 data channels, since all channels are in the same bank.

The BIT_ALIGN_MACHINE generates three control signals that adjust the timing of the appropriate ISERDES. INC and ICE cause the IODELAY to increment or decrement the delay in the datapath by a fixed amount of ~75 ps (if a 200 MHz reference clock is used). BITSLIP causes each ISERDES to rotate the order of the parallel output data bits, facilitating the process of word alignment. These three control signals are directed to the appropriate ISERDES by the decoder shown in Figure 8. Although not shown in the figure, the decoder is also controlled by the RESOURCE_SHARING_CONTROL module.

Table 5 shows the device utilization statistics for the RX interface implemented in a Virtex-5 device. These figures exclude the counters used to track the IODELAY settings on all data channels; in most instances, those counters can be removed after the interface is integrated and verified in a specific environment. The majority of the LUTs utilized are consumed by the BIT_ALIGN_MACHINE, which is the core of the receiver alignment algorithm. As in the TX interface, the RX interface consumes one BUFIO and one BUFR for clocking. The clocking could also be accomplished using BUFGs and a DCM as described in "Interface Clocking," page 5, but the performance/convenience trade off would need to be considered.

Table 5: **DDR RX Interface Utilization Statistics**

Component	Quantity	Usage Description
Slice Flip-Flop	131	Multiple uses
Slice	105	Multiple uses
LUT	263	Multiple uses
IOB	34	17 LVDS input pairs (16 data, 1 clock)
ISERDES	32	Master and slave ISERDES for every LVDS data pair
BUFIO	1	RXCLK
BUFR	1	RXCLKDIV

Receiver Interface Dynamic Timing

The timing of the receiver interface is broken into two parts:

- The suboptimal timing inherent in the data and clock paths
- The optimal timing created by the receiver when adjusting dynamic delays on each of the 16 data channels.

Inherent Timing

An inventory of all propagation delays in the clock and datapaths must be taken to derive the inherent setup/hold times. The clock and datapaths for a single channel of this interface are shown in Figure 9. The ISE Timing Analyzer breaks down the paths into the timing parameters shown. All components in the path have both a minimum and maximum value to account for process variations.

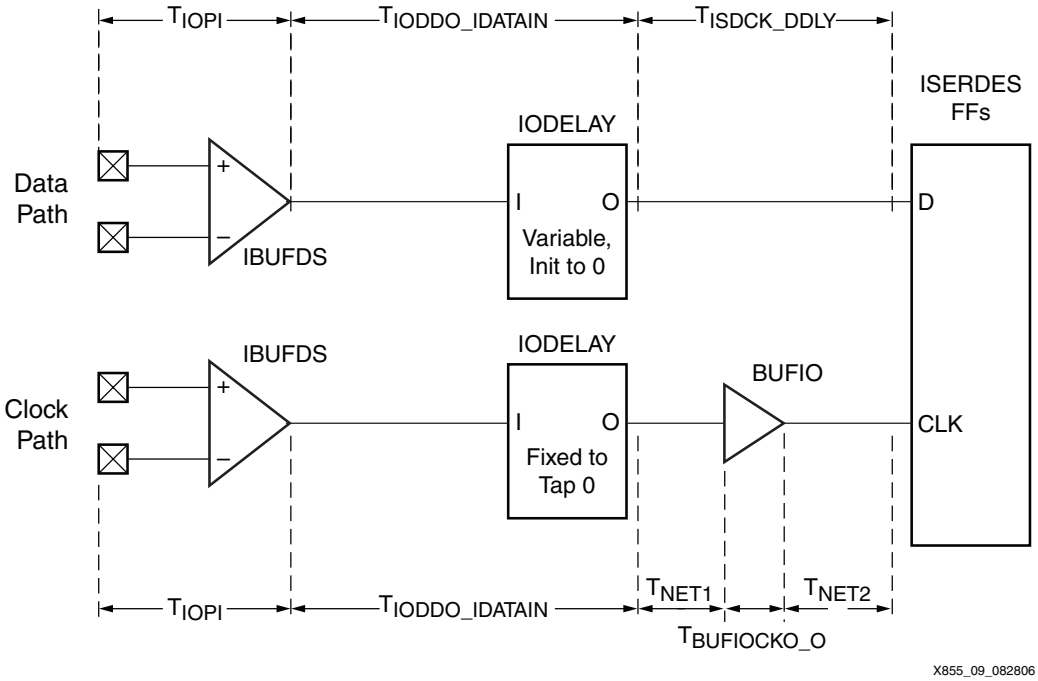


Figure 9: **Timing Components of RX Data and Clock Paths**

Figure 10, page 12 shows the timing analyzer settings used to generate the information in this report. Each of the timing parameters is described in Table 6, page 12 and Table 7. The minimum and maximum values of the individual timing parameters for the clock and datapaths are shown in Table 8 and Table 9, page 13.

Note: All raw timing numbers referenced in this document are subject to minor changes in subsequent revisions of the ISE tools.

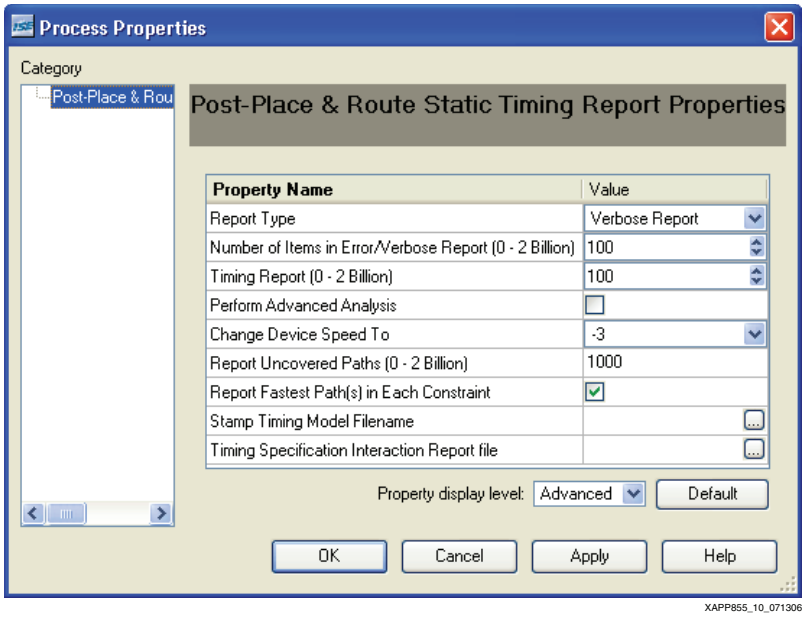


Figure 10: **ISE Timing Analyzer Properties Used in this Document**

Table 6: **Datapath Timing Definitions**

Timing Parameter	Description
T_{IOPI}	Delay from the IOB pad through the LVDS input buffer to the I pin of the IOB pad
$T_{IODDO\_IDATAIN}$	Delay from the I pin of IOB pad to the D input of the ISERDES
T_{ISDCK_DDLY}	Delay from the D input of the ISERDES to the sampling registers in the ISERDES (setup and hold times of ISERDES)

Table 7: **Clock Path Timing Definitions**

Timing Parameter	Description
T_{IOPI}	Delay from the IOB pad through the LVDS input buffer to the I pin of the IOB pad
$T_{IODDO\_IDATAIN}$	Delay from I pin of IOB pad to the O output of the IODELAY block
T_{NET1}	Delay from the O output of the IODELAY block to the I pin of BUFIO
$T_{BUFIOCKO\_O}$	Clock to out delay of BUFIO
T_{NET2}	Clock distribution delay from BUFIO output to the clock input of data ISERDES

Table 8: **Datapath Delay Inventory for a -1 Speed Grade XC5VLX50T Device**

Timing Parameter	Maximum Datapath Delay	Minimum Datapath Delay
T_{IOPI}	1.083 ns	0.763 ns
$T_{IODDO\_IDATAIN}$	0.671 ns	0.671 ns
T_{ISDCK_DDLY}	0.064 ns	–0.038 ns
TOTAL	1.818 ns	1.396 ns

Table 9: **Clock Path Delay Inventory for a -1 Speed Grade XC5VLX50T Device**

Timing Parameter	Maximum Clock Path Delay	Minimum Clock Path Delay
T_{IOPI}	1.150 ns	0.820 ns
$T_{IODDO\_IDATAIN}$	0.671 ns	0.671 ns
T_{NET1}	0.254 ns	0.190 ns
$T_{BUFIOCKO\_O}$	1.130 ns	0.894 ns
T_{NET2}	0.404 ns	0.319 ns
TOTAL	3.609 ns	2.894 ns

According to the inherent timing prediction, the data is going to arrive before the clock by an amount determined by Equation 1 and Equation 2. Equation 1 calculates that data arrives before the clock by at least 1.076 ns in a -1 device. Equation 2 calculates that data arrives before the clock by at most 2.213 ns. Equation 3 shows a timing window that covers all -1 devices under all conditions. This timing window describes the inherent timing of the data and clock paths. Assuming skew-matched PCB traces for all sixteen channels, then it can be assumed that all 16 channels in the receiver have roughly the same timing window.

$$\text{Setup Time} = \text{Max Data Delay} - \text{Min Clock Delay} = 1.818 - 2.894 = -1.076 \text{ ns} \quad \textit{Equation 1}$$

$$\text{Hold Time} = \text{Max Clock Delay} - \text{Min Data Delay} = 3.609 - 1.396 = 2.213 \text{ ns} \quad \textit{Equation 2}$$

$$\text{Timing Window} = 2.213 - 1.076 = 1.137 \text{ ns} \quad \textit{Equation 3}$$

Figure 11 shows the timing windows for all speed grades of an XC5VLX50T device as well as a hardware measurement of the inherent timing relationship (to validate the calculations). The hardware measurement shows the DDR interface data arriving 1.425 ns before the clock, which by inspection, places the device in all three speed grade ranges (the device used for the hardware measurement is a -2 device).

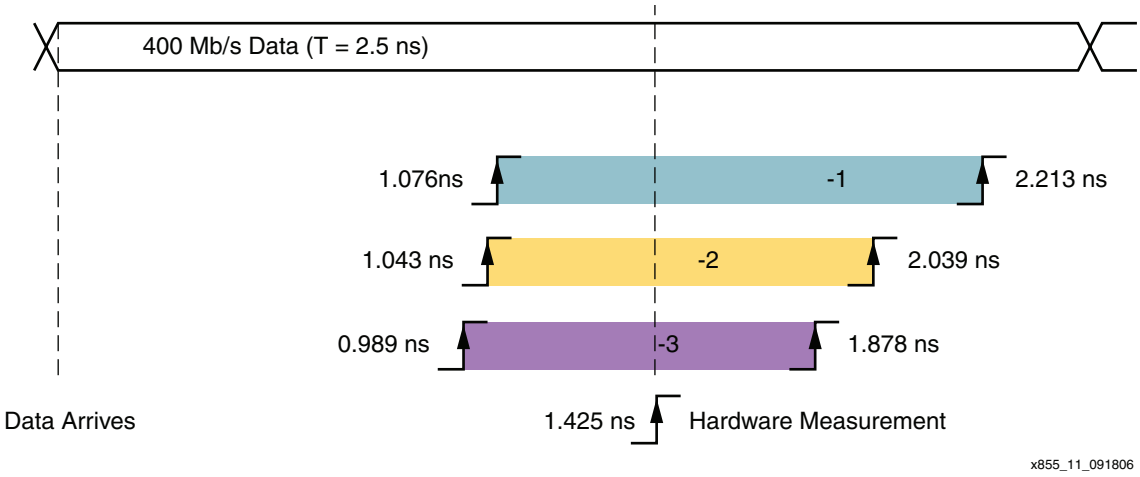


Figure 11: **Timing Windows Show Uncertainty in Clock/Data Relationship as Calculated by Timing Analyzer**

Dynamic Timing and BIT_ALIGN_MACHINE

In "Inherent Timing," page 11, the inherent timing of the interface was calculated for all speed grades and validated with a hardware measurement. In that case, the inherent timing was sufficient because the data rate is only 400 Mb/s (Figure 11, page 13). What happens when the data rate is increased such that the hold edge of the data window begins to shrink (Figure 12)?

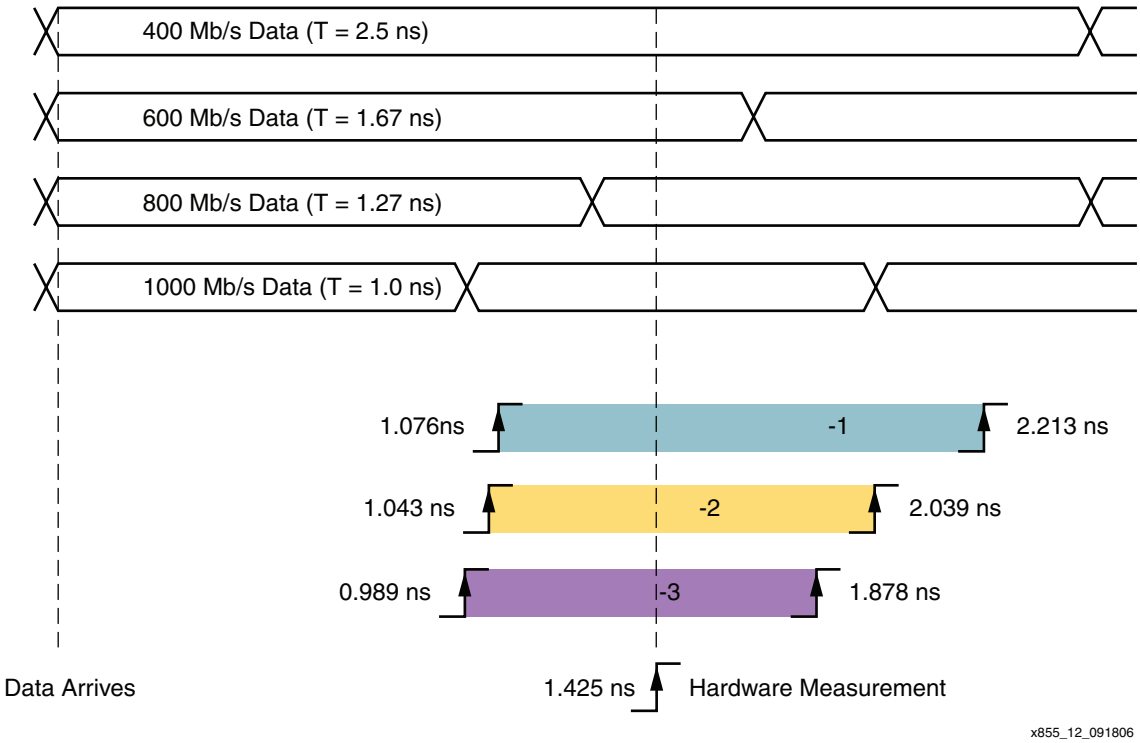


Figure 12: **Inherent Timing Windows Shown in Relation to Multiple Data Rates**

At 600 Mb/s, the inherent timing relationship is no longer adequate to meet timing because there are cases when the sampling clock edge is in the middle of the data transition. As the data rates increase to 800 and 1000 Mb/s, the clock actually captures the data arriving one bit time later. For designs that are sensitive to word alignment, this is unacceptable.

The solution to the suboptimal, inherent timing is dynamic timing. The BIT_ALIGN_MACHINE module in the receiver performs two functions of dynamic timing:

- **Bit Alignment:** Position the sampling edge of the clock at the center of the data eye by adding delay to the datapaths.
- **Word Alignment:** Ensure that the parallel data bits are in the correct order at the output of the ISERDES by using the bitslip function in the ISERDES.

The steps of the bit-alignment procedure are shown in Figure 13, page 15. Each step of the algorithm can either add or subtract delay from the datapath. All 16 channels are taken through this procedure independently. This procedure measures one full data eye (in terms of 75 ps delay taps) and then returns to the center of the data eye. Steps 1 and 2 are dedicated to moving through the partial eye of the initial timing, while steps 3 and 4 are dedicated to measuring a full eye. Step 5 is dedicated to positioning the clock edge at the center of the data eye.

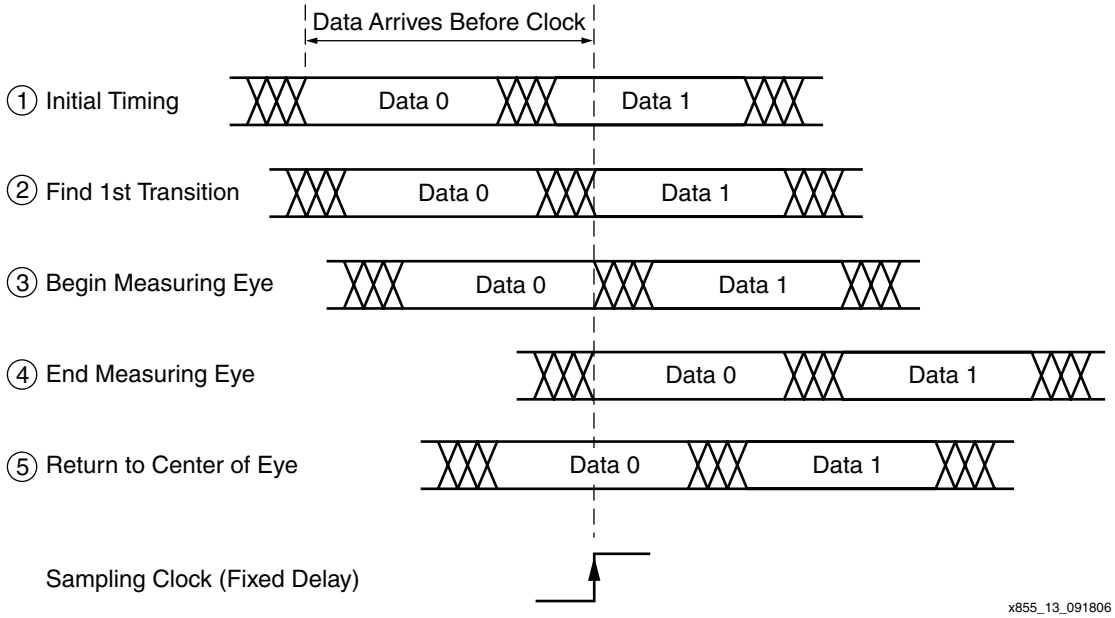


Figure 13: **Dynamic Bit-Alignment Procedure in BIT_ALIGN_MACHINE**

Jitter is represented in Figure 13 as multiple transition lines. Accounting for jitter is a crucial part of the algorithm. In step 2, the first data transition is found. If there is no jitter, then the eye measurement can begin instantly after finding the transition. However, when jitter is considered, the algorithm must find the first transition, move through the transition, and then begin looking for the second transition. If the algorithm does not move through the first transition intelligently, it runs the risk of falsely detecting the second transition.

Once bit alignment is complete, the order of the data bits can be adjusted to achieve word alignment. The bit-alignment procedure ensures that data is being sampled correctly, but the order of the data can be a few bits off from where the receiver expects it to be. To correct this, the bitslip feature of the ISERDES is used to "slip" bit times until the proper alignment is found. For this feature to be useful, a training pattern must be generated by the transmitter (as discussed in "DDR Transmitter," page 3) that the receiver can use to determine the proper word alignment. In this reference design, the training pattern is `00101100` (`0x2C`). This pattern is mostly arbitrary, as many other patterns work just as well. This pattern was chosen because a training pattern should behave electrically as much like real data as possible, such that the center of the training eye is the center of the data eye. Since real data contains strings of consecutive ones and zeros, it is best for the training pattern to do the same. For that reason, a `0x2C` pattern is better than an `0xAA` pattern because it contains run lengths of 1, 2, 3, and 4 bit times.

Table 10, page 16 shows the word-alignment process in the case where bit alignment completes with the data outputs set to `0x58`. Since `0x58` is not the training pattern the receiver is looking for, bitslip is asserted until `0x2C` is found. This reference design uses a 1:8 deserialization, so there are only eight possible configurations of the parallel data outputs. If bitslip is asserted infinitely, the same eight configurations will repeat. Bitslip in DDR mode is somewhat irregular because it does not simply rotate by one bit on every bitslip cycle. This effect is inconsequential to the word-alignment procedure (see the *Virtex-5 User Guide* for more details).

Table 10: **Word Alignment in the DDR Receiver**

Bitslip Cycle	Data Value (Hex)	Data Value (Bin)	Description of Bitslip operation
1	58	0101 1000	–
2	0B	0000 1011	Rotate 3 bits to right
3	16	0001 0110	Rotate 1 bit to left
4	C2	1100 0010	Rotate 3 bits to right
5	85	1000 0101	Rotate 1 bit to left
6	B0	1011 0000	Rotate 3 bits to right
7	61	0110 0001	Rotate 1 bit to left
8	2C	0010 1100	Rotate 3 bits to right

The FSM in the BIT_ALIGN_MACHINE module used to implement both bit and word alignment is shown in Figure 14, page 17. The FSM is divided into five sections, loosely described as: finding the first transition, getting through the first transition, finding the second transition, returning to the center of the eye, and word alignment.

To get through the first transition effectively for all possible types of jitter, two methods are used. The first method pertains to random jitter. If there is a lot of random jitter at the sampling point, then the samples generated are not stable. The algorithm detects this instability by comparing current samples to older samples and, therefore, knows where the transition begins and ends. But what if the jitter is extremely deterministic? The transition then has discreet crossing points, such that within the transition there is very stable, but incorrect, data. In this case, the algorithm does not sense any instability and falsely concludes that the sampling point is not in the transition. To address this case, apart from evaluating stability, the algorithm also evaluates the correctness of the data content by using the bitslip feature in the middle of the transition. For example, if the algorithm determines that the sampled data is stable, it then asserts bitslip to look for the correct data. If `0x2c` is found within eight assertions of bitslip, then the sampling point is not in the transition. But if `0x2c` is not found, then the algorithm increments the data delay and repeats the transition test again.

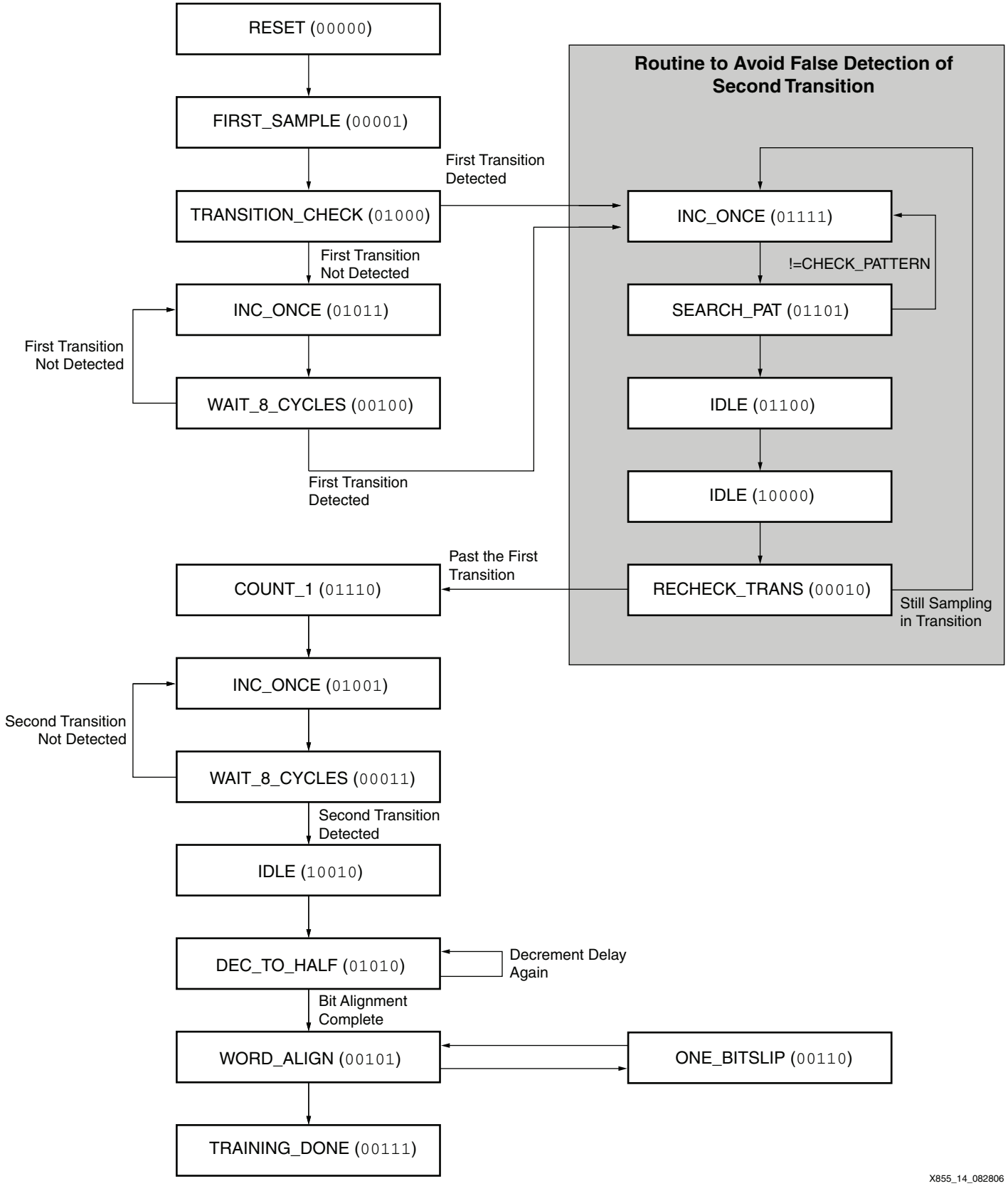


Figure 14: **FSM in the BIT_ALIGN_MACHINE Module**

Interface Timing Budget

In addition to sampling the data as closely as possible to the center of the data eye, the actual size of the data eye is important. By accurately predicting the size of the data eye in the receiver, the overall performance ceiling of the interface can be inferred. The ideal data eye width is the period of the data rate (for example, T_{Bit_Period} = 1.00 ns for 1000 Mb/s). Both the transmitter and receiver circuits have sources of error that subtract from the ideal data eye. The equation for the eye width at the output of the transmitter is shown in Equation 4. T_{JITTER} is the peak-to-peak jitter of the clock source driving the transmitter data bus and forwarded clock. T_{DCD} is the maximum duty cycle distortion of the clock tree driving the data bus and forwarded clock. Skew is not considered in the transmitter or receiver because the receiver calibrates out skew between channels by performing alignment on each channel individually.

$$DATA\_EYE\_WIDTH\_TX = T_{BIT\_PERIOD} - T_{JITTER} - T_{DCD\_BUFIO} \quad \textit{Equation 4}$$

Equation 5 calculates the width of the data eye at the receiver flip-flops. Ideally, the eye width at the receiver is the same as the eye width at the output of the transmitter, but there are sources of error in the transmission medium and receiver circuitry. Duty cycle distortion must be considered again on the receiver clock tree. T_{SAMP_BUFIO} is the receiver sampling error due to drift caused by voltage and temperature variations. $T_{IDELAYPAT\_JIT}$ is the amount of pattern dependent jitter that is accumulated in each tap of the IDELAY chain. For a clock pattern, $T_{IDELAYPAT\_JIT}$ is 0 ps/tap peak to peak. For a data pattern with long and short run lengths of zeroes and ones (simulated by PRBS23), $T_{IDELAYPAT\_JIT}$ is a finite value that must be considered in the timing budget.

$$DATA\_EYE\_WIDTH\_RX = DATA\_EYE\_WIDTH\_TX - T_{BOARD\_JITTER} - T_{SAMP\_BUFIO} - T_{DCD\_BUFIO} - [T_{IDELAYPAT\_JIT} \times \text{IDELAY taps in datapath}] - T_{QUANTIZATION\_ERR} \quad \textit{Equation 5}$$

T_{BOARD_JITTER} includes jitter induced by receiver input capacitance and the parasitics of the physical data path on the PCB. T_{BOARD_JITTER} must be determined by simulation, as it varies as a function of frequency and for receivers of different types and vendors. On the ML550, with a -2 speed-grade Virtex-5 device, the T_{BOARD_JITTER} is measured at roughly 200 ps at 900 Mb/s (assuming data content equivalent to PRBS23). $T_{QUANTIZATION\_ERR}$, or quantization error, is caused by the granularity of the IDELAY tap chain. Working with 75 ps increments, it is not possible to utilize the entire data eye, since inevitably some valid eye width is lost between two taps. The value for this loss is 75 ps. As long as the receiver eye width calculated using Equation 5 is greater than or equal to 0, the interface operates correctly over process, voltage and temperature.

For example, Equation 6 and Equation 7 show the timing budget calculation for the DDR interface running at 900 Mb/s in a -2 speed grade device on an ML550 evaluation board. Refer to the data sheet for the most current values. The TX interface is looped back to the RX interface on the same Virtex-5 FPGA, as shown in Equation 2.

$$DATA\_EYE\_WIDTH\_TX = 1111\ ps - 25\ ps - 100\ ps = 986\ ps \quad \textit{Equation 6}$$

$$DATA\_EYE\_WIDTH\_RX = 986\ ps - 200\ ps - 400\ ps - 100\ ps - [8\ ps \times 13\ taps] - 75\ ps = 107\ ps \quad \textit{Equation 7}$$

Changes in voltage and temperature cause the data channels of the interface to drift relative to the clock. If the DDR interface were to transfer user data for a long period of time over all specified conditions of temperature and voltage, Equation 7 states that there would be at least 107 ps (one or two IDELAY taps) of data window remaining valid during all fluctuations of temperature and voltage. Compare this calculation to the measurements in Table 12, page 21, Case: 900 Mb/s. There are four taps that are error free under all conditions. In "Appendix", there are three -2 devices tested at 900 Mb/s, and each has 4, 4, and 3 taps, respectively, that are error free under all conditions.

At a given temperature and voltage setting, the data valid window is much larger because there is no drift when temperature and voltage are constant. The size of the data valid window under constant conditions is 107 ps + T_{SAMP_BUFIO}, which in this case is at least 507 ps (six or seven IDELAY taps). Compare this calculation to the measurements of any single condition in Table 12, Case: 900 Mb/s. In the worst case (–5% supply) there are 7 taps that are error free.

Equation 8 and Equation 9 show the same timing budget calculation for the DDR interface running at 1.0 Gb/s in a -2 speed grade device on an ML550 Evaluation Board.

$$DATA\_EYE\_WIDTH\_TX = 1000\ ps - 25\ ps - 100\ ps = 875\ ps \quad \textit{Equation 8}$$

$$DATA\_EYE\_WIDTH\_RX = 875\ ps - 300\ ps - 400\ ps - 100\ ps - [8\ ps \times 15\ taps] - 75\ ps = -120\ ps \quad \textit{Equation 9}$$

Equation 9 predicts that no data window remains valid during all specified fluctuations of temperature and voltage (compare to Table 12, Case: 1000 Mb/s). In "Appendix", there are three -2 devices tested at 1000 Mb/s and each has 1, 3, and 1 taps, respectively, that are error free under all conditions. This data rate and device combination are very marginal cases.

To operate at 1.0 Gb/s, the DDR interface requires additional circuitry to track out voltage-temperature variations in real-time (see XAPP860, *16-channel DDR LVDS Interface with Real-time Window Monitoring,* for a DDR Interface with real-time window monitoring). If the voltage-temperature variations are removed from the picture, the predicted data valid window is –120 ps + T_{SAMP_BUFIO}, which in this case is at least 280 ps (3 or 4 taps). Compare this calculation to the measurements of any single condition in Table 18, page 34. There are at least four error-free taps in all conditions.

Interface Characterization

By following the procedure illustrated in Figure 13, page 15, the bit-alignment algorithm should never insert more than approximately 1.5 bit times of delay on the data channels. The fewest number of delay taps should be used in the datapath because they produce a finite amount of degradation ($T_{IDELAYPAT\_JIT}$). The worst-case initial timing for the algorithm occurs when the clock samples just before the data transitions, as in the 600 Mb/s case in Figure 12, page 14. The algorithm must move all the way through the first eye to find the first transition (1 bit time) and then move halfway into the next eye to center the sampling point (0.5 bit time). This process produces a worst-case total delay insertion of 1.5 bit times.

The actual performance of the bit-alignment algorithm is characterized as a function of data rate in Figure 15, page 20. For all data rates, the expectation is that the tap settings of all 16 channels in the DDR receiver do not exceed approximately 1.5 bit times of delay. Both the maximum and minimum tap setting of all 16 channels is recorded for each data rate. This graph only shows the data for a single device. Comparing the 1.5 bit time mask to the actual settings, it is clear that the algorithm remains within the 1.5 bit time limit. At 1.3 Gb/s, the tap setting actually exceeds the mask by one tap (a negligible violation).

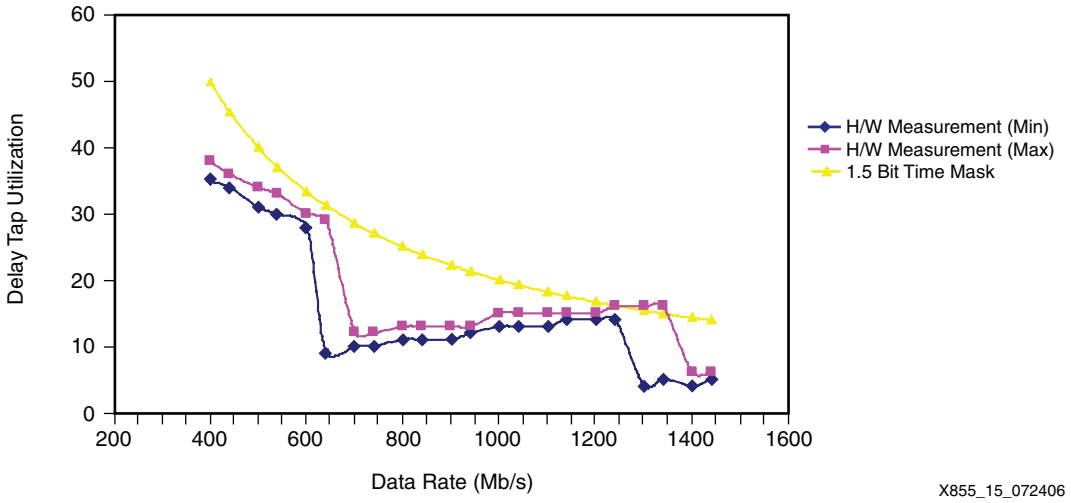


Figure 15: **Bit-Alignment Algorithm Performance**

The maximum and minimum tap settings in Figure 15 generally stay within 3 to 4 taps of each other, except in the case of 640 Mb/s and 1300 Mb/s data rates. These data rates are "seams" in the inherent timing. At data rates below 640 Mb/s, the tap settings are in the range of 30 taps, and at data rates above 640 Mb/s, the tap settings are in the range of 12 taps. Referring back to Figure 12, page 14, it is clear why this "seam" occurs. As the data rate increases past 600 Mb/s, the initial sampling point of the inherent timing moves into a different data eye, creating a different starting point for the algorithm. At 640 Mb/s, some of the 16 channels start in one eye, while other channels start in the other eye. Fortunately this is not an issue because the single bit time of difference between the channels is resolved using bitslip.

Referring back to Figure 8, page 9, the clock channel goes through an IDELAY block with a default value of 0. Once the data rate is chosen for a given design, this initial IDELAY value can be changed to a non-zero value to achieve more favorable inherent timing. For example, a design running at 620 Mb/s can use 30 IDELAY taps on the delay channels, each contributing a certain amount of jitter to the timing budget calculation. By setting the initial clock delay to 5 taps, the inherent timing moves across the seam shown in the 600 Mb/s range of Figure 15, causing the data channels to only use about 12 IDELAY taps. Only spectrally rich data patterns accumulate jitter in the IDELAY tap chain, so the clock IDELAY can be set to any value without diminishing the timing budget. This optimization is entirely optional and can be done once the design is running in hardware.

The DDR receiver is designed to remove skew between channels by aligning each channel individually. The ML550 board on which this reference design is characterized is designed to have minimal skew between channels. However, there is clearly a finite amount of skew between channels due to clock skew in the TX and RX BUFIO networks, package skew, and trace length tolerance on the ML550 board. Table 11, page 21 shows how the bit-alignment algorithm sets the delay for each channel differently to compensate for skew between channels. The table captures the range of settings among the 16 channels at specific data rates for a -2 device. If there were additional skew among the 16 channels, then the tap setting range would be larger to compensate for it. The algorithm is designed such that skew between channels should not diminish the performance of the interface. The range of tap settings differs for different devices and speed grades, but the magnitude should be approximately the same.

Table 11: **Tap Setting Range For Various Data Rates Measured on a -2 Device**

Data Rate (Mb/s)	Tap Setting Range	Compensated Skew
500	31–34	4 taps
600	28–30	3 taps
700	10–12	3 taps
800	11–13	3 taps
900	11–13	3 taps
1000	13–15	3 taps
1100	13–15	3 taps
1200	14–15	2 taps

Since the receiver alignment logic only runs once immediately after reset, the resulting dynamic timing must be adequate to ensure error-free operation over the specified voltage and temperature variations that can occur over time. The data-valid window at the receiver input must be wide enough to withstand these variations (receiver drift). Table 12, page 21 shows the data-valid window at the ISERDES registers in the DDR receiver. The eyes shown are collective eyes of all 16 channels. The BERT testbench configuration loops back the DDR transmitter to the DDR receiver. Using pattern generators and error detectors programmed to send and receive a pseudorandom bit sequence (PRBS23), the width of the data-valid window is evaluated using pseudorandom data that closely resembles real user data.

Table 12: **Measurement of Receiver Drift under Extreme Conditions for Multiple Data Rates**

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
Case: 800 Mb/s																	
25°C, Nom Supplies	F	F	F	P	P	P	P	P	C	P	P	P	P	P	F	F	F
0°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F
25°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
0°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F
0°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	F
85°C, –5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																

Table 12: **Measurement of Receiver Drift under Extreme Conditions for Multiple Data Rates *(Continued)***

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
Case: 900 Mb/s																	
25°C, Nom Supplies	F	F	F	F	P	P	P	P	C	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
Case: 1000 Mb/s																	
25°C, Nom Supplies	F	F	F	F	F	P	P	P	C	P	P	P	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
Case: 1100 Mb/s																	
25°C, Nom Supplies	F	F	F	F	F	P	P	P	C	P	F	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																

Table 12: **Measurement of Receiver Drift under Extreme Conditions for Multiple Data Rates *(Continued)***

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
Case: 1200 Mb/s																	
25°C, Nom Supplies	F	F	F	F	F	F	P	P	C	P	F	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	F	F	F	F	F	F
CONCLUSION	Errors caused by ±5% variations in supply voltages.																

Notes:

1. Where 0 is the reference tap determined by the bit-align machine under nominal conditions at 25°C.
2. P = Error-free transmission; F = Error in transmission; C = IODELAY tap position selected by bit-align machine under nominal conditions at 25°C.
3. Device under test is -2 speed grade.

In all test cases shown in Table 12, page 21, the bit-align machine accurately places the sampling point in the center of the data eye (indicated by the "C" in each test case). In the 1100 Mb/s case, the bit-align machine places the sampling point slightly off center. This slight inaccuracy occurs when the center of a real data pattern diverges from the center of the training pattern. The electrical behavior of different data patterns is discussed below.

After the dynamic timing is established for a given test case under nominal conditions, the device is subjected to extremes of temperature and voltage to stress the receiver timing. At data rates of 1100 Mb/s and below, the dynamic timing established after reset under nominal conditions is sufficient to meet timing over all specified extreme conditions (the column with the "C" passes traffic error free under all conditions). At a data rate of 1200 Mb/s, the design operates correctly under nominal conditions, but the data-valid window is not large enough to withstand the voltage variations. For this particular transmission medium, the 1200 Mb/s case requires a real-time adjustment circuit that could track the center of the eye.

The full datapath of the testbench consists of:

TX → 5" FR-4 → SAMTEC QSE Conn → 12" Ribbon Cable → SAMTEC QSE Conn → 5" FR-4 → RX

For shorter transmission media, higher performance can be achieved in accordance with the section "Interface Timing Budget," page 18. Interface performance is not solely a question of the LVDS driver performance specification, but rather a question of adequate timing margin to withstand production and environmental variations. From Table 12, the total amount of variation experienced over temperature and voltage is roughly 375 ps (5 taps at 75 ps per tap). This number should be comparable to the specification for receiver sampling error (T_{SAMP_BUFIO}) shown in the *Virtex-5 Data Sheet*.

Pattern Dependence of Receiver Performance

Different types of data patterns have different electrical signatures (rise and fall times, jitter, eye symmetry, etc.). A pattern with very narrow spectral content (such as a clock pattern) moves very favorably through the link because the receiver frequency response has little effect on the signal integrity. However, a pattern with wide spectral content (such as real data and pseudorandom patterns) stresses the link's frequency response. If the frequency response is not flat across the entire spectrum of the data content, then the signal integrity is degraded as a result. The amount of degradation measured is shown in Table 13, page 25. The DDR transmitter is looped back to the DDR receiver, and different patterns are programmed to traverse the link. Performance is assessed by evaluating the integrity of those patterns in the receiver.

PRBS7 is a pseudorandom data pattern with a maximum run length of seven consecutive zeroes or ones. PRBS15 is defined as having a maximum run length of fifteen consecutive zeroes or ones. These limitations on run lengths limit the spectral content of the pattern. A PRBS15 pattern has greater spectral content than a PRBS7 pattern and, therefore, is a more strenuous test for the link. PRBS29 is the most strenuous test in Table 13. A clock pattern is effectively a PRBS1.

As predicted, Table 13 shows that there is more degradation for data patterns with more spectral content. At 1000 Mb/s and below, the data eye closure is symmetrical. Symmetrical eye closure is desired because it does not change the center of the eye as determined by the bit-alignment algorithm. Above 1000 Mb/s, the eye closure becomes more asymmetrical, causing the center of the data eye to diverge from the calibrated center (by only 1 tap).

In every data rate shown in Table 13, all significant pattern-dependent degradation is caused between PRBS1 (clock pat) and PRBS15. Between PRBS15 and PRBS29, there is no additional degradation recorded in any of the measurements.

Table 13: **Link Performance for Various Types of Data Measured on a -2 Device**

Pattern	IODELAY Taps (1)																	
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8	+9
Case: 600 Mb/s																		
Clock Pat (0101)	P	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	P	P
Training Pat (0x2C)	P	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	P	F
PRBS7	P	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	P	F
PRBS15	F	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	F	F
PRBS23	F	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	F	F
PRBS29	F	P	P	P	P	P	P	P	C	P	P	P	P	P	P	P	F	F
Case: 800 Mb/s																		
Clock Pat (0101)	F	F	P	P	P	P	P	P	C	P	P	P	P	P	P	F	F	F
Training Pat (0x2C)	F	F	P	P	P	P	P	P	C	P	P	P	P	P	P	F	F	F
PRBS7	F	F	P	P	P	P	P	P	C	P	P	P	P	P	F	F	F	F
PRBS15	F	F	F	P	P	P	P	P	C	P	P	P	P	P	F	F	F	F
PRBS23	F	F	F	P	P	P	P	P	C	P	P	P	P	P	F	F	F	F
PRBS29	F	F	F	P	P	P	P	P	C	P	P	P	P	P	F	F	F	F
Case: 1000 Mb/s																		
Clock Pat (0101)	F	F	F	P	P	P	P	P	C	P	P	P	P	P	F	F	F	F
Training Pat (0x2C)	F	F	F	P	P	P	P	P	C	P	P	P	P	F	F	F	F	F
PRBS7	F	F	F	F	P	P	P	P	C	P	P	P	F	F	F	F	F	F
PRBS15	F	F	F	F	F	P	P	P	C	P	P	P	F	F	F	F	F	F
PRBS23	F	F	F	F	F	P	P	P	C	P	P	P	F	F	F	F	F	F
PRBS29	F	F	F	F	F	P	P	P	C	P	P	P	F	F	F	F	F	F
Case: 1200 Mb/s																		
Clock Pat (0101)	F	F	F	F	P	P	P	P	C	P	P	P	P	F	F	F	F	F
Training Pat (0x2C)	F	F	F	F	P	P	P	P	C	P	P	P	F	F	F	F	F	F
PRBS7	F	F	F	F	F	P	P	P	C	P	F	F	F	F	F	F	F	F
PRBS15	F	F	F	F	F	F	P	P	C	F	F	F	F	F	F	F	F	F
PRBS23	F	F	F	F	F	F	P	P	C	F	F	F	F	F	F	F	F	F
PRBS29	F	F	F	F	F	F	P	P	C	F	F	F	F	F	F	F	F	F
Case: 1400 Mb/s																		
Clock Pat (0101)	F	F	F	F	F	F	P	P	C	P	P	P	F	F	F	F	F	F
Training Pat (0x2C)	F	F	F	F	F	P	P	P	C	P	P	F	F	F	F	F	F	F
PRBS7	F	F	F	F	F	F	F	P	C	P	F	F	F	F	F	F	F	F
PRBS15	F	F	F	F	F	F	F	P	C	F	F	F	F	F	F	F	F	F
PRBS23	F	F	F	F	F	F	F	P	C	F	F	F	F	F	F	F	F	F
PRBS29	F	F	F	F	F	F	F	P	C	F	F	F	F	F	F	F	F	F

Notes:

1. Where 0 is the reference tap determined by the bit-align machine under nominal conditions at 25°C.
2. P = Error-free transmission; F = Error in transmission; C = IODELAY tap position selected by bit-align machine under nominal conditions at 25°C.

Resetting the Interface

Several dependencies determine the order in which circuits should be reset in the interface. The receiver cannot begin the alignment algorithm if the transmitter is not sending the training pattern. The transmitter must be reset before the receiver, and time must be allowed for the training pattern to propagate across the link before the receiver comes out of reset. The receiver also cannot begin the alignment algorithm until IDELAYCTRL has recovered from reset, which could takes hundreds of cycles. The recommended reset timing for the interface is shown in Figure 16. This reset timing is implemented in the BERT testbench for this interface.

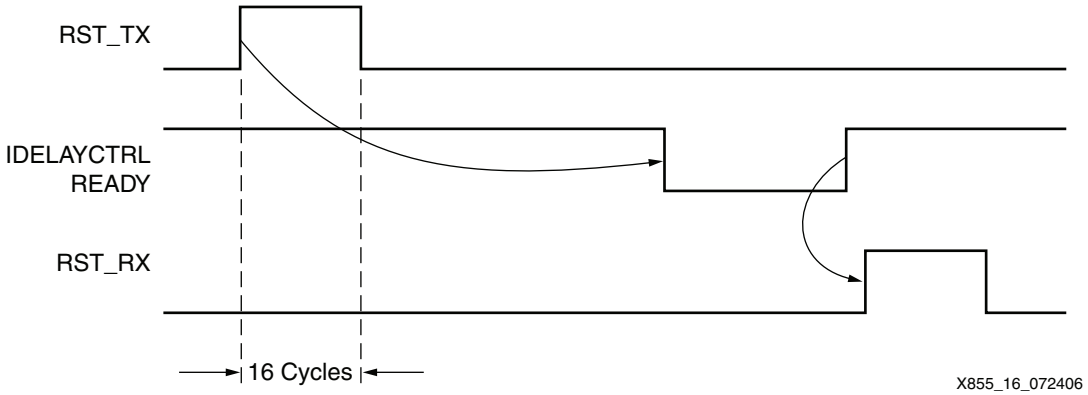


Figure 16: **Recommended Interface Reset Timing**

The TX reset (RST_TX) is used to reset all TX circuitry and also IDELAYCTRL. The IDELAYCTRL reset is asynchronous so driving it with RST_TX is acceptable. The minimum pulse width of IDELAYCTRL reset is 50 ns ($T_{IDELAYCTRL\_RPW}$). For that reason, resets are held High for 16 clock cycles. The RX reset (RST_RX) is used to reset all RX circuitry and is asserted when the IDELAYCTRL READY flag goes High, indicating that the IODELAY blocks are calibrated.

The timing of the READY flag in Figure 16 is a potential hazard. Most likely, it is High during a TX reset because it takes many cycles for IDELAYCTRL to deassert the READY flag. It is easy to make the mistake of resetting the receiver too early. To avoid this hazard, the RX reset should be asserted only after seeing a deassertion and reassertion of the READY flag.

Conclusion

Based on the design and characterization described in this document, the 16-Channel DDR reference design operates to the performance targets in Table 14 under all conditions of process, voltage and temperature. However, to meet these targets over voltage and temperature, the timing budget must be guaranteed according to the analysis in "Interface Timing Budget." See "Appendix," page 27 for further justification of the maximum performance recommendations in Table 14.

Table 14: **Performance of 16-Channel DDR Interface**

Speed Grade	Maximum Performance
-1	800 Mb/s
-2	900 Mb/s
-3	1.0 Gb/s(1)

Notes:

1. To achieve higher performance (up to 1.25 Gb/s), see *16-channel DDR LVDS Interface with Realtime Window Monitoring* for an example of a DDR interface with real-time window monitoring.

Appendix

Performance Characterization Data

Refer to "Interface Characterization," page 19 for explanations about how to interpret the data in the "Appendix". These tables show "collective" data eyes for the entire interface over process, voltage, and temperature (PVT). Three devices from each speed grade were selected for this characterization.

The calibrated center position of the eye (marked by the "C" in the tables below) varies slightly from channel to channel (due to small skews between channels). That range is referred to as center tap range. Analysis of Table 16, page 28 through Table 20, page 40 shows that the center tap range for slow and fast parts differ significantly at the same data rate (because the BIT_ALIGN_MACHINE algorithm adjusts for differences in speed).

All data in the "Appendix" is collected using the BERT testbench shown in Figure 2, page 2. The data pattern is PRBS23 and the device/package is XC5VLX50T-FF1136. The transmission path for the cases shown in Table 16 through Table 20 is repeated for convenience:

TX → 5" FR-4 → SAMTEC QSE Conn → 12" Ribbon Cable → SAMTEC QSE Conn → 5" FR-4 → RX

A summary of these characterization results is shown in Table 15. Each of the nine parts were tested at 800, 900, 1000, 1100, and 1200 Mb/s. When the interface is error free on all channels under all extreme conditions of temperature and voltage, the particular test case is designated by a P. A test case is marked FAIL when the interface suffered errors on any channel under any particular condition of voltage and temperature.

Table 15: **Summary of Interface Characterization Results**

Device (S/N)	Speed Grade	800 Mb/s	900 Mb/s	1000/Mb/s	1100 Mb/s	1200 Mb/s
2194	-1	P	P	P	FAIL	FAIL
2219	-1	P	FAIL	FAIL	FAIL	FAIL
2199	-1	P	P	FAIL	FAIL	FAIL
001	-2	P	P	FAIL	P	FAIL
002	-2	P	P	P	P	FAIL
003	-2	P	P	FAIL	FAIL	FAIL
004	-3	P	P	P	P	P
005	-3	P	P	P	P	P
006	-3	P	P	P	P	P

Table 16: **Measurement of Receiver Drift under Extreme Conditions at 800 Mb/s**

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
S/N 2194, Speed Grade: -1																	
25°C, Nom Supplies	F	F	F	P	P	P	P	P	C	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
0°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F
0°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F
85°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F
Center Tap Range	Taps 11–12																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 2219, Speed Grade: -1																	
25°C, Nom Supplies	F	F	F	P	P	P	P	P	C	P	P	P	F	F	F	F	F
0°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F
Center Tap Range	Taps 13–16																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 2199, Speed Grade: -1																	
25°C, Nom Supplies	F	F	F	P	P	P	P	P	C	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
0°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F
0°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F
85°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F
Center Tap Range	Taps 10–12																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																

Table 16: **Measurement of Receiver Drift under Extreme Conditions at 800 Mb/s *(Continued)***

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
S/N 001, Speed Grade: -2																	
25°C, Nom Supplies	F	F	F	P	P	P	P	P	C	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
0°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F
0°C, –5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F
85°C, –5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F
Center Tap Range	Taps 10–12																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 002, Speed Grade: -2																	
25°C, Nom Supplies	F	F	F	P	P	P	P	P	C	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
0°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F
0°C, –5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F
85°C, –5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F
Center Tap Range	Taps 10–12																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 003, Speed Grade: -2																	
25°C, Nom Supplies	F	F	F	P	P	P	P	P	C	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
0°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F
0°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F
85°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F
Center Tap Range	Taps 11–13																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																

Table 16: **Measurement of Receiver Drift under Extreme Conditions at 800 Mb/s *(Continued)***

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
S/N 004, Speed Grade: -3																	
25°C, Nom Supplies	F	F	F	P	P	P	P	P	C	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
0°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F
0°C, –5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F
85°C, –5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F
Center Tap Range	Taps 8–9, 23–24																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 005, Speed Grade: -3																	
25°C, Nom Supplies	F	F	P	P	P	P	P	P	C	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F
25°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
0°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	F	F
0°C, –5% Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	F	F
85°C, –5% Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	F	F
Center Tap Range	Taps 9–10																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 006, Speed Grade: -3																	
25°C, Nom Supplies	F	F	P	P	P	P	P	P	C	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
0°C, +5% Supplies	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, –5% Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F
0°C, –5% Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	P	F	F	F
85°C, –5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F
Center Tap Range	Taps 8–9, 23–24																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																

Notes:

1. IODELAY taps, where "0" is the reference tap determined by the bit align machine at nominal voltage and 25°C.
2. P = Error-free transmission; F = Error in transmission; C = IODELAY tap position selected by bit-align machine under nominal conditions at 25°C.

Table 17: **Measurement of Receiver Drift under Extreme Conditions at 900 Mb/s**

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
S/N 2194, Speed Grade: -1																	
25°C, Nom Supplies	F	F	F	F	F	P	P	P	C	P	P	P	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F
Center Tap Range	Taps 11–12																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 2219, Speed Grade: -1																	
25°C, Nom Supplies	F	F	F	F	F	P	P	P	C	P	P	P	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	P	P	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	P	P	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F
Center Tap Range	Taps 12–15																
CONCLUSION	Errors caused by –5% variation in supply voltage																
S/N 2199, Speed Grade: -1																	
25°C, Nom Supplies	F	F	F	F	F	P	P	P	C	P	P	P	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F
Center Tap Range	Taps 10–12																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																

Table 17: **Measurement of Receiver Drift under Extreme Conditions at 900 Mb/s *(Continued)***

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
S/N 001, Speed Grade: -2																	
25°C, Nom Supplies	F	F	F	F	P	P	P	P	C	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F
Center Tap Range	Taps 9–11																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 002, Speed Grade: -2																	
25°C, Nom Supplies	F	F	F	F	P	P	P	P	C	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F
Center Tap Range	Taps 10–12																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 003, Speed Grade: -2																	
25°C, Nom Supplies	F	F	F	F	F	P	P	P	C	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F
Center Tap Range	Taps 11–13																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																

Table 17: **Measurement of Receiver Drift under Extreme Conditions at 900 Mb/s *(Continued)***

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
S/N 004, Speed Grade: -3																	
25°C, Nom Supplies	F	F	F	F	P	P	P	P	C	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F
Center Tap Range	Taps 7–8																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 005, Speed Grade: –3																	
25°C, Nom Supplies	F	F	F	P	P	P	P	P	C	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
0°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F
0°C, –5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F
Center Tap Range	Taps 9–10																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 006, Speed Grade: -3																	
25°C, Nom Supplies	F	F	F	F	P	P	P	P	C	P	P	P	P	F	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F
85°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F
25°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
0°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F
0°C, –5% Supplies	F	F	F	F	F	P	P	P	P	P	P	P	P	P	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F
Center Tap Range	Taps 7–8																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																

Notes:

1. IODELAY taps, where "0" is the reference tap determined by the bit align machine at nominal voltage and 25°C.
2. P = Error-free transmission; F = Error in transmission; C = IODELAY tap position selected by bit-align machine under nominal conditions at 25°C.

Table 18: **Measurement of Receiver Drift under Extreme Conditions at 1000 Mb/s**

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
S/N 2194, Speed Grade: -1																	
25°C, Nom Supplies	F	F	F	F	F	P	P	P	C	P	P	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F
Center Tap Range	Taps 12–13																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 2219, Speed Grade: -1																	
25°C, Nom Supplies	F	F	F	F	F	F	P	P	C	P	P	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	P	P	P	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F
Center Tap Range	Taps 14–17																
CONCLUSION	Errors caused by –5% variation in supply voltage.																
S/N 2199, Speed Grade: -1																	
25°C, Nom Supplies	F	F	F	F	F	F	P	P	C	P	P	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F
Center Tap Range	Taps 12–14																
CONCLUSION	Errors caused by –5% variation in supply voltage.																

Table 18: **Measurement of Receiver Drift under Extreme Conditions at 1000 Mb/s *(Continued)***

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
S/N 001, Speed Grade: -2																	
25°C, Nom Supplies	F	F	F	F	F	F	P	P	C	P	P	P	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F
Center Tap Range	Taps 11–12																
CONCLUSION	Errors caused by –5% variation in supply voltage.																
S/N 002, Speed Grade: -2																	
25°C, Nom Supplies	F	F	F	F	F	P	P	P	C	P	P	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F
Center Tap Range	Taps 11–13																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 003, Speed Grade: -2																	
25°C, Nom Supplies	F	F	F	F	F	F	P	P	C	P	P	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F
Center Tap Range	Taps 13–14																
CONCLUSION	Errors caused by –5% variation in supply voltage.																

Table 18: **Measurement of Receiver Drift under Extreme Conditions at 1000 Mb/s *(Continued)***

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
S/N 004, Speed Grade: -3																	
25°C, Nom Supplies	F	F	F	F	F	P	P	P	C	P	P	P	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F
Center Tap Range	Taps 9–10																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 005, Speed Grade: -3																	
25°C, Nom Supplies	F	F	F	F	P	P	P	P	C	P	P	P	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, +5% Supplies	F	F	P	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F
Center Tap Range	Taps 11–12																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 006, Speed Grade: -3																	
25°C, Nom Supplies	F	F	F	F	P	P	P	P	C	P	P	P	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	P	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F
Center Tap Range	Taps 9–10																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																

Notes:

1. IODELAY taps, where "0" is the reference tap determined by the bit align machine at nominal voltage and 25°C.
2. P = Error-free transmission; F = Error in transmission; C = IODELAY tap position selected by bit-align machine under nominal conditions at 25°C.

Table 19: **Measurement of Receiver Drift under Extreme Conditions at 1100 Mb/s**

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
S/N 2194, Speed Grade: -1																	
25°C, Nom Supplies	F	F	F	F	F	F	P	P	C	P	P	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F
Center Tap Range	Taps 13–14																
CONCLUSION	Errors caused by –5% variation in supply voltage.																
S/N 2219, Speed Grade: -1																	
25°C, Nom Supplies	F	F	F	F	F	F	P	P	C	P	F	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	P	P	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	P	P	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F
Center Tap Range	Taps 6, 15–17																
CONCLUSION	Errors caused by ±5% variation in supply voltage.																
S/N 2199, Speed Grade: -1																	
25°C, Nom Supplies	F	F	F	F	F	F	F	P	C	P	F	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	P	P	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	P	P	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	P	P	F	F	F	F	F
Center Tap Range	Taps 13–15																
CONCLUSION	Errors caused by –5% variation in supply voltage.																

Table 19: **Measurement of Receiver Drift under Extreme Conditions at 1100 Mb/s *(Continued)***

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
S/N 001, Speed Grade: -2																	
25°C, Nom Supplies	F	F	F	F	F	F	P	P	C	P	P	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F
Center Tap Range	Taps 12–13																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 002, Speed Grade: -2																	
25°C, Nom Supplies	F	F	F	F	F	P	P	P	C	P	F	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F
Center Tap Range	Taps 13–14																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 003, Speed Grade: -2																	
25°C, Nom Supplies	F	F	F	F	F	F	F	P	C	P	F	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	P	P	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	P	P	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F
Center Tap Range	Taps 14–16																
CONCLUSION	Errors caused by –5% variation in supply voltage.																

Table 19: **Measurement of Receiver Drift under Extreme Conditions at 1100 Mb/s *(Continued)***

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
S/N 004, Speed Grade: -3																	
25°C, Nom Supplies	F	F	F	F	F	P	P	P	C	P	P	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F
Center Tap Range	Taps 9–10																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 005, Speed Grade: -3																	
25°C, Nom Supplies	F	F	F	F	F	P	P	P	C	P	P	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F
Center Tap Range	Taps 11–12																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 006, Speed Grade: -3																	
25°C, Nom Supplies	F	F	F	F	F	P	P	P	C	P	P	P	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	P	P	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	P	F	F	F	F
Center Tap Range	Taps 9–10																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																

Notes:

1. IODELAY taps, where "0" is the reference tap determined by the bit align machine at nominal voltage and 25°C.
2. P = Error-free transmission; F = Error in transmission; C = IODELAY tap position selected by bit-align machine under nominal conditions at 25°C.

Table 20: **Measurement of Receiver Drift under Extreme Conditions at 1200 Mb/s**

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
S/N 2194, Speed Grade: -1																	
25°C, Nom Supplies	F	F	F	F	F	F	F	P	C	F	F	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	F	P	P	F	F	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	F	P	P	F	F	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	F	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	P	F	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	F	F	F	F	F	F	F
Center Tap Range	Taps 13–15																
CONCLUSION	Errors caused by ±5% variation in supply voltage.																
S/N 2219, Speed Grade: -1																	
25°C, Nom Supplies	F	F	F	F	F	F	F	F	C	F	F	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	F	P	P	F	F	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	F	F	P	F	F	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	F	F	P	P	F	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
Center Tap Range	Taps 6–7, 16–17																
CONCLUSION	Errors caused by ±5% variation in supply voltage.																
S/N 2199, Speed Grade: -1																	
25°C, Nom Supplies	F	F	F	F	F	F	F	P	C	F	F	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	F	P	P	F	F	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	F	F	P	F	F	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
Center Tap Range	Taps 13–15																
CONCLUSION	Errors caused by ±5% variation in supply voltage.																

Table 20: **Measurement of Receiver Drift under Extreme Conditions at 1200 Mb/s *(Continued)***

Condition	IODELAY Taps [1]																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
S/N 001, Speed Grade: -2																	
25°C, Nom Supplies	F	F	F	F	F	F	F	P	C	P	F	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	P	F	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	P	F	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	P	F	F	F	F	F	F
Center Tap Range	Taps 12–13																
CONCLUSION	Errors caused by –5% variation in supply voltage.																
S/N 002, Speed Grade: -2																	
25°C, Nom Supplies	F	F	F	F	F	F	P	P	C	P	F	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	F	P	P	F	F	F	F	F	F
Center Tap Range	Taps 13–14																
CONCLUSION	Errors caused by ±5% variation in supply voltage.																
S/N 003, Speed Grade: -2																	
25°C, Nom Supplies	F	F	F	F	F	F	F	P	C	F	F	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	F	F	P	P	F	F	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	F	F	P	F	F	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	F	P	P	P	F	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	F	F	P	P	F	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
Center Tap Range	Taps 14–15																
CONCLUSION	Errors caused by ±5% variation in supply voltage.																

Table 20: **Measurement of Receiver Drift under Extreme Conditions at 1200 Mb/s *(Continued)***

Condition	IODELAY Taps (1)																
	–8	–7	–6	–5	–4	–3	–2	–1	0	+1	+2	+3	+4	+5	+6	+7	+8
S/N 004, Speed Grade: -3																	
25°C, Nom Supplies	F	F	F	F	F	F	P	P	C	P	F	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F	F
Center Tap Range	Taps 9–11																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 005, Speed Grade: -3																	
25°C, Nom Supplies	F	F	F	F	F	P	P	P	C	P	F	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	F	P	P	P	F	F	F	F	F	F
Center Tap Range	Taps 11–13																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																
S/N 006, Speed Grade: -3																	
25°C, Nom Supplies	F	F	F	F	F	P	P	P	C	P	F	F	F	F	F	F	F
0°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F
85°C, Nom Supplies	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F
25°C, +5% Supplies	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F	F
0°C, +5% Supplies	F	F	F	P	P	P	P	P	P	F	F	F	F	F	F	F	F
85°C, +5% Supplies	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F
25°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F
0°C, –5% Supplies	F	F	F	F	F	F	P	P	P	P	P	F	F	F	F	F	F
85°C, –5% Supplies	F	F	F	F	F	F	F	P	P	P	P	F	F	F	F	F	F
Center Tap Range	Taps 10–11																
CONCLUSION	Error free under all conditions when calibrated under nominal conditions to position C.																

Notes:

1. IODELAY taps, where "0" is the reference tap determined by the bit align machine at nominal voltage and 25°C.
2. P = Error-free transmission; F = Error in transmission; C = IODELAY tap position selected by bit-align machine under nominal conditions at 25°C.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/13/06	1.0	Initial Xilinx release.