XAPP905 (v1.0) August 25, 2005

Using CoolRunner-II with OMAP, XScale, i.MX & Other Chipsets

Introduction

Getting it Right Every Time

Consumer electronics product designs, such as cell phone handsets and MP3 players, typically are very high volume products. To that end, most product designers choose ASIC or ASSP methodologies to pack the greatest functionality into tiny, portable packages. This “hits the mark” for dense functionality, and usually has acceptable power consumption. But the consumer world is rapidly changing, so features envisioned at one point in time become quickly obsolete, as competitors must deliver differentiated solutions to seek greater market success. The term cutthroat is frequently used to describe this level of competition! Mistakes are not tolerated, and mistakes are expensive. Choosing the correct ASSP, or designing an ASIC correctly every time is nearly impossible. Mitigating these circumstances is crucial to sustaining market share, and that is where CoolRunner™-II CPLDs enter the picture.

CoolRunner-II CPLDs are the leading, low power, low price programmable solution for digital consumer designs today.

This discussion will show you ways to expand beyond the limitations of today’s ASIC/ASSP solutions, with simple, cost effective, low power programmable logic using CoolRunner-II CPLDs. As well, we will show solutions to some of the problems mentioned here, with links to application notes that give in-depth details.

Level Translation

Interfacing two chips of different voltage standards is a common problem. Every type of memory is not made at every voltage standard, and microprocessors are offered at many voltages. Matching standards can be as simple as introducing level translators, but they are expensive and take more area than might be desired. Using a CPLD is a better solution, and offers substantially greater flexibility. All Xilinx CoolRunner-II CPLDs are capable of translating between two voltages, and some can handle as many as four.

CoolRunner-II CPLD I/O banks easily translate between voltages ranging from 1.5 to 3.6V, in a single chip. But, this totally disregards the programmability of the devices. You get the translation as part of the whole package, which means you get a bundle of logic, flip flops, power reduction resources, and I/O buffers frequently priced below level translator chips! **XAPP785** explains the details on how you can take advantage of this powerful feature, to expand the capabilities of your OMAP, XScale or i.MX designs.

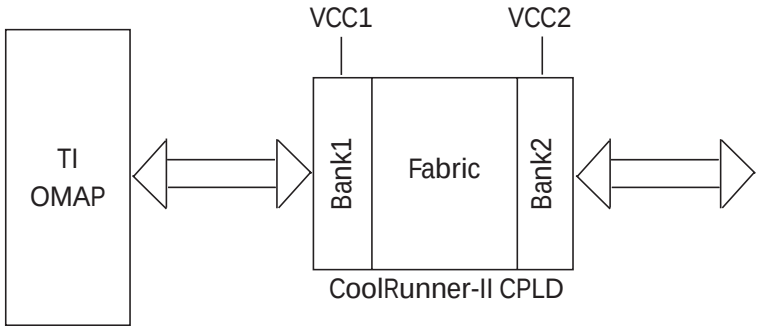

Figure 1: **CoolRunner-II Level Translation of TI OMAP Signals**

Pin Expansion

High pin count ASICs are more expensive than low pin count ASICs, in general. If your logic needs dictate a low capacity, but your I/O requirements dictate a high capacity, you may be paying for logic you will never use, to gain the pins. One solution to this is adding a CoolRunner-II CPLD to operate as a “pin expander”. The basic idea is to identify GPIO pins that typically operate at a slow speed. Then, rather than assign ASIC pins to them, attach CoolRunner-II CPLD pins to the slow moving GPIO signals, serialize the signals and import them to the ASIC on fewer net pins.

Serializing/deserializing is done through simple, efficient shifting, and can drop the pin counts dramatically on expensive ASICs. **XAPP799** shows how to do this through an I2C port, but other methods can be used.

As an alternate viewpoint, OMAP, XScale and i.MX processors provide specific pin mixes to support the applications their vendors deem appropriate. This doesn’t mean that you must agree, as a designer. CoolRunner-II pin expansion permits you to create your own GPIO pins, of assorted voltages and additional capabilities (pulsing, PWM, individually 3-stated). Increasing the effectiveness of your solution is our goal.

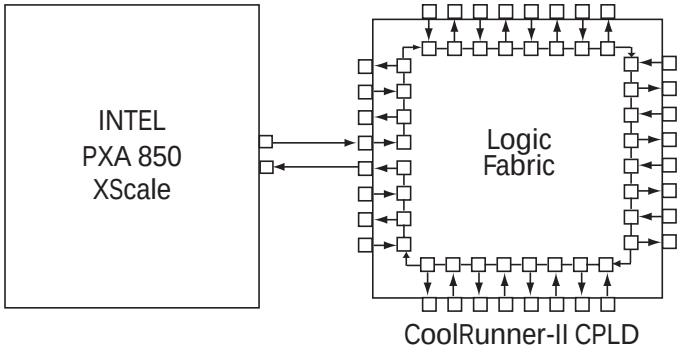

Figure 2: **CoolRunner-II Pin Expansion of XScale Processor**

Pin Swizzling

CPLDs offer the ability to rearrange your pinouts when PCB layout errors occur. This valuable quality is key to keeping you on schedule and within financial and power budgets.

Correcting misconnections on a board, without having to re-spin the PCB can shave weeks to months out of product schedules. CoolRunner-II CPLDs are built from powerful logic blocks using Programmable Logic Arrays, that can reassign pin logic “at will.” You will be amazed at how well these devices retain pinouts through multiple edits, yet permit re-assigning a design onto different pins as needed. The **CoolRunner-II Family data sheet** explains the architecture and points you to application notes that give all the detail you will need to understand the value of PLAs.

Power Control

Quick power up is one of the strengths of CPLDs. Containing their own configuration cells permits CoolRunner-II CPLDs to power up and direct the activities of other chips, as they subsequently arise. This includes some power regulators, which may be sequenced by the Coolrunner-II CPLDs, as well as other controlling signals that need to be well defined early in board operation. **XAPP436** describes some of these capabilities.

Power Reduction

XScale, OMAP and i.MX based chipsets all include some version of the ARM microprocessor. This is not a surprise. Advanced RISC Machines started early with developing low power methods to operate microprocessors, and subsequently, the licensing vendors have all added their own methods to further reduce processor power. Typical power reduction operations are: clock gating, voltage throttling and on board memory management to reduce transfers within the device. These are sometimes referred to as run, wait, doze, sleep, hibernate, and so on. Also, operating systems like Symbian have added “power awareness” to the mix, so that

unused resources can be parked in the lowest power mode possible for the current tasks being executed. This all works well and lowers processor power. However, lowering power in the rest of the system exceeds the scope of these methods. Enter CoolRunner-II CPLDs.

CoolRunner-II CPLDs are designed to be inherently low power parts. That is important, but alone is not enough. CoolRunner-II special features also can be used to lower the power in other devices. Using clock dividers and Xilinx's patented DataGATE™ technology can reduce power in many (if not all) of the chips on your design. **XAPP378** shows how to do this, and **WP227** shows just how much power you can save with DataGATE. Blocking power to other chips can also reduce electromagnetic fields being propagated on your board and emanating from your system. This powerful signal blocking technique can pay off in many ways!

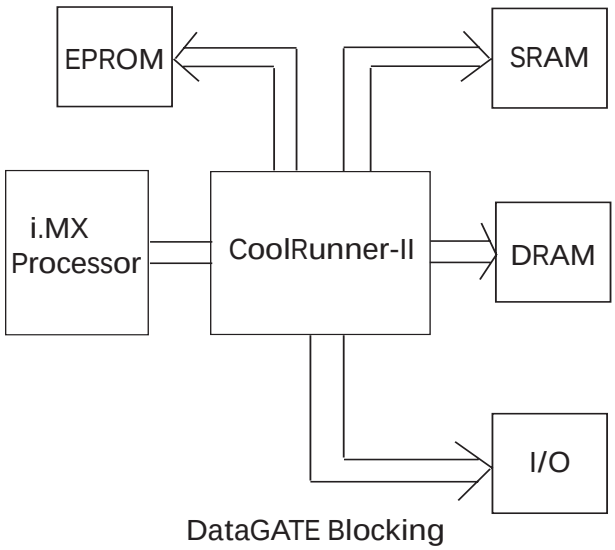

Figure 3: **DataGATE Blocking Extraneous Switching to Various Devices**

Logic Consolidation

Having three, two input AND gates, two three input OR gates and a Schmitt buffer package on your board can burden your bill of materials (BOM), eat away at your power and cost budgets, and lower your reliability. Collecting all that stray logic into a consolidated, low power CoolRunner-II not only solves these problems, but stores additional unused logic right there, on your board – ready to use with future improvements/edits. **WP214** shows what you can expect from collecting logic gates/flip flops into CoolRunner-II CPLDs. Table 1 summarizes the "burn rate" for logic.

Table 1: **Macrocell "Burn Rate" for Common TTL Functions**

Function	Macrocells	P-terms	Flip-Flops
Shift register (simple)	1 per bit	1 per bit	1 per bit
Counter (simple)	1 per bit	1 per bit	1 per bit
2:1 Mux	1	2	0
4:1 Mux	1	4	0
8:1 Mux	1	8	0
8 bit loadable shifter	8	16	8
8 bit loadable/SL/SR shifter	8	24	8
8 bit loadable counter	8	16	8
8 bit load/up/dn counter	8	24	8

Table 1: **Macrocell "Burn Rate" for Common TTL Functions**

Function	Macrocells	P-terms	Flip-Flops
Full Adder / bit	2	7	0/1 (optional)
2:4 Decoder	4	4	0
3:8 Decoder	8	8	0
4:16 Decoder	16	16	0
8 bit Equality Comparator	1	16	0
And/Nand gate (1-40 inputs)	1	1	0
Or/Nor gate (1-40 inputs)	1	11	0
Ex-or/Ex-nor (2-3 inputs)	1	2-3	0
Level translator (per bit)	1	1	0

Additional Information

CoolRunner-II Data Sheets and Application Notes

Conclusion - The Future

CoolRunner-II CPLDs are quickly becoming the standard for low power, low cost, high volume, handheld consumer products. This application note has focused on how these powerful products can make life easier when building systems with OMAP, XScale and i.MX processors, but CoolRunner-II works just as well with many other processors, to add functionality, save power and get products to market fast.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/25/05	1.0	Initial Xilinx release.