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Connecting Intel PXA27x Processors to Hard-Disk Drives with a CoolRunner-II CPLD

Summary

With the increasing functionality of modern handheld devices, greater storage capacity requirements become very important. The Intel PXA27x Processor Family is very popular and is used in many high end cell phones and PDAs. In order to support the higher storage capacity associated with hard-disk drives (HDD), Intel published the application note, *Connecting the Intel PXA27x Processor Family to a Hard-Disk Drive via the VLIO Memory Interface*.

The Variable Latency I/O (VLIO) interface solution only requires a small number of additional components and produces low-cost and efficient Direct Memory Access (DMA) performance. The Xilinx CoolRunner-II™ CPLD is the ideal solution to bridge the Intel processor to an HDD without the need of other components.

Introduction

The Intel application note provides detailed suggestions for connecting a CompactFlash, true IDE mode, parallel ATA, HDD to a PXA27x processor using a VLIO memory interface. Configurations using Programmed I/O (PIO) and flow-through DMA are presented. The HDD in this application note is assumed to be using 3.3V logic. The PXA27x processor is assumed to be running a 1.8V memory bus, so level shifting is used to buffer logic to and from the HDD interface logic.

With the introduction of the XC2C32A and XC2C64A CPLDs, the Xilinx CoolRunner-II Family becomes the ideal solution to address the need of the level shifting for this application. The XC2C32A, XC2C64A, XC2C128, and XC2C256 CPLD devices have two banks each, and the XC2C384 and XC2C512 devices have four banks each. This means that the V_{CCIO} can be powered at 3.3V on one bank to interface to the HDD, and at 1.8V on the other bank to interface to PXA27x processor. The supported I/O standards for the CoolRunner-II device can be seen in Table 1 below. More information about level translation using Xilinx CoolRunner-II CPLDs can be found in **XAPP785**.

Table 1: **Supported I/O Standards in CoolRunner-II Family**

IOSTANDARD Attribute	Output V_{CCIO}	Input V_{CCIO}	Input(1) V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS33	3.3	3.3	N/A	N/A
LVCMOS25	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
LVCMOS15(2)	1.5	1.5	N/A	N/A
HSTL_1(2)(3)	1.5	1.5	0.75	0.75
SSTL2_1(2)(3)	2.5	2.5	1.25	1.25
SSTL3_1(2)(3)	3.3	3.3	1.5	1.5

1. Input V_{REF} details given in individual data sheets.
2. Requires the use of Schmitt-trigger inputs.
3. HSTL_1, SSTL2_1, and SSTL3_1 on devices of 128 macrocells and above.

PXA27x

Mapping Intel PXA27x Processors to True IDE CompactFlash Interfaces

Figure 1 shows a block diagram of a CompactFlash connection to the PXA27x processor VLIO interface in true IDE PIO mode. This diagram describes the mapping of the CompactFlash true IDE signals to the PXA27x processor.

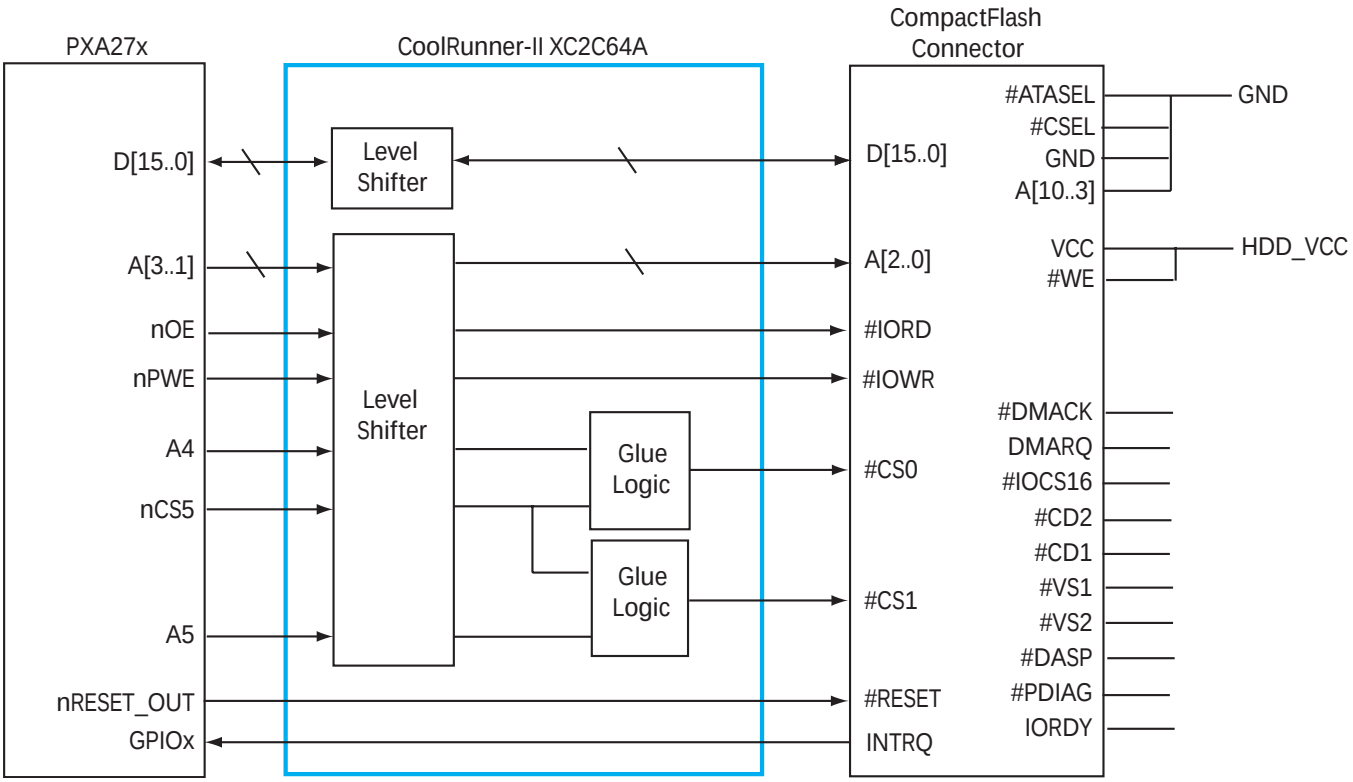

Figure 1: **True IDE PIO Block Diagram**

This design uses two address lines and nCS5 of the PXA27x to get the two chip select signals the HDD needs. Table 2 shows the relationship of the PXA27x processor nCS5 memory mapping to the HDD CS0# and CS1# signals.

Table 2: **Memory Mapping**

nCS5	A4	A5	CS0#	CS1#	R/W Field	Address
0	0	1	0	1	Task File Register	0x1400_0020
0	1	0	1	0	CTL Register	0x1400_0010
0	1	1	1	1	DMA	0x1400_0030
1	x	x	1	1	N/A	N/A

Timing Considerations

The PXA27x VLIO interface is designed to interface to high speed memory devices, such as Flash and SRAM. This capability requires attention to timing parameters. Analysis of HDD vendor devices shows that the “CS Valid to IIORD/IOWR” is close to the specified limits of the PXA27x processor. It may be necessary to perform timing analysis and use glue logic to adjust the timing to meet the HDD timing requirements.

As you can see from Figure 1, the glue logic for memory mapping and level shifting functions can be easily integrated into a single XC2C64A CPLD. And the CoolRunner-II family’s

programmable logic array can be flexibly designed and programmed to meet the timing requirements for this application.

Conclusion

Xilinx CoolRunner-II CPLDs are the ideal solution for applications requiring level translation. This application connects Intel's PXA27x processor to a hard disk drive. integrating level shifting and glue logic for memory mapping into a single XC2C64A CPLD.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/15/06	1.0	Initial Xilinx release.