Xilinx Broadest Cost Effective All Programmable Low-End Portfolio

Introduction

All programmable, cost-sensitive applications have reached new levels of sophistication and diversity of requirements. Low-cost systems for the consumer, automotive, industrial, medical, and communications space may need a programmable logic device for high serial bandwidth, advanced processing, or simply for bridging functionality and little else. Commonly termed the "low-end" market due to the devices' relatively low cost and density, these platforms provide varying levels of system integration, performance, and power. They may need to perform critical tasks such as video analytics or packet processing, or simply expand a system's I/O connectivity to peripheral devices.

Due to the broad range of application needs, a single low-end product at a single process node is no longer an "ideal fit for all." A developer does not necessarily need superior performance-per-watt for simple interconnect logic functionality, and an application that demands advanced analytics as opposed to serial bandwidth should not carry the cost burden of unused transceivers. There are trade-offs to deliver the right value per application, and there cannot be a "catch all" platform that delivers everything to everyone.

For this reason, Xilinx delivers the broadest cost effective, All Programmable Low-End Portfolio that delivers the best value for a given application. Specifically, the Xilinx® Spartan®-6 FPGAs deliver I/O optimization; Artix®-7 FPGAs provide transceiver optimization; and Zynq®-7000 All Programmable SoCs (Z-7010, Z-7015, and Z-7020) deliver system integration and optimization for system-on-chip (SoC) applications.

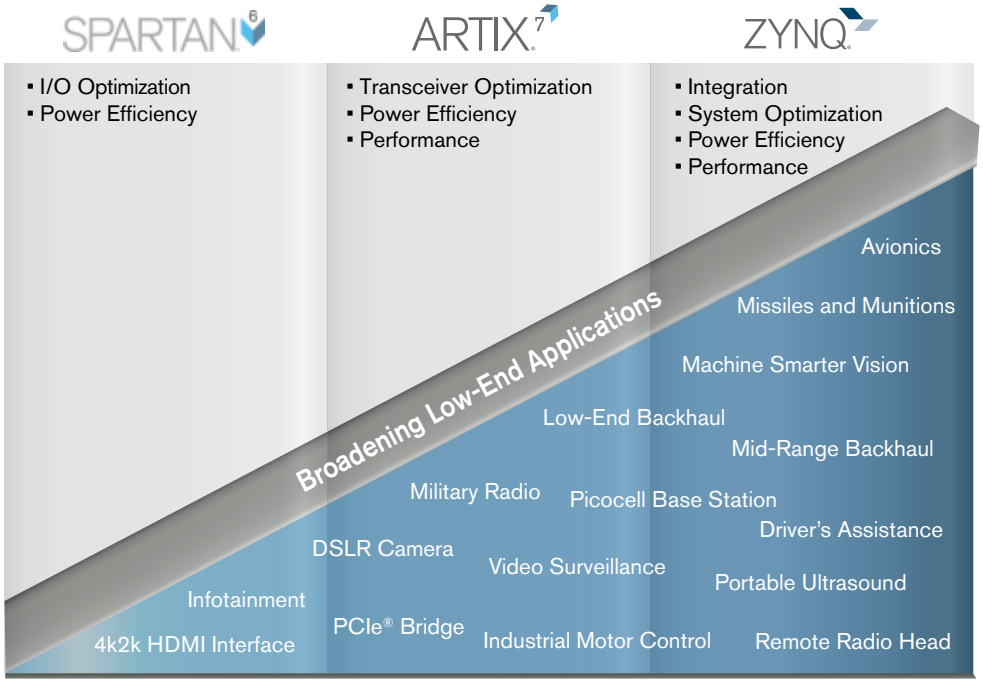

Figure 1: Expanding application set for low-end devices

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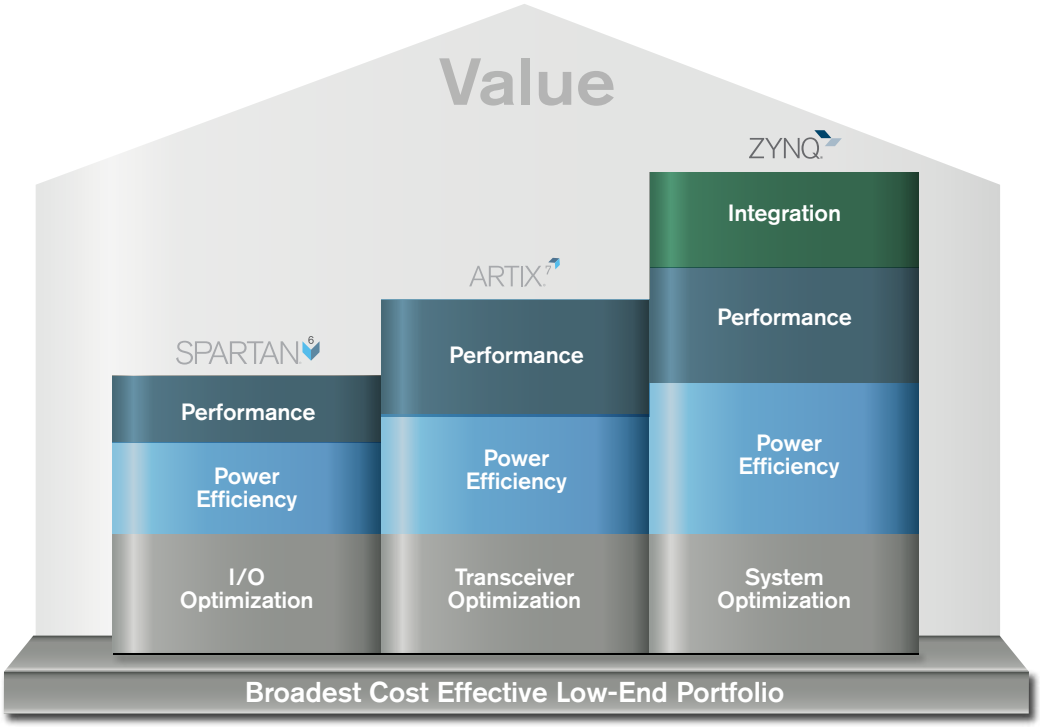

Figure 2: Each device family delivers the right value for its target applications

Spartan-6 FPGA for I/O Optimization

I/O optimization, while considered the simplest of functions, still requires a capable platform. While bridging logic may demand embedded memory, DSPs, and other hardened blocks, typically, the most important factor is high pin count and low cost.

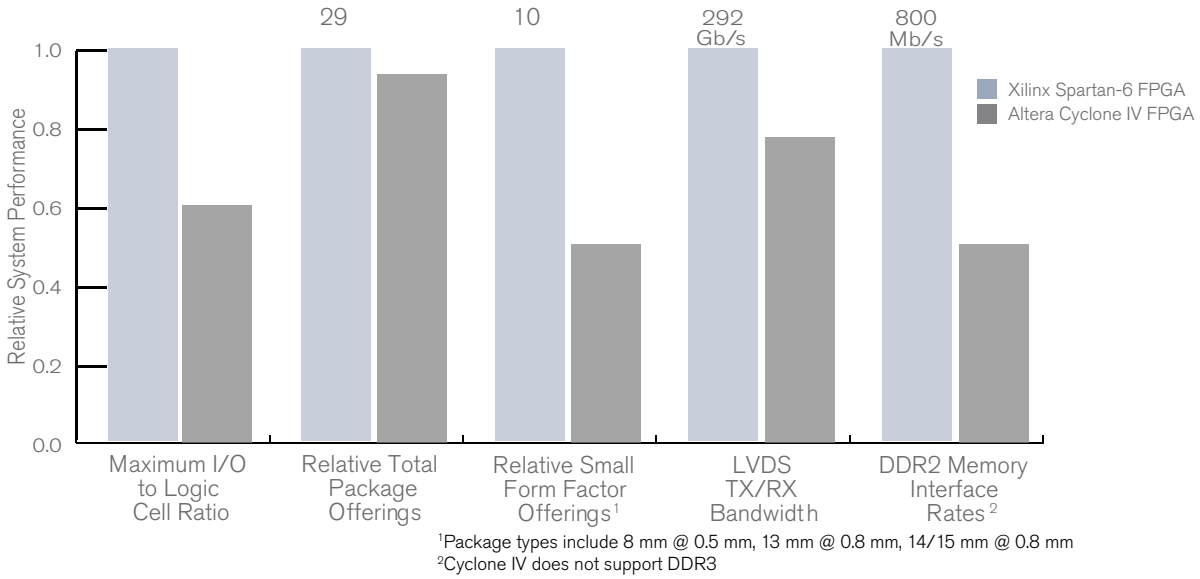

Figure 3: Spartan-6 FPGA family provides best-in-class I/O and packaging features

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Based on Samsung's 45 nm low power (LP) process, the Spartan-6 family is the industry's low cost leader and an ideal fit for simple to moderately complex glue logic designs commonly found in a range of applications that includes infotainment, consumer and industrial automation. Because it is biased towards raw connectivity, the Spartan-6 family has best-in-class I/O and form-factor related features:

- Maximum I/O to logic cell ratio
- Most relative total package offerings
- Smallest form-factor offerings
- Fastest parallel I/O performance with LVDS
- Fastest memory interface rates (including DDR3)

With these capabilities, Spartan-6 FPGAs offer a targeted solution for chip-to-chip interfaces and memories while supporting more than 40 interface protocols and true 3.3V I/O standards with full undershoot/overshoot protection. Such features make the Spartan-6 FPGA the device of choice for I/O optimization. A partial list of supported I/O standards, is shown below. For more information on supported I/O standards, visit www.xilinx.com/spartan6.

I/O Type	I/O Standards
Simple Single Ended	LVTTL, LVCMOS, JEDEC
Simple Interfaces	I2C, PCI33
Differential Interfaces	LVDS, RSDS, Mini-LVDS, LVPECL
Emerging Interfaces	TMDS, PPDS, Diff HSTL, Diff SSTL
Memory Interfaces	DDR, DDR2, DDR3, LP DDR
High Speed Serial Interfaces	PCI Express, 1G Ethernet, Aurora, EPON, GPON, DisplayPort, XAUI, CPRI/OBSAI, SRIO, SATA, V-by-One, Triple Rate SDI

Table 1: Protocols supported by Spartan-6 FPGAs (subset)

The Spartan-6 family also features advanced logic fabric that meets the power requirements for many cost-sensitive systems. Using process and architectural innovations at 45 nm, Spartan-6 FPGAs deliver power efficiencies that include power management modes (e.g., suspend, hibernate, stop clock, multi-pin wake-up) and voltage scaling options.

Artix-7 FPGA for Transceiver Optimization

Based on TSMC's 28 nm high performance, low power (HPL) process, the Artix-7 family delivers the industry's most optimized transceivers, lowest power, and highest performance. This family is the perfect fit for low-end applications needing high end features. The Artix-7 family is the industry's low-end leader in nearly every measure of performance and bandwidth:

- Up to sixteen 6.6 Gb/s transceivers
- Highest aggregate serial bandwidth
- Maximum memory line rate
- Maximum LVDS I/O bandwidth
- Highest signal processing bandwidth
- Highest embedded memory F_{MAX}
- Highest logic fabric performance

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Perhaps the most important distinction of the Artix-7 family within the Xilinx All Programmable Low-End Portfolio is its high performance, low power transceivers. With over 6 Gb/s line rates, not only are these the smallest and fastest transceiver-based devices in the industry (available in 10x10 mm packaging), but the transceivers support advanced features such as pre-emphasis and continuous time linear equalization (CTLE) to compensate for signal distortion across transmission channels. Artix-7 FPGAs are also the only low-end FPGAs to offer an on-chip scope (2D Eye Scan) to measure signal integrity. With its massive serial throughput (211 Gb/s), the Artix-7 family is an ideal low-cost alternative for bandwidth-sensitive applications that would otherwise require mid-range solutions. With these line rates, applications such as networking, wireless, and medical imaging can take advantage of the fact that the Artix-7 family supports the latest connectivity standards, such as RXAUI, 6.144 CPRI, and JESD204B.

The device's logic and embedded resources offer the ideal balance of power and performance for "high-end applications at the low end." The RAM-to-logic and DSP-to-logic ratios are the highest in their class, on par with the processing capabilities of many mid-range products. The DSP bandwidth in particular makes the family useful for wireless communications and portable medical imaging. The Artix-7 FPGA also features analog mixed signal integration for functions ranging from simple system monitoring to more signal- processing-intensive tasks.

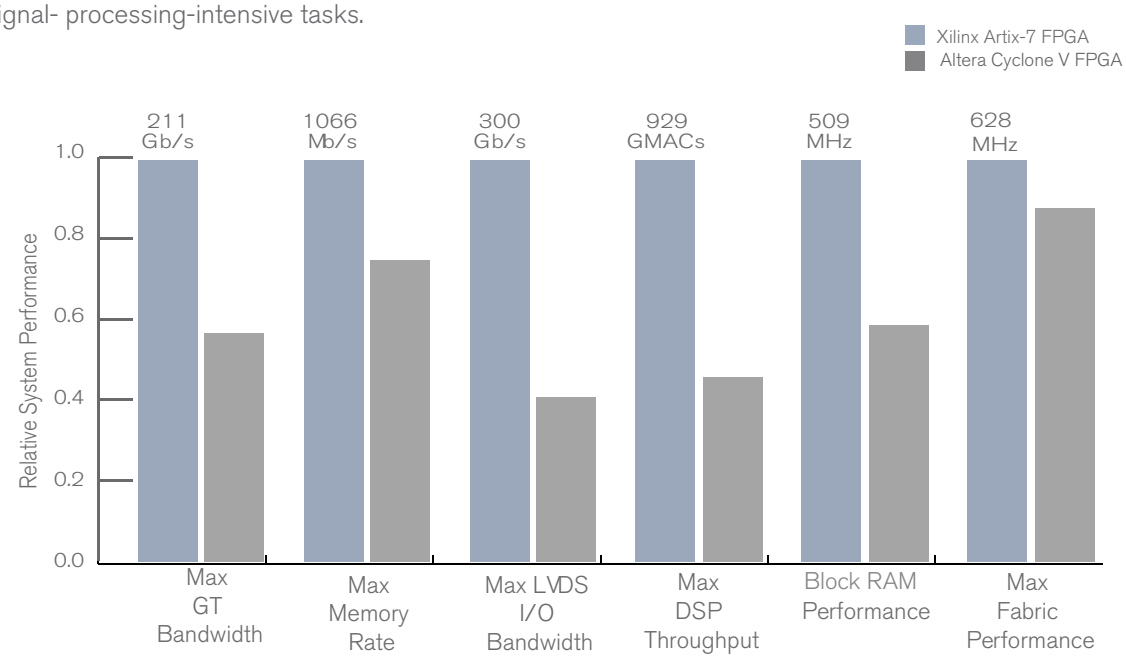

Figure 4: This Artix-7 FPGA family is the bandwidth leader in every category

The Zynq Platform for System Integration and Optimization

In contrast to the applications enabled by the Artix-7 FPGA family, there are many systems that need a different type of value—more than just high bandwidth, but intelligent processing and analytics to provide the highest system optimization. These needs are most ideally met by a processor-based all programmable SoC to deliver maximum system integration—which includes software, hardware, analog mixed signal, and connectivity within the platform and to external devices.

Perhaps the most diversely capable device of the portfolio is the Zynq-7000 All Programmable SoC family, which addresses this breed of applications, demanding processor-based analytics and imaging such as intelligent driver's assistance, broadcast cameras, industrial motor control, and other vision-based systems. The Zynq-7000 All Programmable SoCs (Z-7010, Z-7015, and Z-7020) are based on a fast processor system (PS) consisting of a dual core ARM® Cortex™-A9 processor fused with the Artix-7 FPGA's programmable logic (PL). Within the PS, the dual core Cortex-A9 achieves the lowest latency possible between on-chip memory and hardened I/O peripherals—key for coherent acceleration applications. The ARM® AMBA® AXI interfaces also enable the most optimized interconnect between PL and PS, allowing for massive FPGA parallel processing and acceleration of key algorithms.

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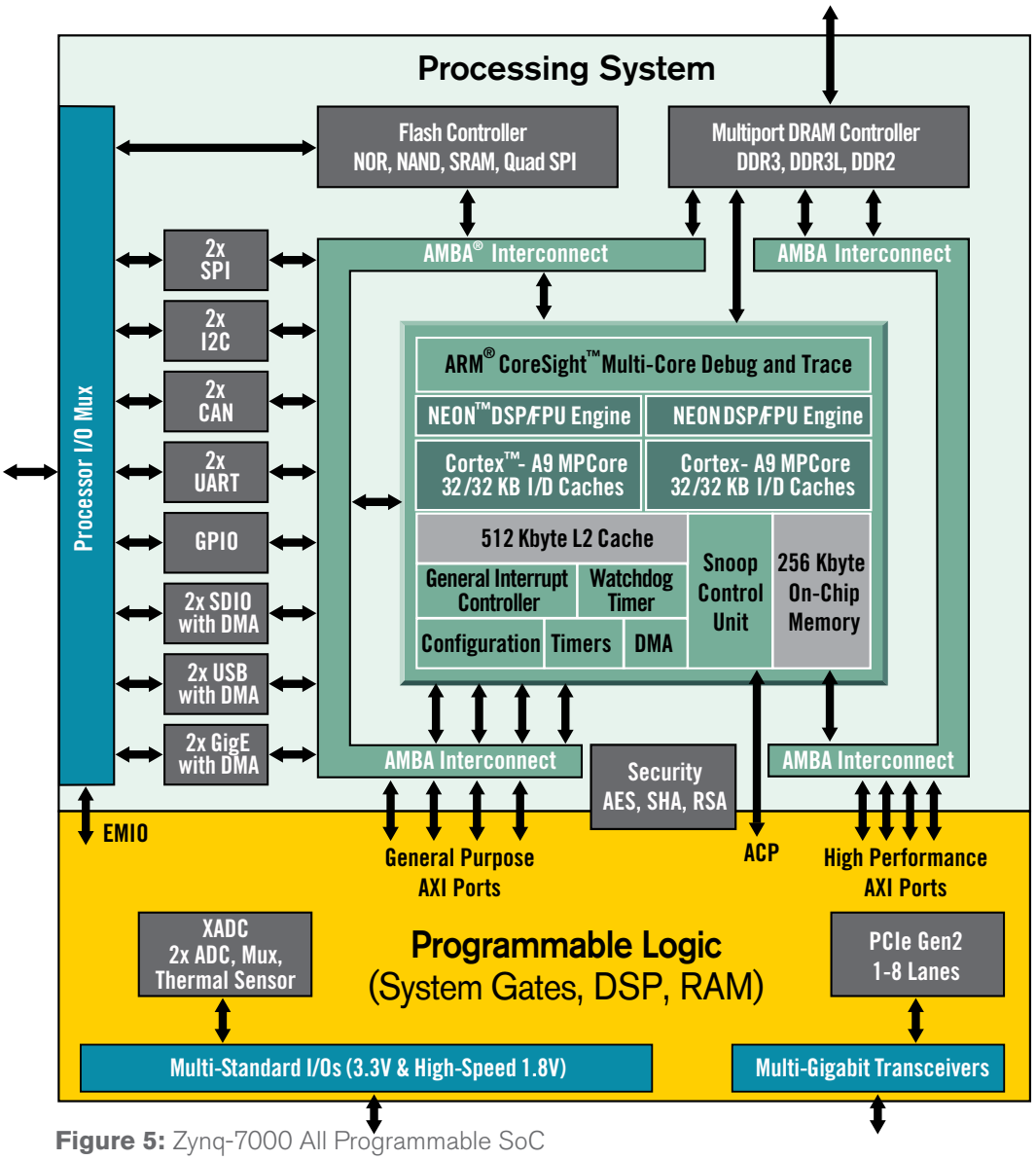

Figure 5: Zynq-7000 All Programmable SoC

Among the many industry leading advantages of the Zynq-7000 All Programmable SoCs (Z-7010, Z-7015, and Z-7020) are:

- Fastest overall processing system performance
- The largest and highest performance memory system
- Largest portfolio of IP, design kits, and reference designs
- Most extensive OS, middleware, and stack ecosystem
- Highest level of security (and reliability)

The essence of the Zynq platform is system integration and optimization. Because of the flexibility of the platform, the integration

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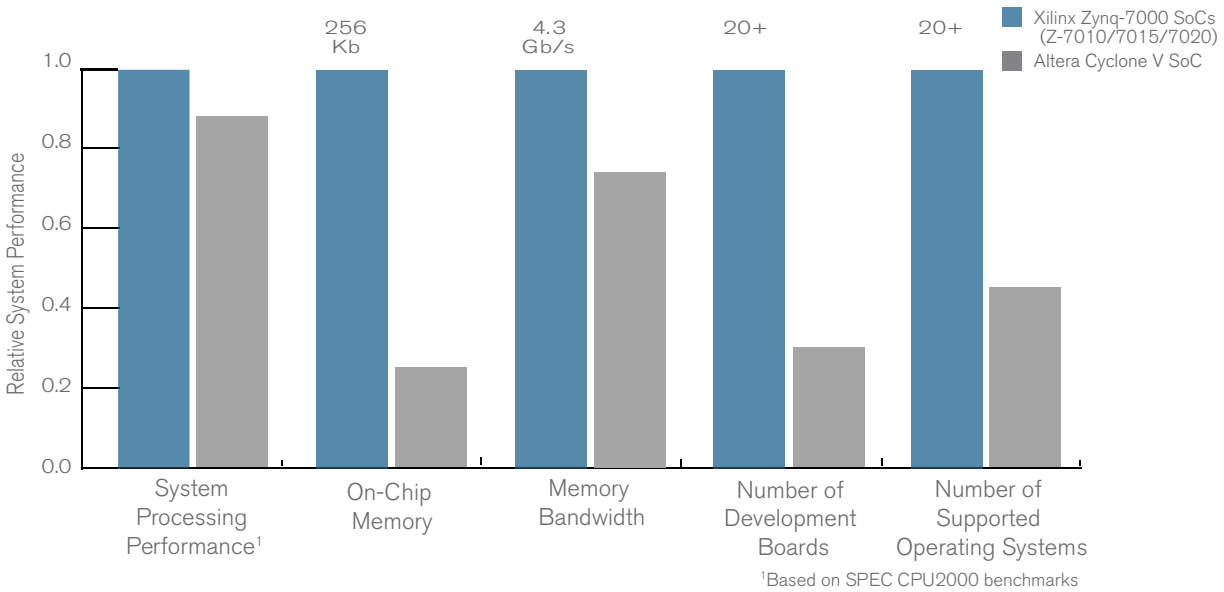

Figure 6: The Zynq platform leadership in system integration and optimization

can be leveraged beyond the original application to derivative products in adjacent markets. The integration itself has positive downstream effects on cost, system performance, and power. In multi-camera driver's assistance for example, the platform integrates typical sensing, environment characterization, and decision-making capabilities in a single device—reducing BOM cost and lowering system power, while boosting performance compared to traditional multi-chip solutions.

Because security and reliability are critical to integrated systems in applications like networking, aerospace, and defense—and becoming more important to industrial and medical devices—the Zynq All Programmable SoC family ensures trust, information assurance, and anti-tamper on the entire system. The processor also offers a secure boot operation that supports user authentication (RSA), encryption (AES-256), and data authentication (HMAC).

Delivering the Best Value at the Low End

Cost-sensitive applications can be just as specialized as their high-end counterparts. The requirements at the low end have become as dynamic and segmented as the entire programmable device market was several years ago. The portfolio offering must keep up with this level of diversity.

Xilinx offers the broadest cost effective portfolio optimized for the performance needs of diverse markets. While the classic domain of the low end, bridging applications have pushed the envelope in terms of I/O connectivity and foot print requirements. The Spartan-6 family has the industry's best I/O optimization and continues to lead in this category. On the other end of the spectrum, leading edge applications at the low end demand advanced logic and serial bandwidth capabilities. The Artix-7 FPGA family delivers transceiver optimization. And finally, levels of system integration and optimization not thought possible several years ago are now viable with the processor-centric Zynq-7000 All Programmable SoCs, enabling CPU, ASIC, ASSP, and programmable logic functionality fused on a single device. Collectively, the Spartan-6 FPGA, Artix-7 FPGA, and Zynq-7000 All Programmable SoC families redefine the low end for this generation and beyond for all programmable design.

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Take the Next Step

Read the All Programmable Low-End Portfolio Brief

Read the technology white papers:

Spartan-6 FPGA: WP396 High-Volume Spartan-6 FPGAs: Performance and Power Leadership by Design

Artix-7 FPGA: WP423 Reducing System Power and Cost with Artix-7 FPGAs

Zynq-7000 All Programmable SoCs: Zynq-7000 All Programmable SoC Backgrounder

See the full selection of boards and kits targeting low-end designs

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