Sheet#	Rev#	Description
1	6	Notes Page
2	2	Top Hierarchical Block Diagram
3	2	Clock Sources: Epson EC2121CA-166M OSC, SMA's
4	2	SystemAce Controller & CF Socket, JTAG Conn.
5	2	DDR-1 Micron MT46V16M16P-75 - MEM Top
6	1	DDR-1 Mem Top Termination Resistors
7	3	DDR-1 Micron MT46V16M16P-75 - MemL 01
8	1	DDR-1 MemL 01 Termination Resistors
9	2	DDR-1 Micron MT46V16M16P-75 - MemL 23
10	1	DDR-1 MemL 23 Termination Resistors
11	2	DDR-1 Micron MT46V16M16P-75 - MemL 45
12	1	DDR-1 MemL 45 Termination Resistors
13	2	DDR-1 Micron MT46V16M16P-75 - MemL 67
14	3	DDR-1 MemL 67 Termination Resistors
15	3	DDR-1 SODIMM 200-pin Socket "Right"
16	1	DDR-1 SODIMM Termination Resistors
17	1	LCD I/F Connector, MC74LCX541D level shifters, 7-Segment Display
18	2	RS232 I/F MAX3316ECUP 2.5V & DB9F Serial Conn (entire pages is DNA)
19	2	3S1500FG676 BANK0 MemL A[12:0] I/F, SYSCLK INPUT, 2XHEADER I/F ,Vcco=+2.5V
20	2	3S1500FG676 BANK1 Mem Top I/F, Vcco=+2.5V
21	2	3S1500FG676 BANK2 SODIMM Socket I/F, Vcco=+2.5V
22	2	3S1500FG676 BANK3 SODIMM Socket I/F, Vcco=+2.5V
23	2	3S1500FG676 BANK4 SODIMM Socket I/F, SYSACE I/F, Vcco=+2.5V
24	2	3S1500FG676 BANK5 LCD I/F, RS232 I/F, Vcco=+2.5V
25	2	3S1500FG676 BANK6 MemL I/F, Vcco=+2.5V
26	2	3S1500FG676 BANK7 MemL I/F, Vcco=+2.5V
27	4	3S1500FG676 Config Bank, XCONFIG Conn., Mode Sw, Prog PB Sw
28	2	3S1500FG676 Power Pins: GND, Vccaux (+2.5V), Vccint (+1.2V)
29	2	Power: +2.5V, +1.25V_Vtt, +1.25V_DDR1
30	5	Power: +3.3V, +1.2V_Vccint, +1.25V_FPGA
31	2	Decoupling Caps: +1.25V_Vtt, +1.25V_FPGA, +1.25V_DDR1
32	6	Decoupling Caps: +5V, +3.3V, +2.5V, +1.2V_Vccint
33	6	Rev. Notes

Revision Notes are on Sheet 33

Highest Ref. Des. #:

C452	Q5
D12	R738
DD1	SW6
J6	U14
L4	
P42	Y2

Notes Page

Latest Schematic Rev.: 6, on Date 03/15/2005

Title: Spartan3 DDR-1 Interface Board		
Size: B	Document Number: 0381177	Rev: 6
Date: Tuesday, March 15, 2005	Sheet 01 of 33	

4 x 16-bit DDR-1 Mem
on the Left are designated:
MEMB = MEM DQS(0:1)
MEMC = MEM DQS(2:3)
MEMD = MEM DQS(4:5)
MEME = MEM DQS(6:7)

DDR1_Top

DDR1_Left

3S1500FG676

SPARTAN3

SODIMM_Right

SODIMM_RIGHT

LCD

Seiko L167100J000

POWER_IF

RS232_DRIVER

CLOCKS

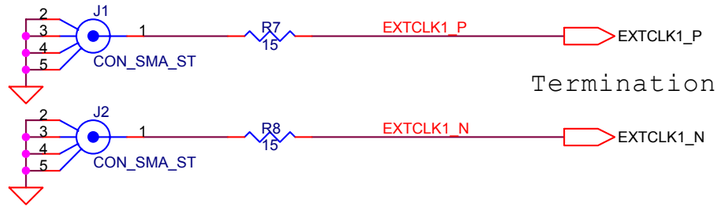
CONFIG EEPROM

SystemAce

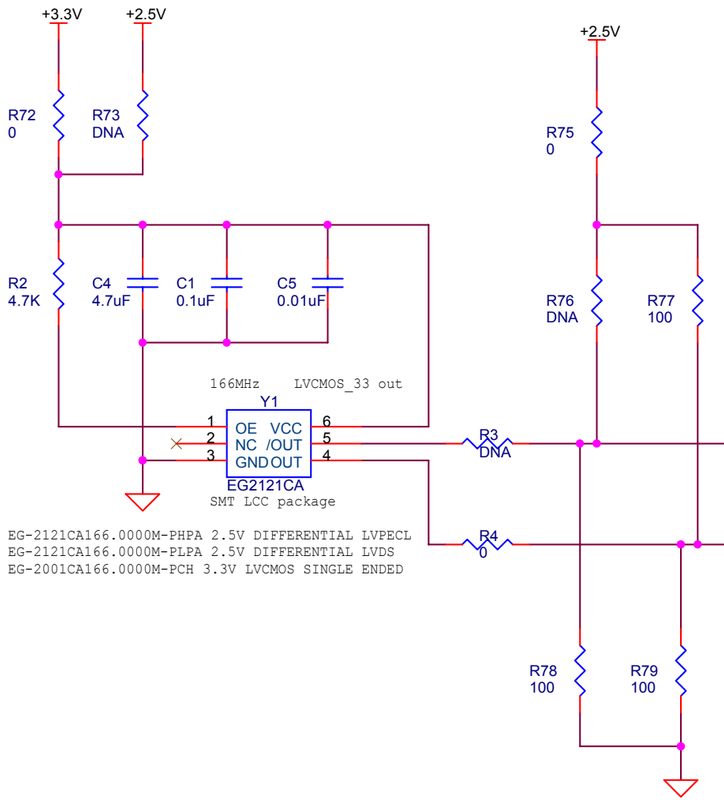
Spartan3 DDR-1 Board Top

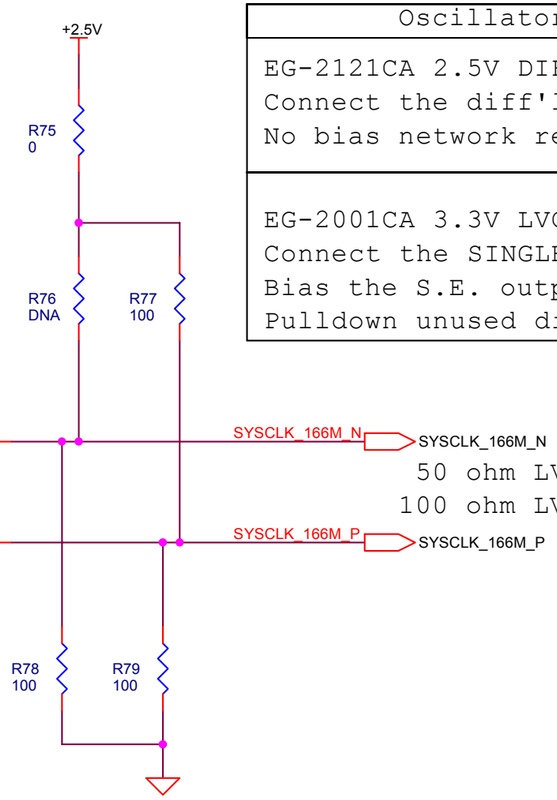
Title	Spartan3 DDR-1 Interface Board	
Size B	Document Number 0381177	Rev 2
Date: Monday, January 31, 2005	Sheet 02 of 33	

Differential Inputs for Test Equip. clock



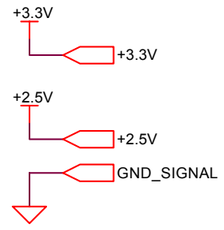
Termination resistors at FPGA Bank4 (Sheet 23)





Oscillator	Osc. Power	Resistor Configuration
EG-2121CA 2.5V DIFF'L LVPECL Connect the diff'l P & N outputs No bias network required	+2.5V	R73 0 ohms R72 DNA R4 0 ohms R3 0 ohms R76, R77, R78, R79 all DNA
EG-2001CA 3.3V LVCMOS SINGLE ENDED Connect the SINGLE ENDED "P" output Bias the S.E. output to 2.5V center Pulldown unused diff'l N clock sig	+3.3V	R72 0 ohms R73 DNA R4 0 ohms R3 DNA R77 100 ohms R79 100 ohms R78 100 ohms

50 ohm LVPECL term. R's at FPGA Bank0 (Sheet 19)
100 ohm LVDS parallel term. R at FPGA Bank0 (Sheet 19)



CLOCKS

Title: Spartan3 DDR-1 Interface Board			
Size: B	Document Number: 0381177		Rev: 2
Date: Monday, January 31, 2005	Sheet 03 of 33		

CONFIG via SystemAce CF

U10 — SystemAce Controller (TQFP144)

SYSACE_CLK 2.5V signal excursion constraint R's (copied from ML300 pcb)

+3.3V, +2.5V

R17 4.7K
R24 100
C7 4.7uF
C8 0.1uF
C9 0.01uF
R25 100
R26 15
SYSACE_CLK

Y2 33.0000MHz
SG-8002CA 3.3V CMOS
OE, VDD, GND, OUT

16-bit mode not supported

SYSACE_MPD[7:0] ↔ MPD15 MPD14 MPD13 MPD12 MPD11 MPD10 MPD09 MPD08 MPD07 MPD06 MPD05 MPD04 MPD03 MPD02 MPD01 MPD00

SYSACE_MPA[6:0] ↔ MPA06 MPA05 MPA04 MPA03 MPA02 MPA01 MPA00

SYSACE_MPBRDY ↔ MPBRDY
SYSACE_MPIRQ ↔ MPIRQ
SYSACE_MPWE_B ↔ MPWE#
SYSACE_MPOE_B ↔ MPOE#
SYSACE_MPCE_B ↔ MPCE#
SYSACE_CLK ↔ CLK

NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11 NC12 NC13 NC14 NC15 NC16 NC17 NC18

VCCL1 VCCL2 VCCL3 VCCL4 VCCL5 VCCL6 VCCL7 VCCL8 (+2.5V)
P9 P10 P11 P12 P13 P14 P15 P16 (+3.3V)
RESET# POR_BYPASS POR_TEST POR_RESET

SW1 SW PUSHBUTTON
R9 4.7K
MOM. PB FOR SysAce RESET

CFD15 CFD14 CFD13 CFD12 CFD11 CFD10 CFD09 CFD08 CFD07 CFD06 CFD05 CFD04 CFD03 CFD02 CFD01 CFD00
CFA10 CFA09 CFA08 CFA07 CFA06 CFA05 CFA04 CFA03 CFA02 CFA01 CFA00
CFCE2# CFCE1# CFCD2# CFCD1#
CFREG# CFWAIT# CFGRSVD
CFWE# CFOE#
ERRLED STATLED
NC19 NC20 NC21 NC22 NC23 NC24 NC25

J3 — CF_Socket

D15 D14 D13 D12 D11 D10 D09 D08 D07 D06 D05 D04 D03 D02 D01 D00
A10 A09 A08 A07 A06 A05 A04 A03 A02 A01 A00
CE2# CE1# CD2# CD1#
REG# WAIT# RDY/BSY#
WE# OE#

VCC1 VCC2 (+3.3V)
IORD# IOWR# — R27 1K, R28 1K
BVD2 BVD1 VS2# VS1# WP INPACK#
MH1 MH2 MH3 MH4 MH5 MH6 MH7 MH8 MH9 MH10
CSEL# RESET — R30 1K, R29 1K
GND1 GND2

+2.5V
+3.3V
GND_SIGNAL

R31 4.7K
RED D2, BLUE D1
R15 1K, R14 1K

P39 SysAce ERR LED Enable = ON
P39 HEADER 1x2

HALT_B

HDR_7x2_2MM P3

HEADER 8X2 P1
R164 7K, R184 7K, R194 7K, R204 7K, R214 7K, R224 7K, R23 DNA
SYSACE_TSTTDO SYSACE_TSTTDI SYSACE_TSTTCK SYSACE_TSTTMS HALT_B POWER_IS_ON TRST_B → TRST_B
DNA

CFPROG# goes to PROG_B
CFGINIT# comes from INIT_B

SYSACE_CFGINIT_B
SYSACE_CFGPROG_B
CFPROG = O.C. output

R11 4.7K, R12 4.7K, R13 4.7K
CFGINIT# CFGPROG# CFGTDO CFGTMS CFGTCK CFGTDI CFGADDR2 CFGADDR1 CFGADDR0 CFGMODEPIN TSTTDO TSTTMS TSTTCK TSTTDI
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14 GND15 GND16 GND17 GND18

SystemAce_Controller

R32 4.7K, R33 4.7K, R10 4.7K

SYSACE_TDO — R306 0
TMS — R307 0
TCK — R308 0
FPGA_TDO — R309 0

SW2 SysAceAddr_RotarySW

Disable SysAce after RESET

P2 HEADER 1x2

SYSACE_TSTTDI SYSACE_TSTTCK SYSACE_TSTTMS SYSACE_TSTTDO

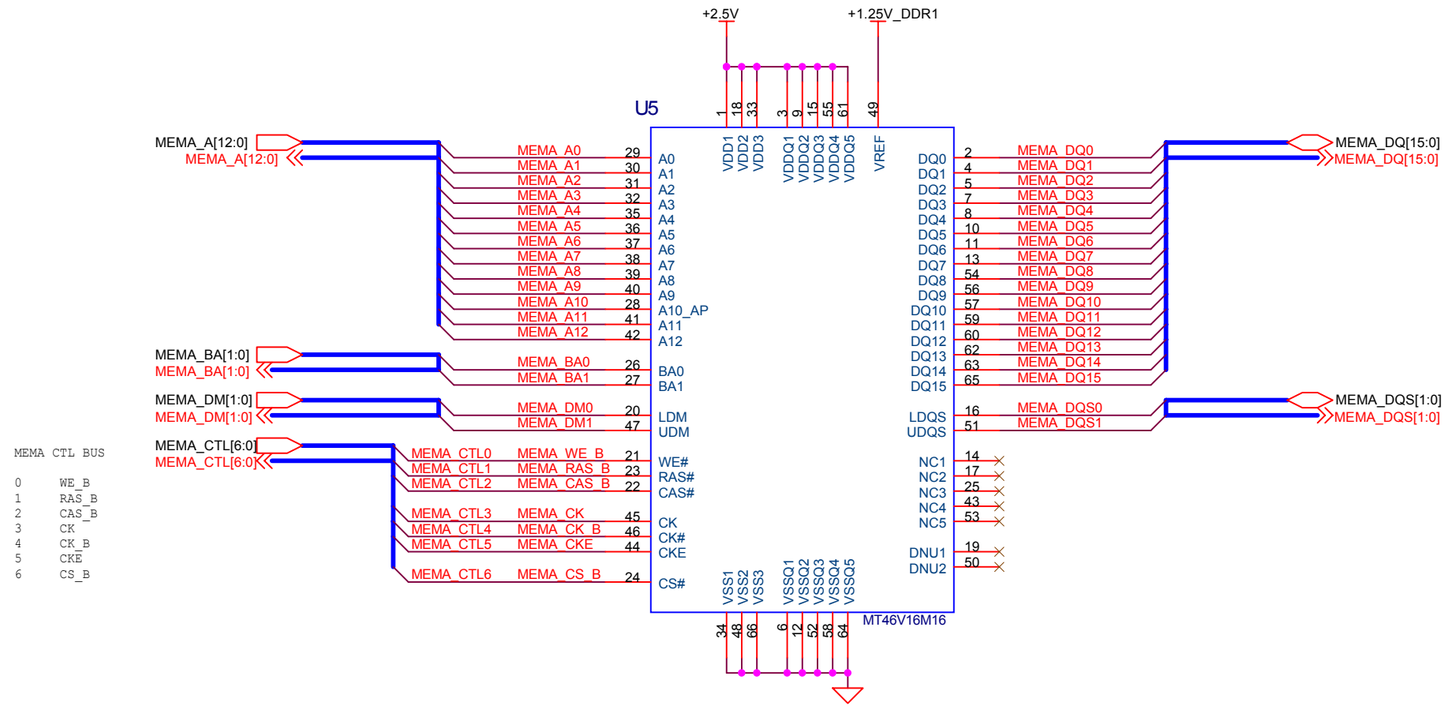
(FPGA_TDI)
SYSACE_TDO — R302 DNA
TMS — R303 DNA
TCK — R304 DNA
FPGA_TDO — R305 DNA

0 ohm 0402 resistors
SysAce Controller Bypass

Normal=R306,R307,R308,R309 In, R302,R303,R304,R305 Out
Bypass=R302,R303,R304,R305 In, R306,R307,R308,R309 Out

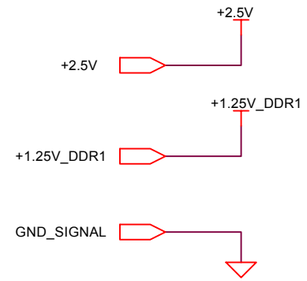
Title	Spartan3 DDR-1 Interface Board	
Size B	Document Number 0381177	Rev 2
Date: Monday, January 31, 2005	Sheet 04 of 33	

Single DDR-1 Memory on Top is designated MEMA



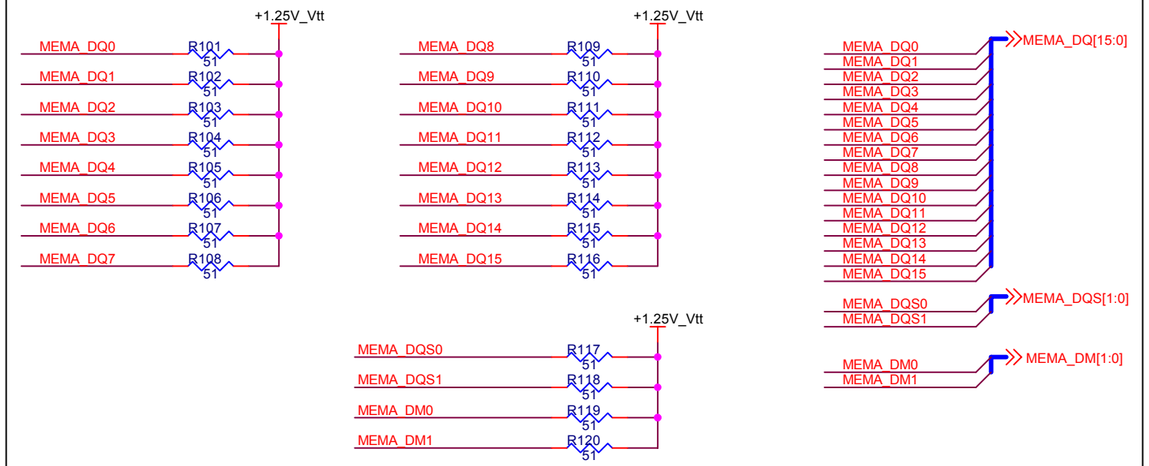

```
MEMA CTL BUS

0     WE_B
1     RAS_B
2     CAS_B
3     CK
4     CK_B
5     CKE
6     CS_B
```

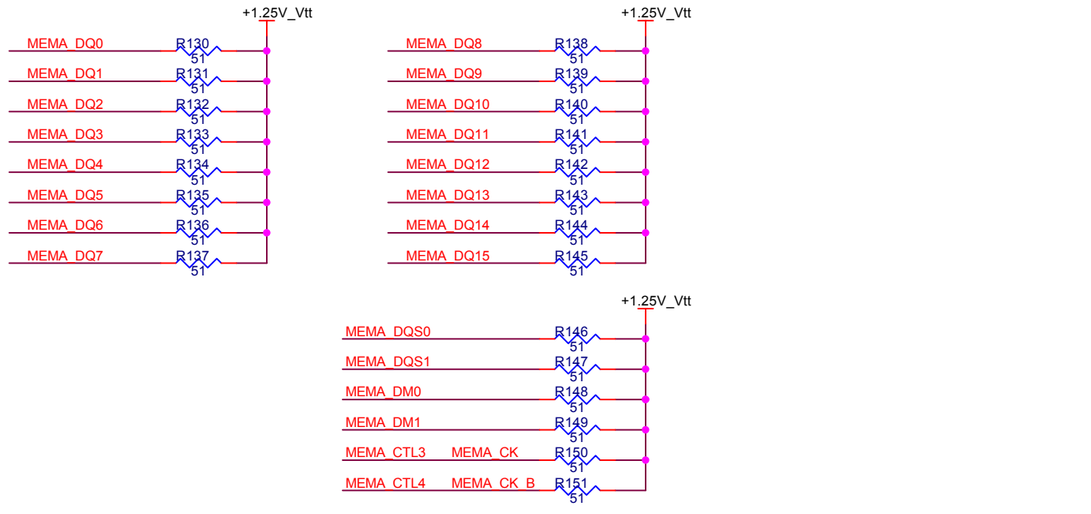


MT46V16M16TG-6P Single DDR-1 Memory on Top (MEM_Top)

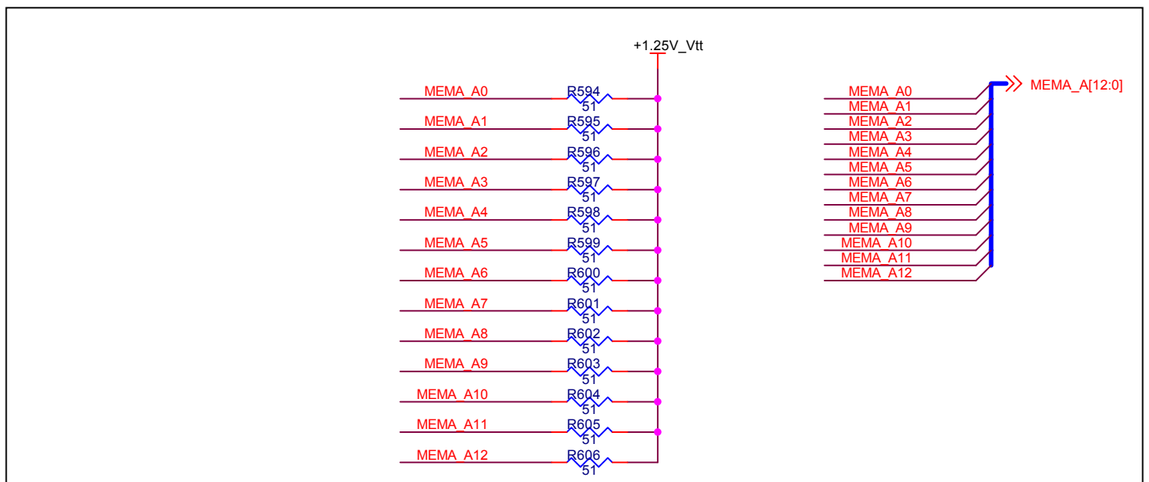
Title: Spartan3 DDR-1 Board		
Size: B	Document Number: 0381177	Rev: 1
Date: Monday, January 31, 2005	Sheet 05 of 33	



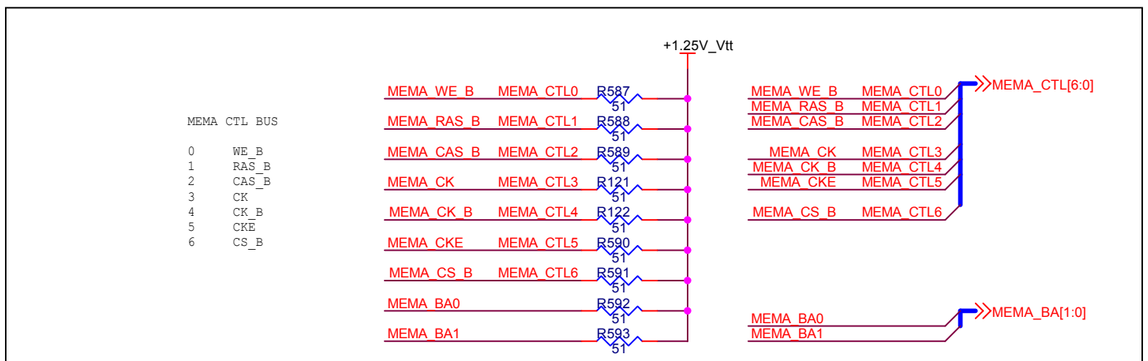
Place these resistors close to the FPGA



Place these resistors close to the MEMA



Common address signals
Place these resistors close to the MEMA

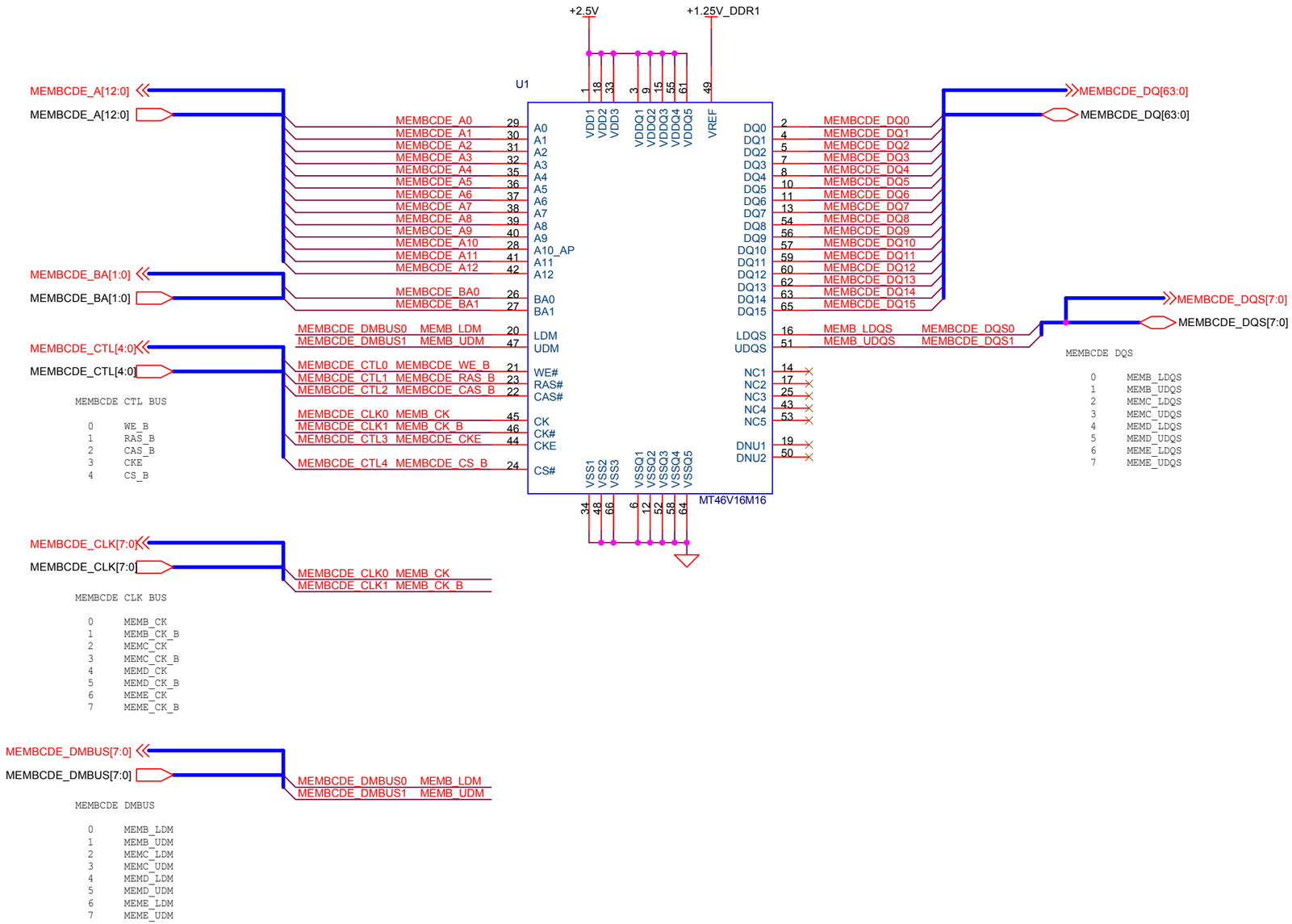


Common control signals
Place these resistors close to the MEMA

MEMA MT46V16M16TG-6P (Top) Termination Resistors

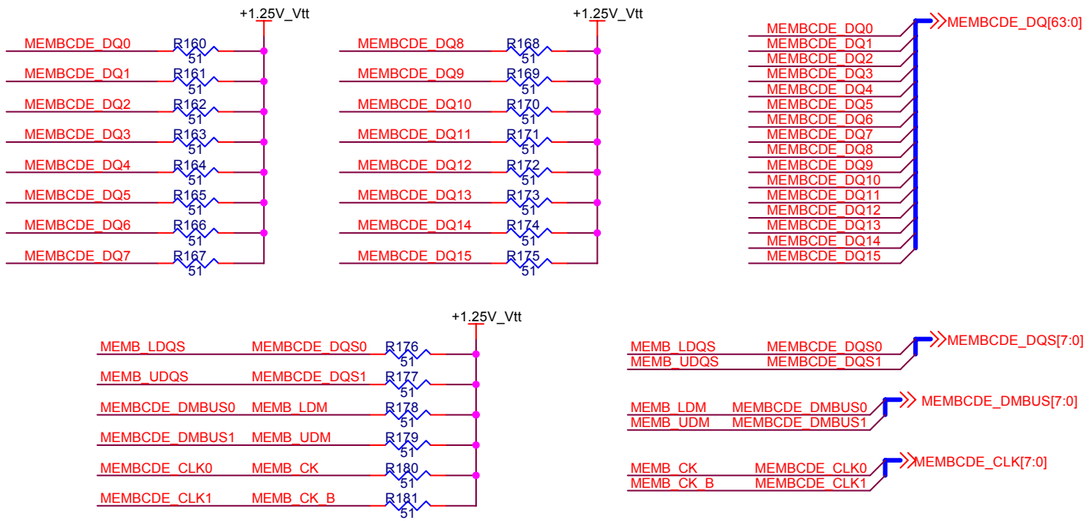
+1.25V_Vtt
+1.25V_Vtt

Title	Spartan3 DDR-1 Board	
Size B	Document Number 0381177	Rev 1
Date: Monday, January 31, 2005	Sheet 06 of 33	

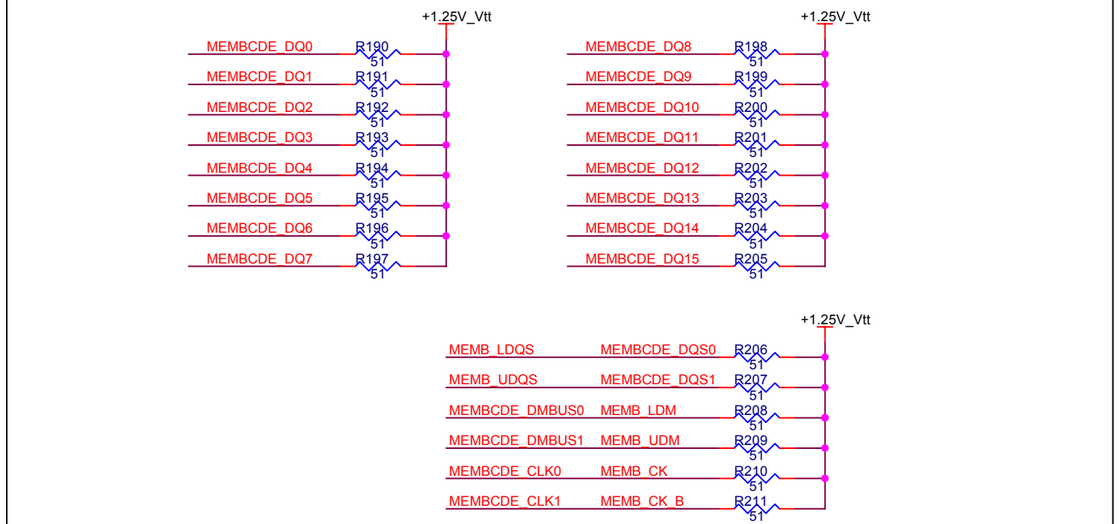


MT46V16M16TG-6P DDR-1 Memory on Left MEMB = MEM DQS(0:1)

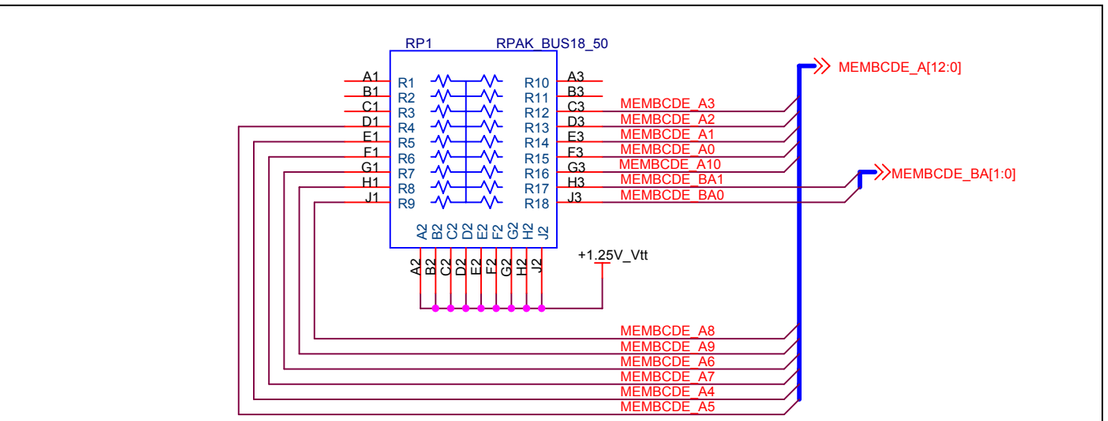
Title	Spartan3 DDR-1 Board	
Size B	Document Number 0381177	Rev 1
Date: Monday, January 31, 2005	Sheet 07 of 33	



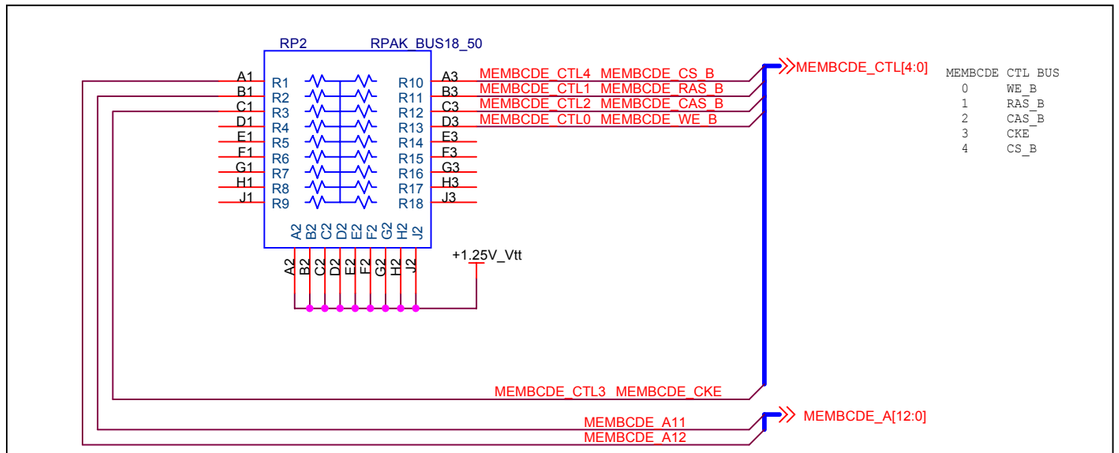
Place these resistors close to the FPGA



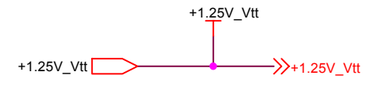
Place these resistors close to the MEMB/U1



Common address signals
Place this Rpak at end of bus "T"

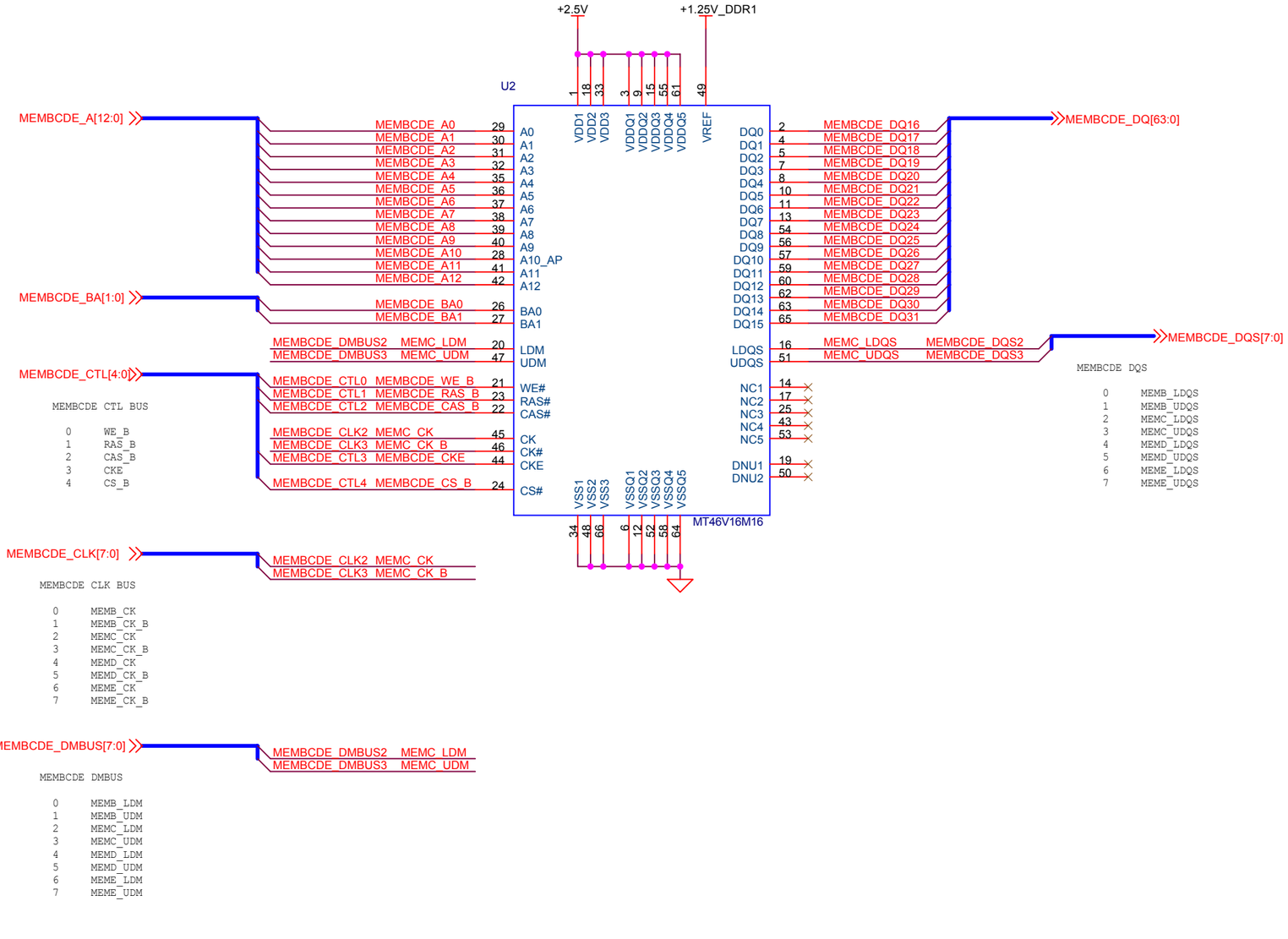


Common control signals
Place this Rpak at end of bus "T"



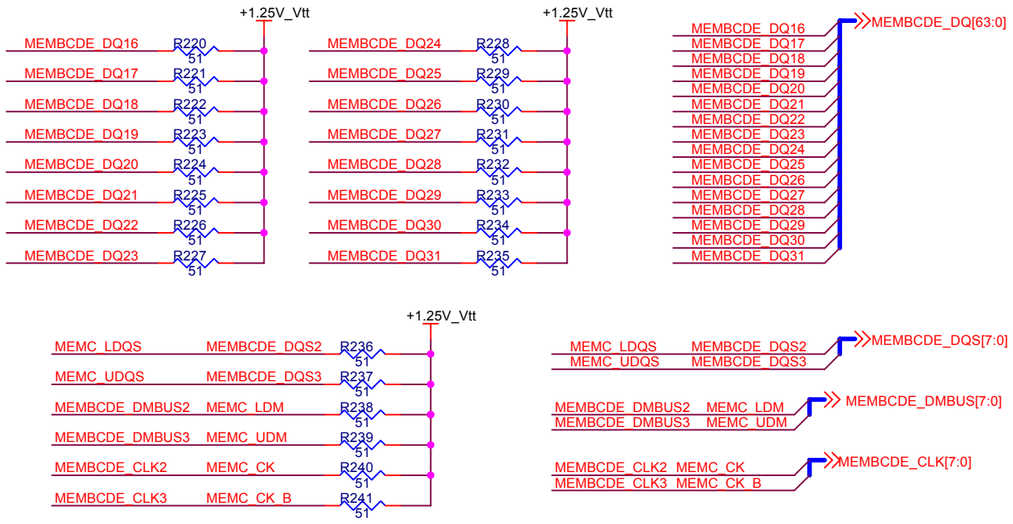
MEMB MT46V16M16TG-6P (Left) "Lower" Termination Resistors

Title: Spartan3 DDR-1 Board		
Size: B	Document Number: 0381177	Rev: 3
Date: Monday, January 31, 2005	Sheet 08 of 33	

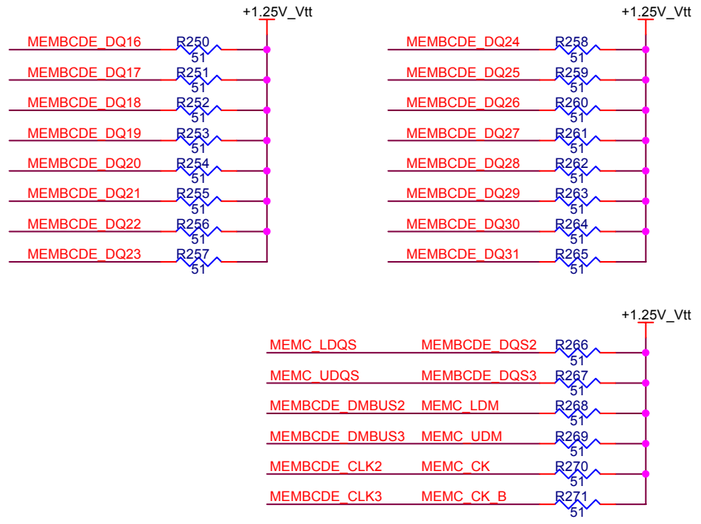


MT46V16M16TG-6P DDR-1 Memory on Left MEMC = MEM DQS(2:3)

Title	Spartan3 DDR-1 Board	
Size B	Document Number 0381177	Rev 1
Date: Monday, January 31, 2005	Sheet 09 of 33	



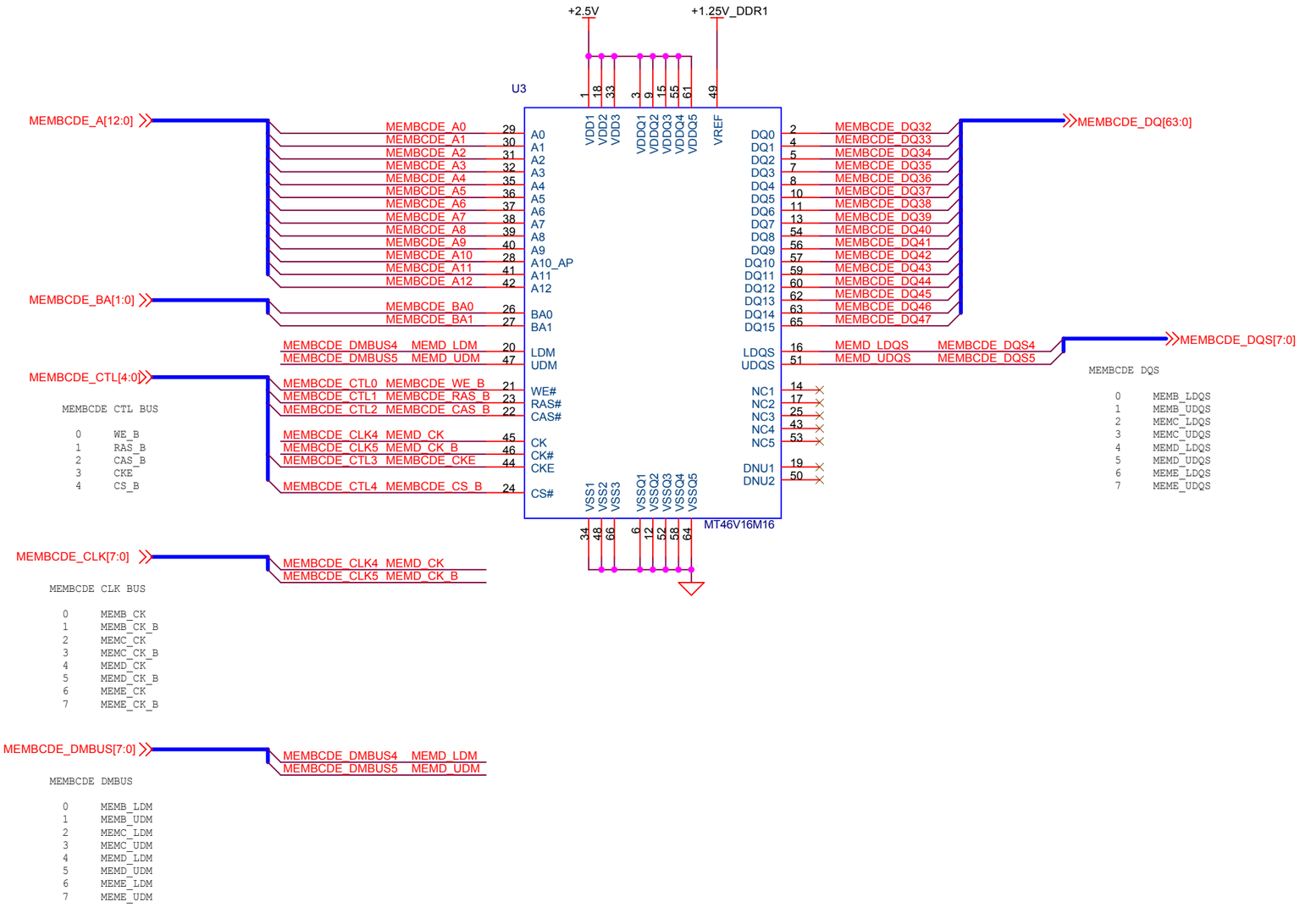
Place these resistors close to the FPGA



Place these resistors close to the MEMC

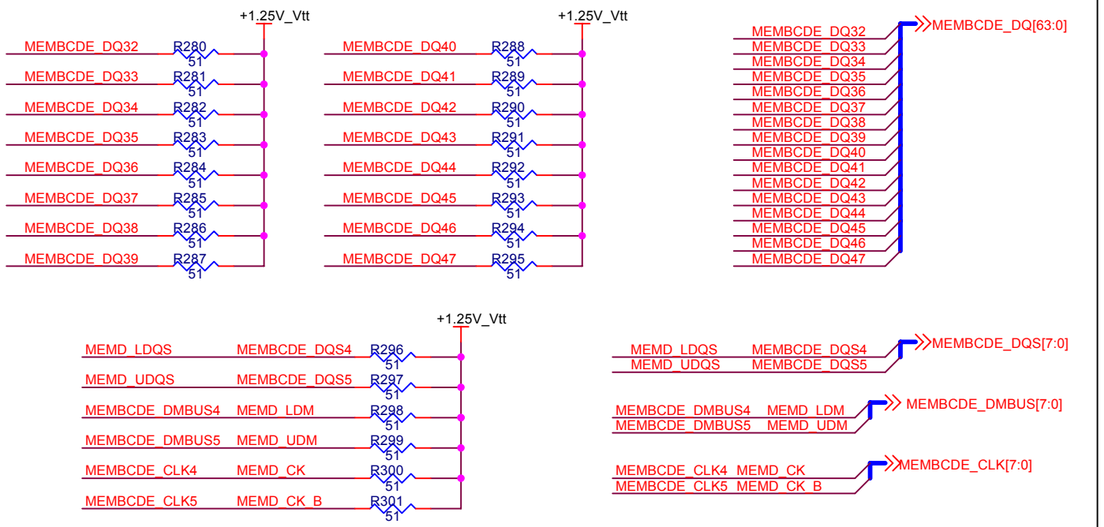
MEMC MT46V16M16TG-6P (Left) Termination Resistors

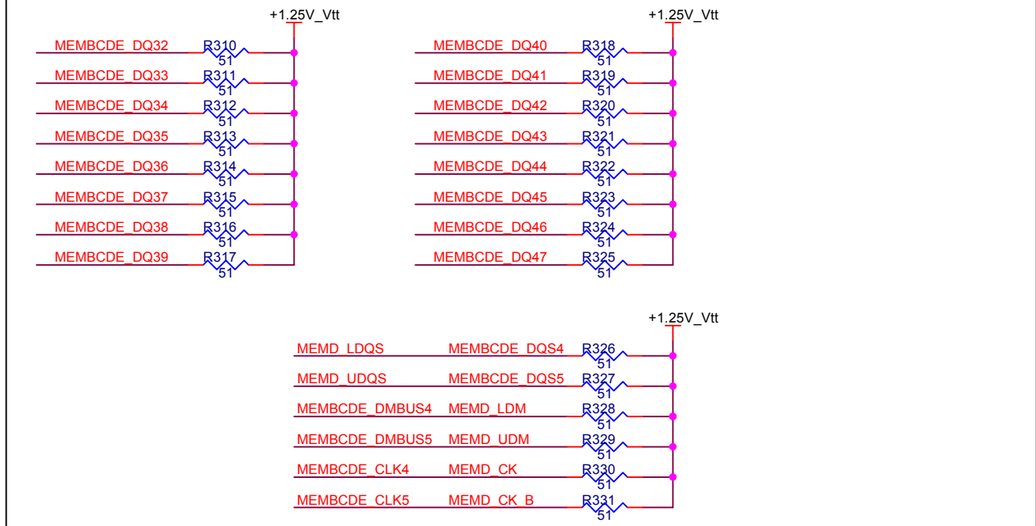
Title: Spartan3 DDR-1 Board		
Size: B	Document Number: 0381177	Rev: 1
Date: Monday, January 31, 2005	Sheet 10 of 33	

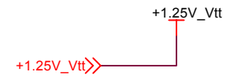


MT46V16M16TG-6P DDR-1 Memory on Left MEMD = MEM DQS(4:5)

Title	Spartan3 DDR-1 Board	
Size B	Document Number 0381177	Rev 1
Date: Monday, January 31, 2005	Sheet 11 of 33	

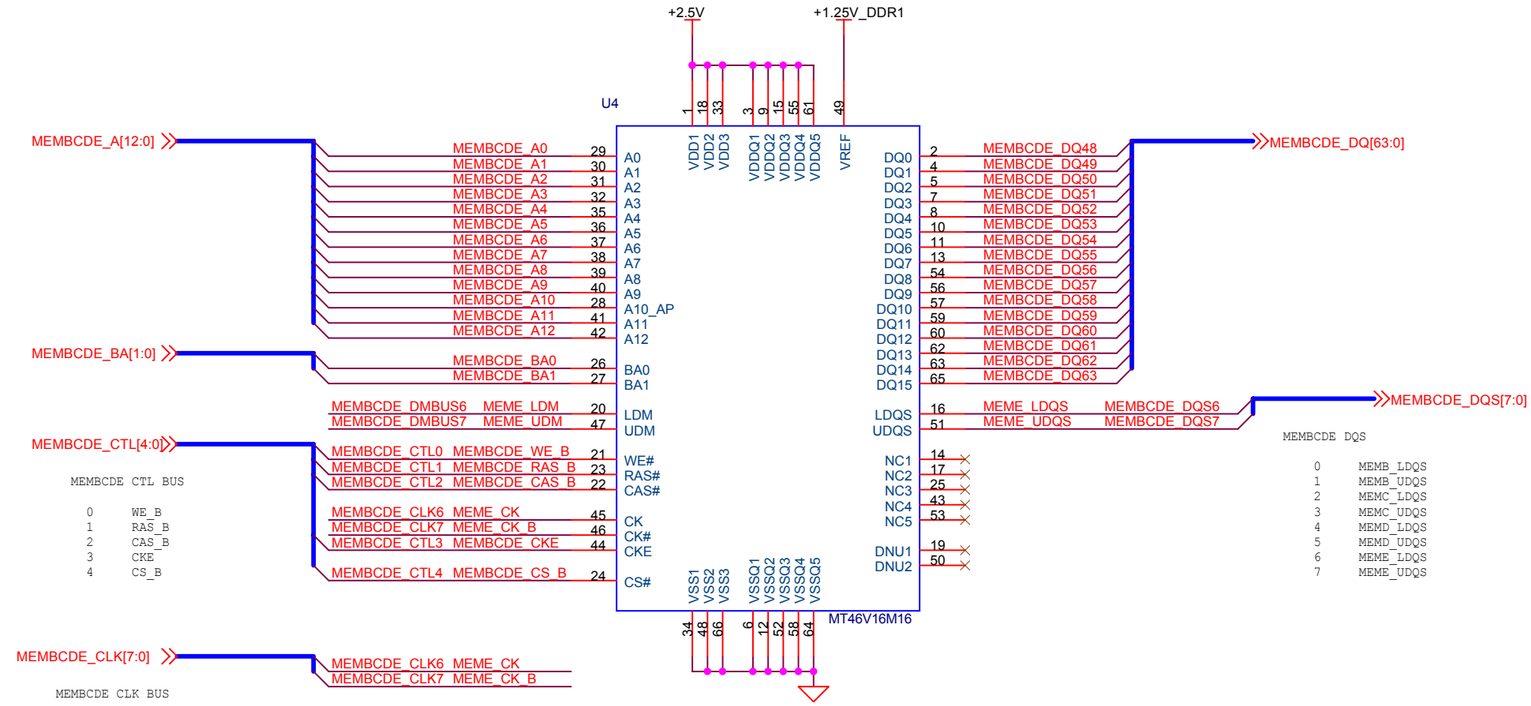






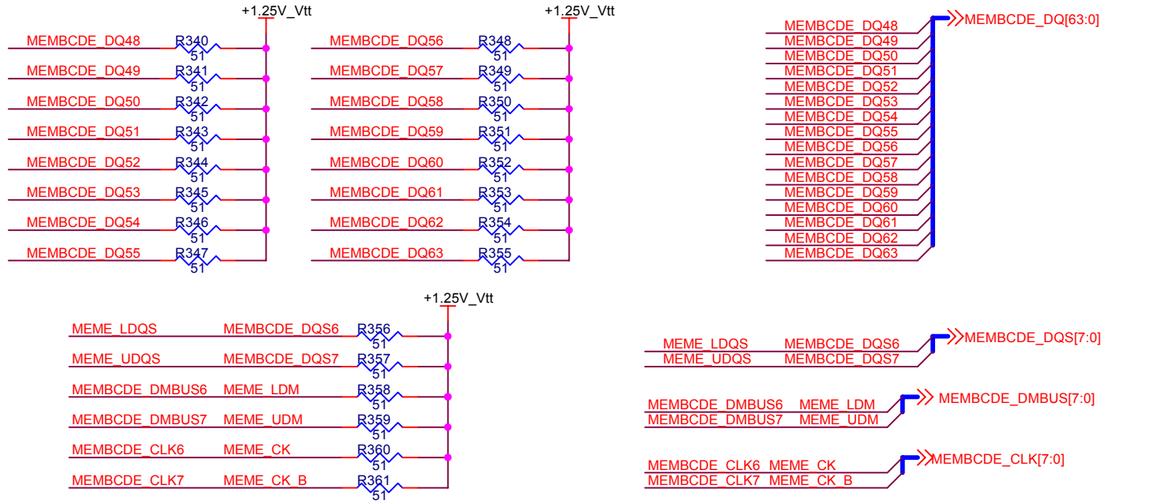
MEMD MT46V16M16TG-6P (Left) Termination Resistors

Title: Spartan3 DDR-1 Board		
Size: B	Document Number: 0381177	Rev: 1
Date: Monday, January 31, 2005	Sheet 12 of 33	

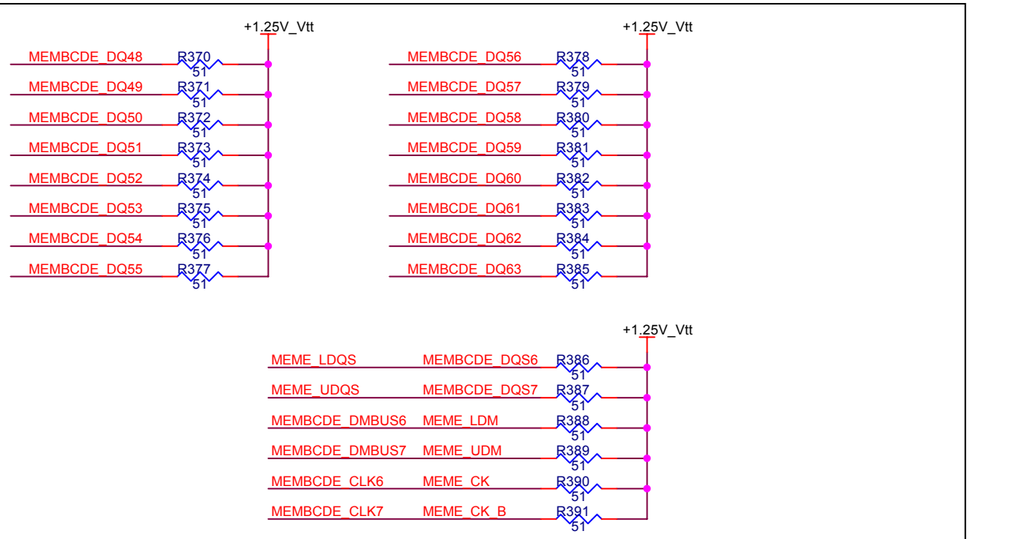


MT46V16M16TG-6P DDR-1 Memory on Left MEME = MEM DQS(6:7)

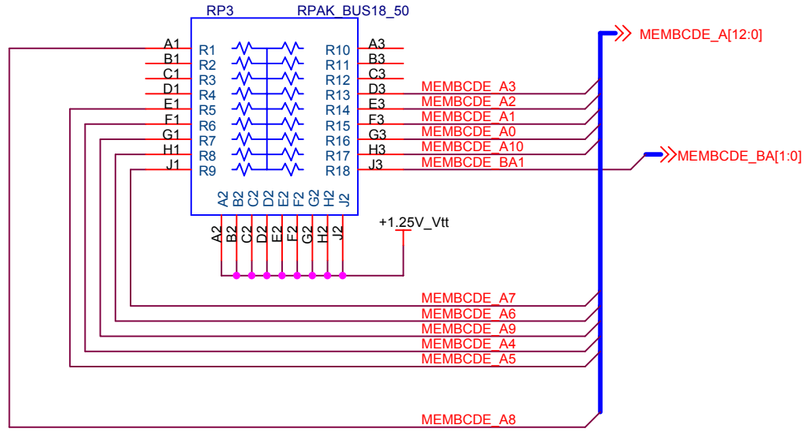
Title	Spartan3 DDR-1 Board	
Size B	Document Number 0381177	Rev 1
Date: Monday, January 31, 2005	Sheet 13 of 33	



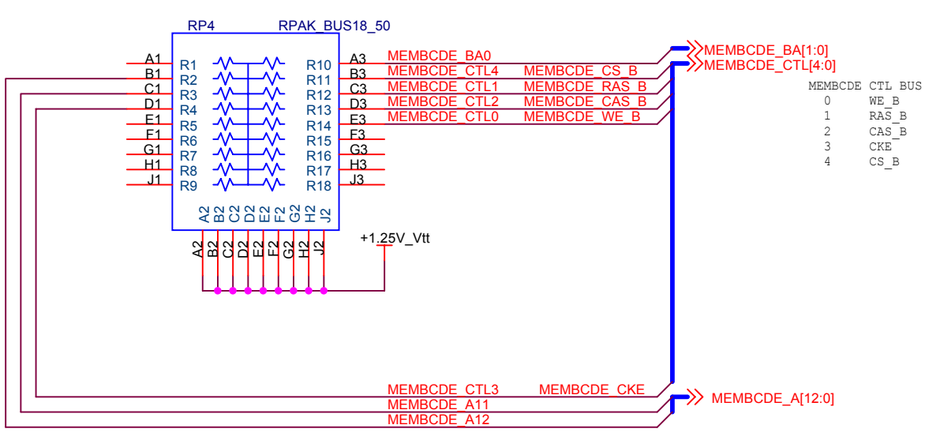
Place these resistors close to the FPGA



Place these resistors close to the MEME/U4



Common address signals
Place this Rpak at end of bus daisy-chain



Common control signals
Place this Rpak at end of bus daisy-chain

MEME MT46V16M16TG-6P (Left) "Upper" Termination Resistors

+1.25V_Vtt
+1.25V_Vtt

Title	Spartan3 DDR-1 Board	
Size B	Document Number 0381177	Rev 3
Date: Monday, January 31, 2005	Sheet 14 of 33	

DIMM_DQ[71:0]
DIMM_DQ[71:0]
DIMM_DQ0
DIMM_DQ1
DIMM_DQ2
DIMM_DQ3
DIMM_DQ4
DIMM_DQ5
DIMM_DQ6
DIMM_DQ7
DIMM_DQ8
DIMM_DQ9
DIMM_DQ10
DIMM_DQ11
DIMM_DQ12
DIMM_DQ13
DIMM_DQ14
DIMM_DQ15
DIMM_DQ16
DIMM_DQ17
DIMM_DQ18
DIMM_DQ19
DIMM_DQ20
DIMM_DQ21
DIMM_DQ22
DIMM_DQ23
DIMM_DQ24
DIMM_DQ25
DIMM_DQ26
DIMM_DQ27
DIMM_DQ28
DIMM_DQ29
DIMM_DQ30
DIMM_DQ31
DIMM_DQ32
DIMM_DQ33
DIMM_DQ34
DIMM_DQ35
DIMM_DQ36
DIMM_DQ37
DIMM_DQ38
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DIMM_DQ58
DIMM_DQ59
DIMM_DQ60
DIMM_DQ61
DIMM_DQ62
DIMM_DQ63
DIMM_DQ64
DIMM_DQ65
DIMM_DQ66
DIMM_DQ67
DIMM_DQ68
DIMM_DQ69
DIMM_DQ70
DIMM_DQ71

DIMM_A[12:0]
DIMM_A[12:0]
DIMM_A0
DIMM_A1
DIMM_A2
DIMM_A3
DIMM_A4
DIMM_A5
DIMM_A6
DIMM_A7
DIMM_A8
DIMM_A9
DIMM_A10
DIMM_A11
DIMM_A12

DIMM_BA[1:0]
DIMM_BA[1:0]
DIMM_BA0
DIMM_BA1

DIMM_DM[8:0]
DIMM_DM[8:0]
DIMM_DM0
DIMM_DM1
DIMM_DM2
DIMM_DM3
DIMM_DM4
DIMM_DM5
DIMM_DM6
DIMM_DM7
DIMM_DM8

DIMM_SA[2:0]
DIMM_SA[2:0]
DIMM_SA0
DIMM_SA1
DIMM_SA2

DIMM_S[1:0]
DIMM_S[1:0]
DIMM_S0 S0_B
DIMM_S1 S1_B

DIMM_CTL[3:0]
DIMM_CTL[3:0]
DIMM_CTL0 DIMM_WE_B
DIMM_CTL1 DIMM_RAS_B
DIMM_CTL2 DIMM_CAS_B
DIMM_CTL3 DIMM_CKE0

DIMM_CK[3:0]
DIMM_CK[3:0]
DIMM_CK0 DIMM_CK0_P
DIMM_CK1 DIMM_CK0_N
DIMM_CK2 DIMM_CK1_P
DIMM_CK3 DIMM_CK1_N

DIMM_SER[1:0]
DIMM_SER0 SDA
DIMM_SER1 SCL

DIMM_DQS[8:0]
DIMM_DQS[8:0]
DIMM_DQS0
DIMM_DQS1
DIMM_DQS2
DIMM_DQS3
DIMM_DQS4
DIMM_DQS5
DIMM_DQS6
DIMM_DQS7
DIMM_DQS8

J4
FRONT BACK
1 VREF1 — VREF2 2
3 VSS1 — VSS2 4
DIMM_DQ0 5 DQ0 — DQ4 6 DIMM_DQ4
DIMM_DQ1 7 DQ1 — DQ5 8 DIMM_DQ5
9 VDD1 — VDD2 10
DIMM_DQS0 11 DQS0 — DM0 12 DIMM_DM0
DIMM_DQ2 13 DQ2 — DQ6 14 DIMM_DQ6
15 VSS3 — VSS4 16
DIMM_DQ3 17 DQ3 — DQ7 18 DIMM_DQ7
DIMM_DQ8 19 DQ8 — DQ12 20 DIMM_DQ12
21 VDD3 — VDD4 22
DIMM_DQ9 23 DQ9 — DQ13 24 DIMM_DQ13
DIMM_DQS1 25 DQS1 — DM1 26 DIMM_DM1
27 VSS5 — VSS6 28
DIMM_DQ10 29 DQ10 — DQ14 30 DIMM_DQ14
DIMM_DQ11 31 DQ11 — DQ15 32 DIMM_DQ15
33 VDD5 — VDD6 34
DIMM_CK0_P 35 CK0 — VDD8 36
DIMM_CK0_N 37 CK0_B — VSS8 38
39 VSS7 — VSS10 40
KEY KEY
DIMM_DQ16 41 DQ16 — DQ20 42 DIMM_DQ20
DIMM_DQ17 43 DQ17 — DQ21 44 DIMM_DQ21
45 VDD7 — VDD10 46
DIMM_DQS2 47 DQS2 — DM2 48 DIMM_DM2
DIMM_DQ18 49 DQ18 — DQ22 50 DIMM_DQ22
51 VSS9 — VSS12 52
DIMM_DQ19 53 DQ19 — DQ23 54 DIMM_DQ23
DIMM_DQ24 55 DQ24 — DQ28 56 DIMM_DQ28
57 VDD9 — VDD12 58
DIMM_DQ25 59 DQ25 — DQ29 60 DIMM_DQ29
DIMM_DQS3 61 DQS3 — DM3 62 DIMM_DM3
63 VSS11 — VSS14 64
+1.25V_DDR1 DIMM_DQ26 65 DQ26 — DQ30 66 DIMM_DQ30 +1.25V_DDR1
DIMM_DQ27 67 DQ27 — DQ31 68 DIMM_DQ31
69 VDD11 — VDD14 70
DIMM_DQ64 R683 0 71 CB0 — CB4 72 CB4 R684 0 DIMM_DQ68
DIMM_DQ65 73 CB1 — CB5 74 CB5 R686 0 DIMM_DQ69
R685 0
75 VSS13 — VSS16 76
DIMM_DQS8 R687 0 77 DQS8 — DM8 78 DM8 R688 0 DIMM_DM8
DIMM_DQ66 79 CB2 — CB6 80 CB6 R690 0 DIMM_DQ70
R689 0
DIMM_DQ67 R691 0 81 CB3 — VDD16 82 CB7 R692 0 DIMM_DQ71
83 CB3/DNU9 — CB7/DNU10 84
85 NC1 — NC2 86
87 VSS15 — VSS18 88
89 CK2 — VSS20 90
91 CK2_B — VDD18 92
93 VDD15 — VDD20 94
DIMM_CKE0 R738 0 95 NC3/CKE1 — CKE0 96 DIMM_CKE0
97 NC5 — NC4 98
DIMM_A12 99 NC7/A12 — A11 100 DIMM_A11
DIMM_A9 101 A9 — A8 102 DIMM_A8
103 VSS17 — VSS22 104
DIMM_A7 105 A7 — A6 106 DIMM_A6
DIMM_A5 107 A5 — A4 108 DIMM_A4
DIMM_A3 109 A3 — A2 110 DIMM_A2
DIMM_A1 111 A1 — A0 112 DIMM_A0
113 VDD17 — VDD22 114
DIMM_A10 115 A10 — BA1 116 DIMM_BA1
DIMM_BA0 117 BA0 — RAS_B 118 DIMM_RAS_B
DIMM_WE_B 119 WE_B — CAS_B 120 DIMM_CAS_B
S0_B 121 S0_B — NC6/S1_B 122 S1_BAR R693 0 S1_B
123 NC9/A13 — NC8 124
125 VSS19 — VSS24 126
DIMM_DQ32 127 DQ32 — DQ36 128 DIMM_DQ36
DIMM_DQ33 129 DQ33 — DQ37 130 DIMM_DQ37
131 VDD19 — VDD24 132
DIMM_DQS4 133 DQS4 — DM4 134 DIMM_DM4
DIMM_DQ34 135 DQ34 — DQ38 136 DIMM_DQ38
137 VSS21 — VSS26 138
DIMM_DQ35 139 DQ35 — DQ39 140 DIMM_DQ39
DIMM_DQ40 141 DQ40 — DQ44 142 DIMM_DQ44
143 VDD21 — VDD26 144
DIMM_DQ41 145 DQ41 — DQ45 146 DIMM_DQ45
DIMM_DQS5 147 DQS5 — DM5 148 DIMM_DM5
149 VSS23 — VSS28 150
DIMM_DQ42 151 DQ42 — DQ46 152 DIMM_DQ46
DIMM_DQ43 153 DQ43 — DQ47 154 DIMM_DQ47
155 VDD23 — VDD28 156
157 VDD25 — CK1_B 158 DIMM_CK1_N
159 VSS25 — CK1 160 DIMM_CK1_P
161 VSS27 — VSS30 162
DIMM_DQ48 163 DQ48 — DQ52 164 DIMM_DQ52
DIMM_DQ49 165 DQ49 — DQ53 166 DIMM_DQ53
167 VDD27 — VDD30 168
DIMM_DQS6 169 DQS6 — DM6 170 DIMM_DM6
DIMM_DQ50 171 DQ50 — DQ54 172 DIMM_DQ54
173 VSS29 — VSS32 174
DIMM_DQ51 175 DQ51 — DQ55 176 DIMM_DQ55
DIMM_DQ56 177 DQ56 — DQ60 178 DIMM_DQ60
179 VDD29 — VDD32 180
DIMM_DQ57 181 DQ57 — DQ61 182 DIMM_DQ61
DIMM_DQS7 183 DQS7 — DM7 184 DIMM_DM7
185 VSS31 — VSS33 186
DIMM_DQ58 187 DQ58 — DQ62 188 DIMM_DQ62
DIMM_DQ59 189 DQ59 — DQ63 190 DIMM_DQ63
191 VDD31 — VDD34 192
SDA 193 SDA — SA0 194 DIMM_SA0
SCL 195 SCL — SA1 196 DIMM_SA1
197 VDDSPD — SA2 198 DIMM_SA2
199 NC11 — NC10 200
SODIMM_DDR1_SKT_ECC
+2.5V +2.5V

+2.5V
+2.5V
+1.25V_DDR1
+1.25V_DDR1
GND_SIGNAL

SODIMM 200-pin Socket
MT4VDDT1664HY 128MB Memory

Title	Spartan3 DDR-1 Board	
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MT4VDDT1664HY 128MB Memory Termination Resistors

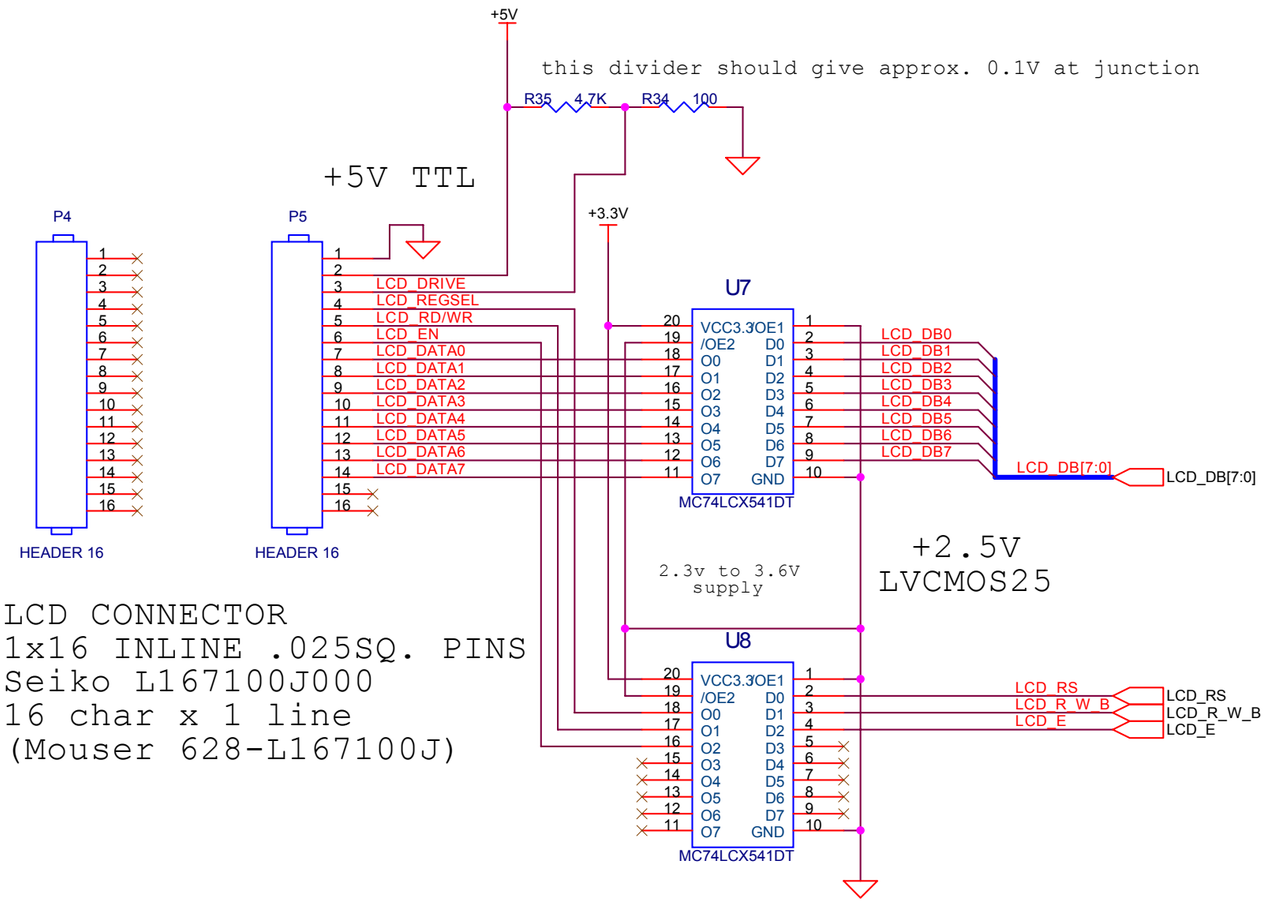
Place these resistors close to the FPGA

Place these resistors at the end of the bus daisy-chain

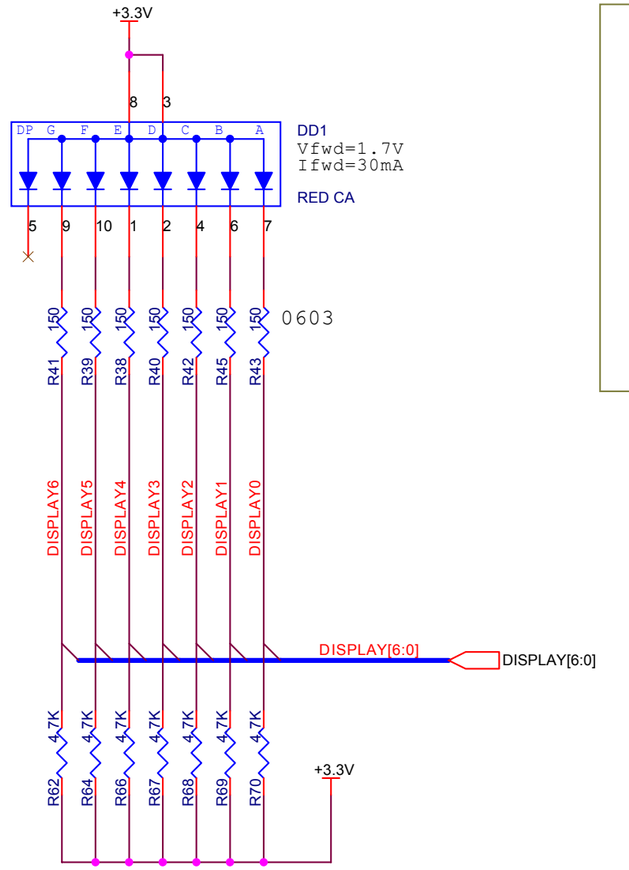
Place these resistors close to the SODIMM socket

Title	Spartan3 DDR-1 Board	
Size B	Document Number 0381177	Rev 1
Date: Monday, January 31, 2005	Sheet 16 of 33	

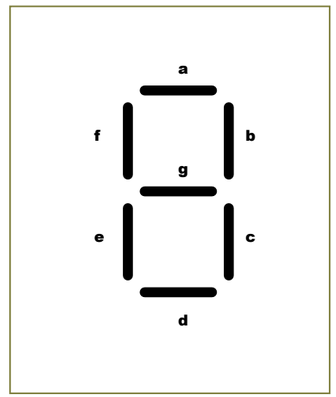
This LCD requires two rows of 16 pins to support it physically
Place the 1X16 SIP headers 31mm apart per the LCD spec sheet

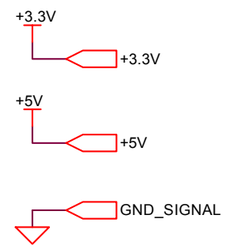


LCD CONNECTOR
1x16 INLINE .025SQ. PINS
Seiko L167100J000
16 char x 1 line
(Mouser 628-L167100J)



4.7K 0402 Pullups to keep display turned off at power on





LCD

Title: Spartan3 DDR-1 Interface Board		
Size: B	Document Number: 0381177	Rev: 1
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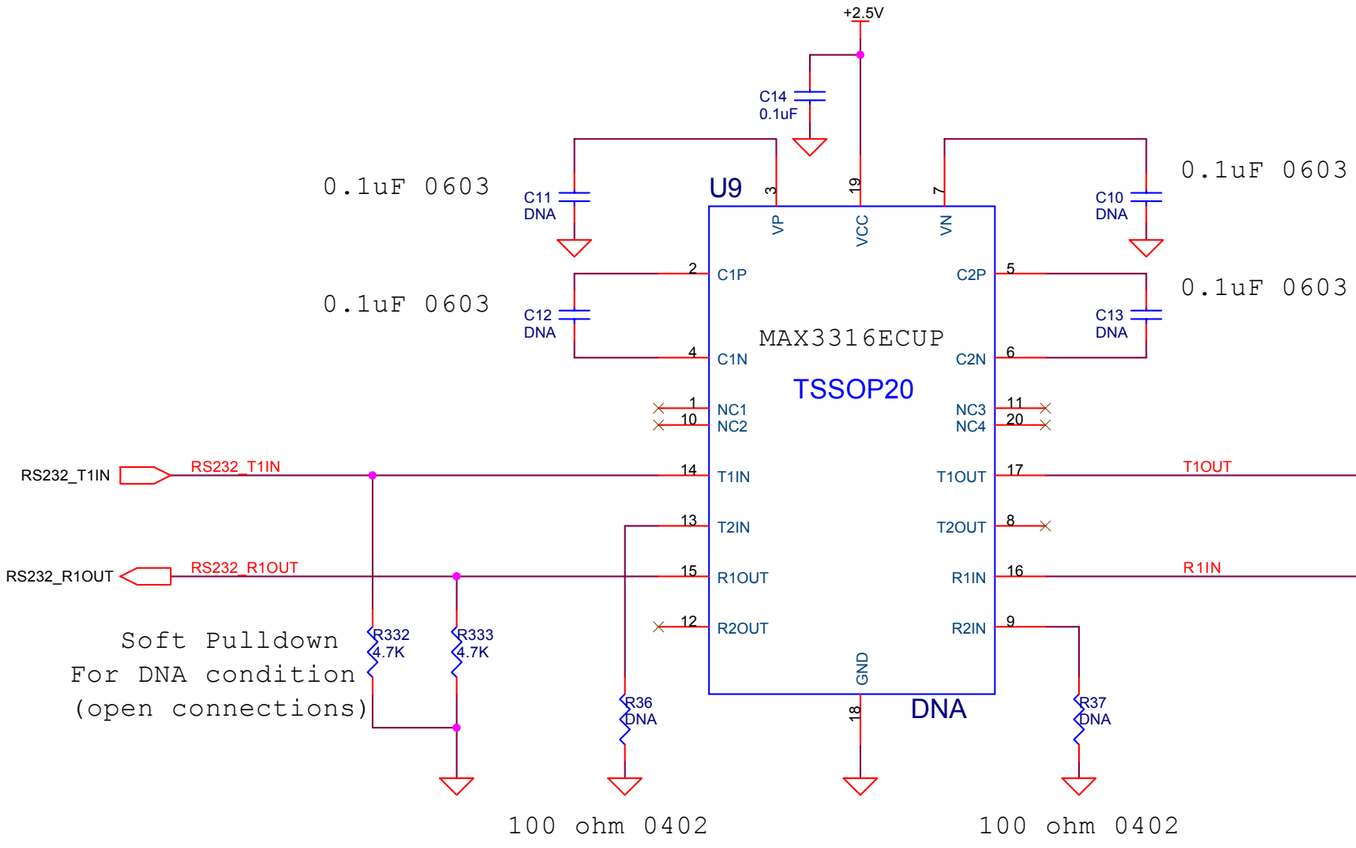

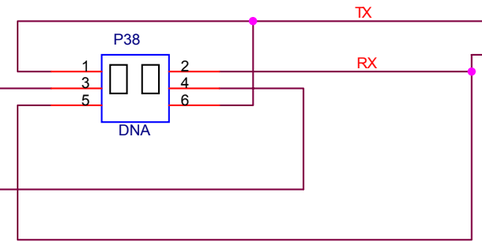

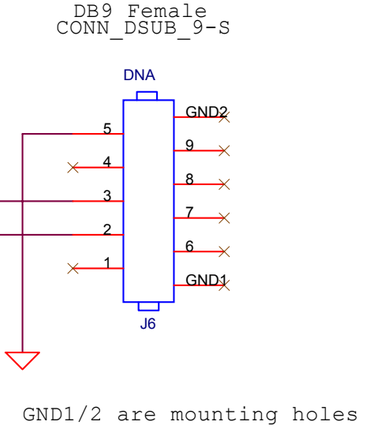

NULL MODEM HEADER

TX 1-3 TXOUT ON J5.3
RX 2-4 RXIN ON J5.2

TX 3-5 TXOUT ON J5.2
RX 4-6 RXIN ON J5.3

RS232 Components are not installed, and will not be tested

RS232 DRIVER

Title: Spartan3 DDR-1 Interface Board		
Size: B	Document Number: 0381177	Rev: 1
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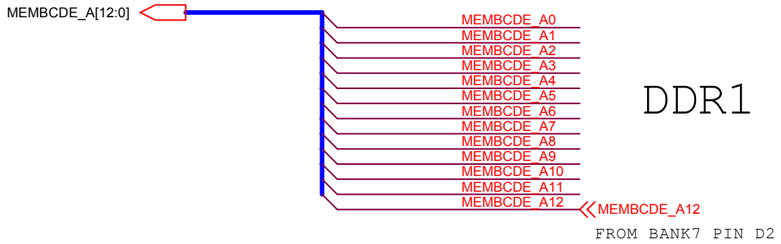
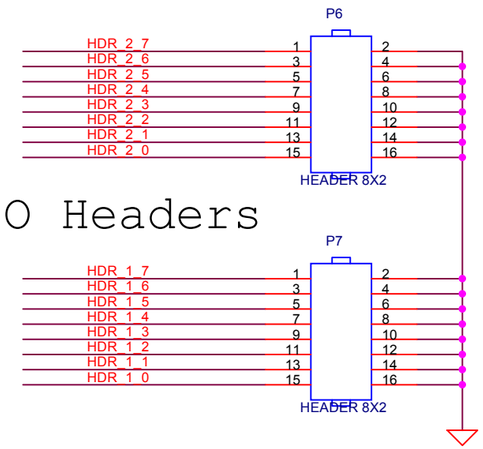
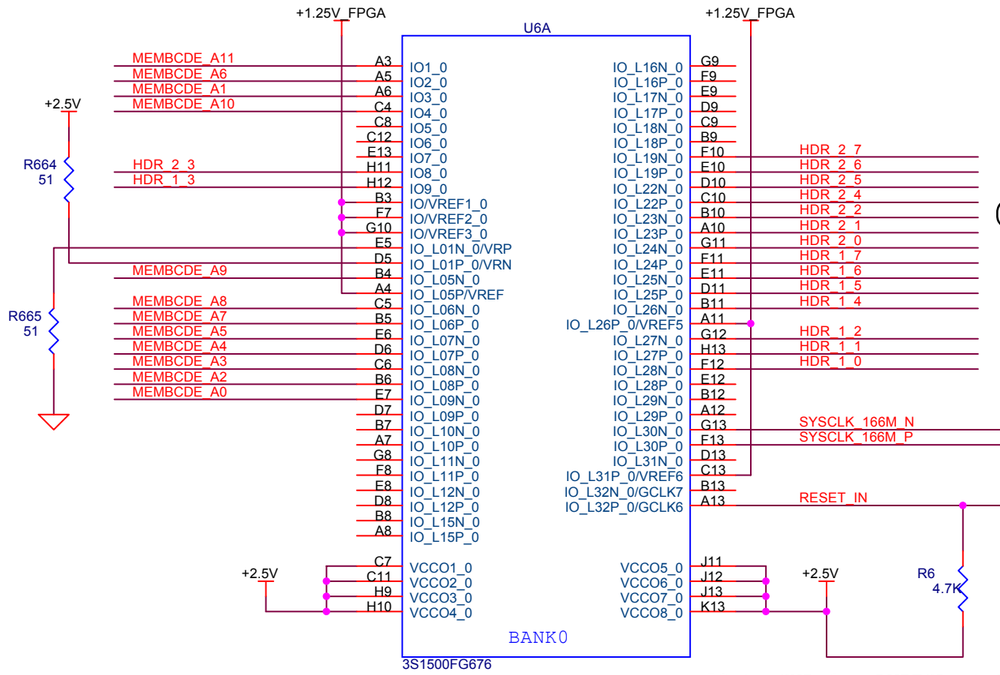


DDR1 x4 (MEMB - MEME) "Left" Side Interface



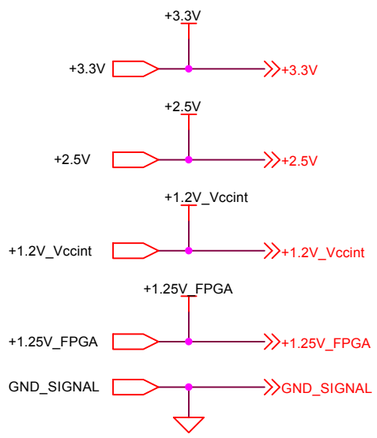
GPIO Headers



GPIO Header Interface

Reset P.B.

Osc. Y1 Clock Interface



DDR1 x4 (MEMB - MEME) "Left" Side Interface
Osc. Y1 Clock Interface
Reset P.B. Interface
GPIO Header Interface

4 x 16-bit DDR-1 Mem
on the Left are designated:
MEMB = MEM DQS(0:1)
MEMC = MEM DQS(2:3)
MEMD = MEM DQS(4:5)
MEME = MEM DQS(6:7)

3S1500FG676 Bank0

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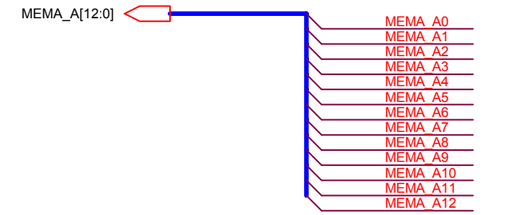
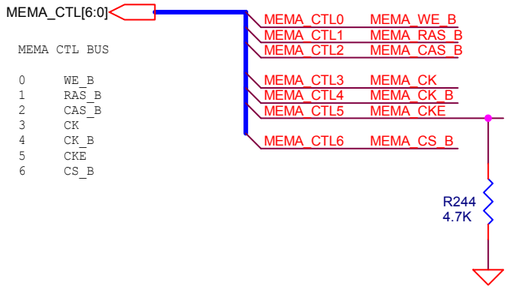
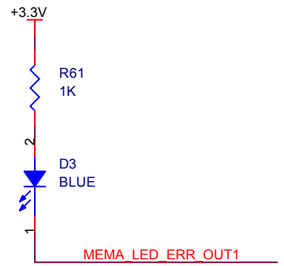
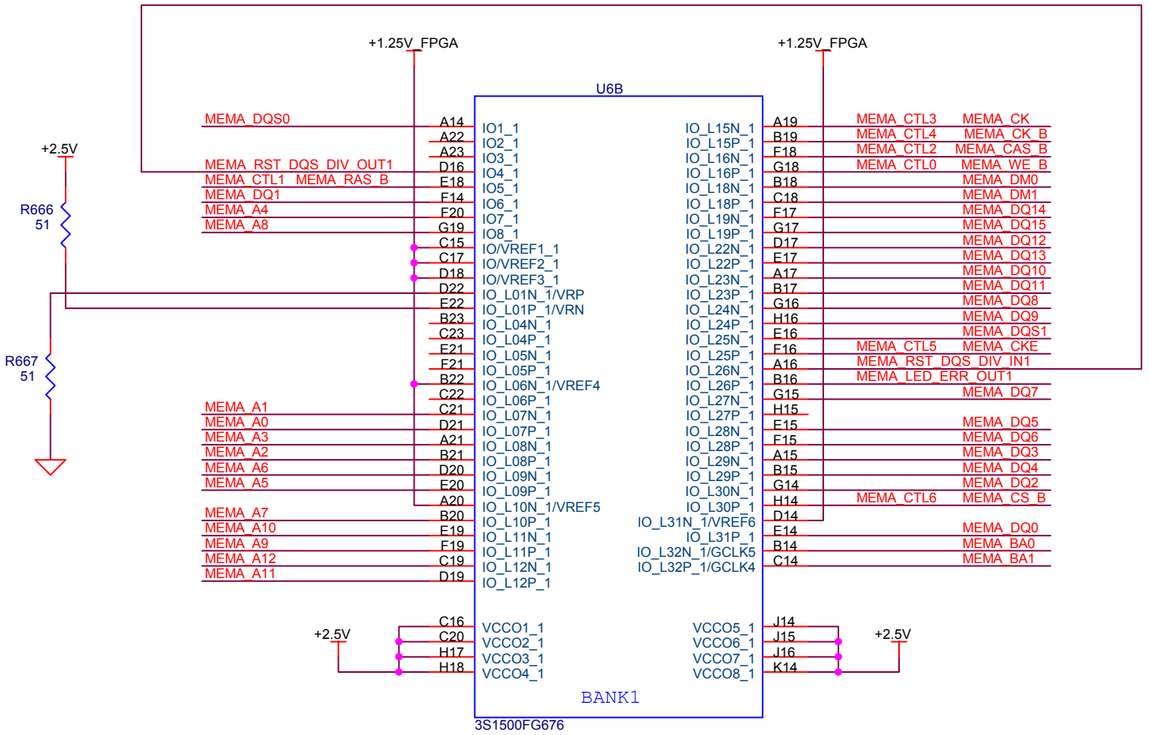


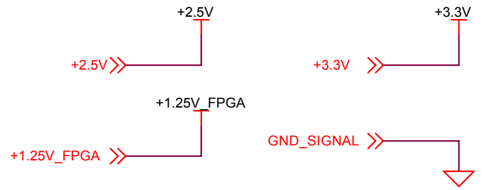






"Top" Memory DQS loop wire

DDR1 x 1 "Top" Interface



3S1500FG676 Bank1

Title: Spartan3 DDR-1 Board		
Size: B	Document Number: 0381177	Rev: 2
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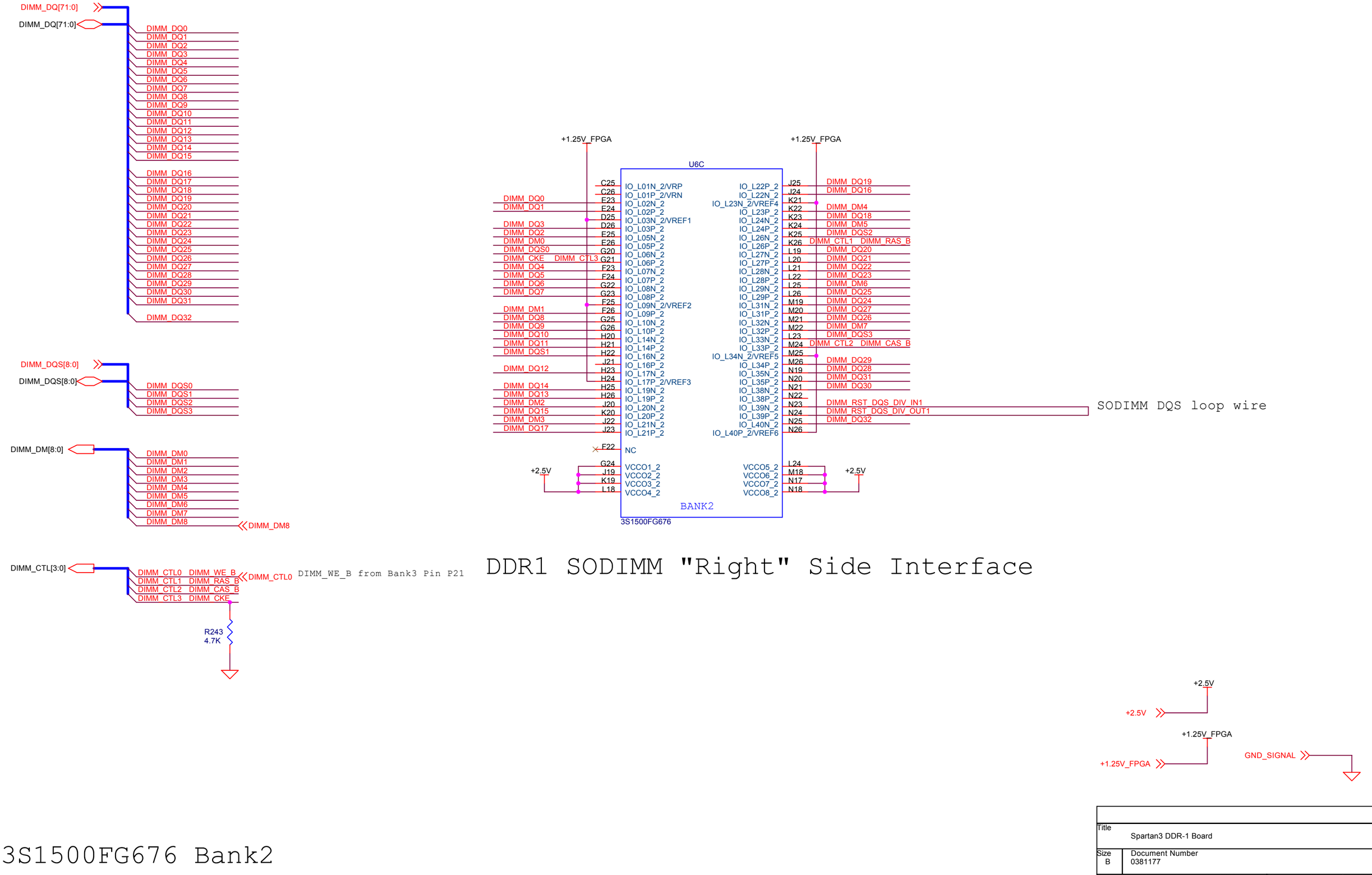

Title	Spartan3 DDR-1 Board	
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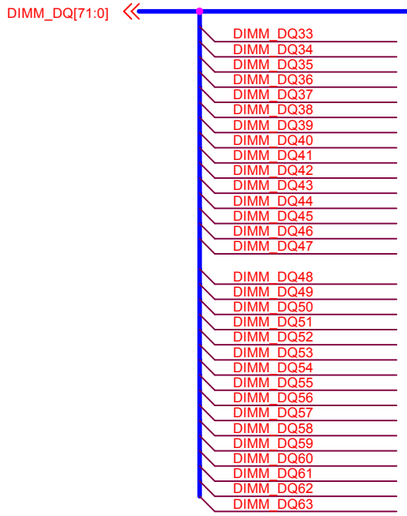
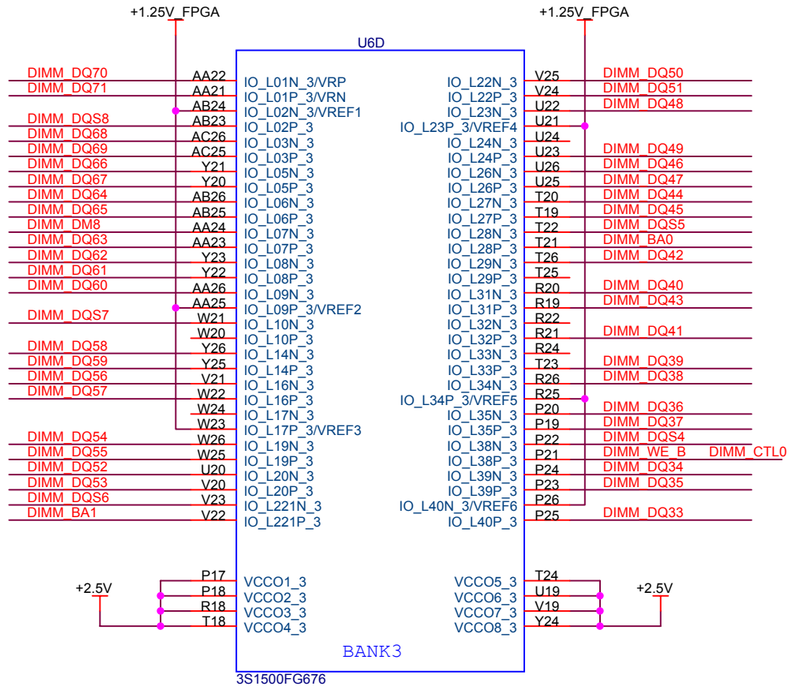
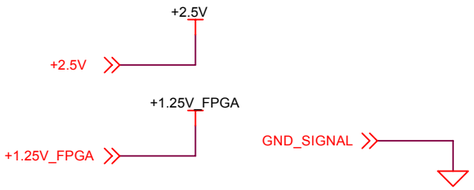




DDR1 SODIMM "Right" Side Interface



3S1500FG676 Bank3

Title	Spartan3 DDR-1 Board	
Size B	Document Number 0381177	Rev 2
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DDR1 SODIMM Interface

DIMM_A[12:0]
DIMM_A0
DIMM_A1
DIMM_A2
DIMM_A3
DIMM_A4
DIMM_A5
DIMM_A6
DIMM_A7
DIMM_A8
DIMM_A9
DIMM_A10
DIMM_A11
DIMM_A12

DIMM_SA[2:0]
DIMM_SA0
DIMM_SA1
DIMM_SA2

DIMM_S[1:0]
DIMM_S0 S0_B
DIMM_S1 S1_B

DIMM_SER[1:0]
DIMM_SER0 SDA
DIMM_SER1 SCL

DIMM_CK[3:0]
DIMM_CK0 DIMM_CK0_P
DIMM_CK1 DIMM_CK0_N
DIMM_CK2 DIMM_CK1_P
DIMM_CK3 DIMM_CK1_N

+3.3V
R63
1K
D4
BLUE
DIMM_LED_ERR_OUT1

+1.25V_FPGA
+1.25V_FPGA
U6E

DIMM_A2	AA20	IO1_4	IO_L15N_4	AE19	DIMM_LED_ERR_OUT1
S1_B DIMM_S1	AD15	IO2_4	IO_L15P_4	AF19	
S0_B DIMM_S0	AD19	IO3_4	IO_L16N_4	Y18	DIMM_SA1
DIMM_A10	AD23	IO4_4	IO_L16P_4	AA18	DIMM_SER0 SDA
DIMM_SA0	AF21	IO5_4	IO_L17N_4	AB18	
DIMM_SER1 SCL	AF22	IO6_4	IO_L17P_4	AC18	
	W15	IO7_4	IO_L18N_4	AD18	
	W16	IO8_4	IO_L18P_4	AE18	
	AB14	IO/VREF1_4	IO_L19N_4	AC17	
	AD25	IO/VREF2_4	IO_L19P_4	AA17	
	Y17	IO/VREF3_4	IO_L22N_4/VREF5	AD17	
	AB22	IO_L01N_4/VRP	IO_L22P_4	AB17	
	AC22	IO_L01P_4/VRN	IO_L23N_4	AE17	
DIMM_CK1_N DIMM_CK3	AE24	IO_L04N_4	IO_L23P_4	AF17	
DIMM_CK1_P DIMM_CK2	AF24	IO_L04P_4	IO_L24N_4	Y16	
DIMM_A11	AE23	IO_L05N_4	IO_L24P_4	AA16	
DIMM_A12	AF23	IO_L05P_4	IO_L25N_4	AB16	
	AD22	IO_L06N_4/VREF4	IO_L25P_4	AC16	
DIMM_A9	AE22	IO_L06P_4	IO_L26N_4	AE16	
DIMM_A7	AB21	IO_L07N_4	IO_L26P_4/VREF6	AF16	
DIMM_A8	AC21	IO_L07P_4	IO_L27P_4/D1	W14	
DIMM_CK0_N DIMM_CK1	AD21	IO_L08N_4	IO_L28N_4	AA15	
DIMM_CK0_P DIMM_CK0	AE21	IO_L08P_4	IO_L28P_4	AB15	
DIMM_SA2	AB20	IO_L09N_4	IO_L29N_4	AE15	
	AC20	IO_L09P_4	IO_L29P_4	AF15	
DIMM_A5	AE20	IO_L10N_4	IO_L30N_4/D2	Y14	
DIMM_A6	AF20	IO_L10P_4	IO_L30P_4/D3	AA14	
DIMM_A3	Y19	IO_L11N_4	IO_L31N_4/INIT_B PIN AC14		
DIMM_A4	AA19	IO_L11P_4	IO_L31P_4/DOUT/BUSY PIN AD14		
DIMM_A0	AB19	IO_L12N_4	IO_L32N_4/GCLK1	AE14	
DIMM_A1	AC19	IO_L12P_4	IO_L32P_4/GCLK0	AF14	
	AD16	VCCO1_4	VCCO5_4	V15	
	AD20	VCCO2_4	VCCO6_4	V16	
	U14	VCCO3_4	VCCO7_4	W17	
	V14	VCCO4_4	VCCO8_4	W18	

+2.5V
+2.5V
BANK4
3S1500FG676

100 parallel term. for LVDS at SMA's J1/J2 (Sheet 3)

R584
100
EXTCLK1_N
EXTCLK1_P

EXTCLK SMA Interface

R585 DNA
R586 DNA

50 to GND for LVPECL at SMA's J1/J2 (Sheet 3)

For single-ended LVCMOS oscillator at Y1, no term. R's here

DDR1 SODIMM "Right" Side Interface
EXTCLK SMA Interface

+2.5V
+2.5V
+3.3V
+3.3V
+1.25V_FPGA
+1.25V_FPGA
GND_SIGNAL

3S1500FG676 Bank4

Title: Spartan3 DDR-1 Board		
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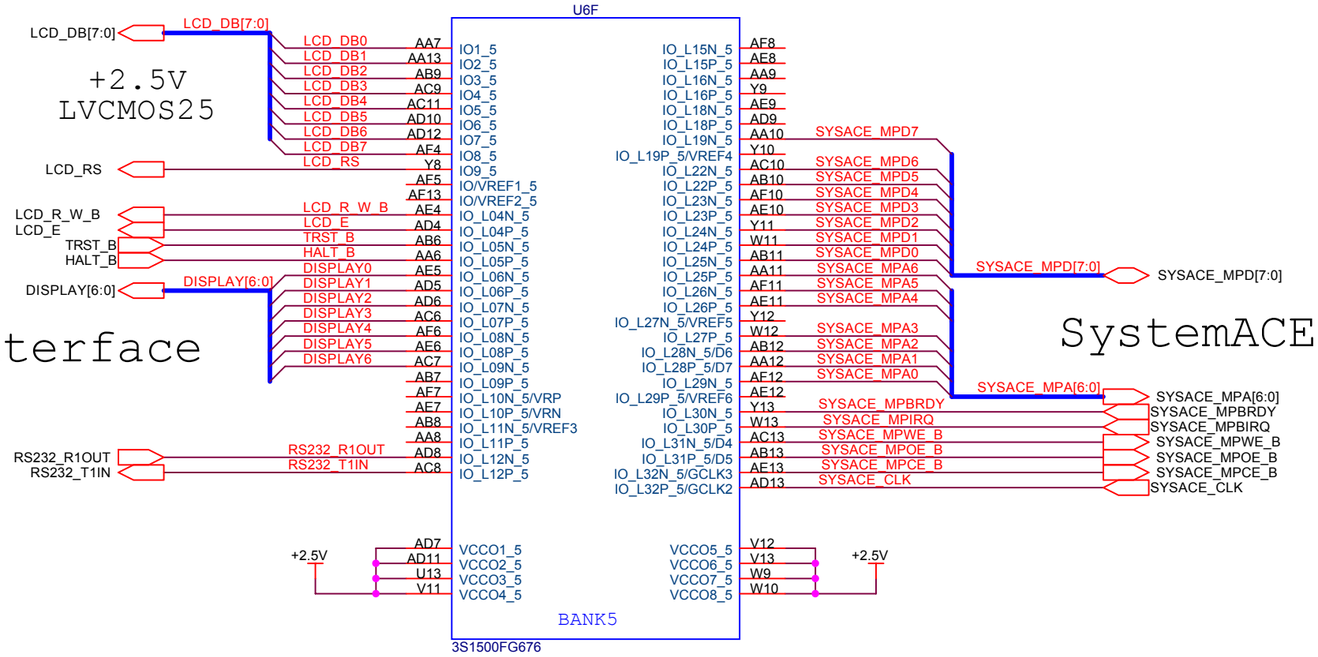
LCD Interface

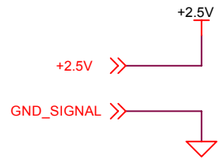
7-Seg. Display Interface

RS232 Interface



SystemACE Interface

LCD Interface
7-Seg. Display Interface
RS232 Interface
SystemACE Interface



3S1500FG676 Bank5

Title: Spartan3 DDR-1 Board		
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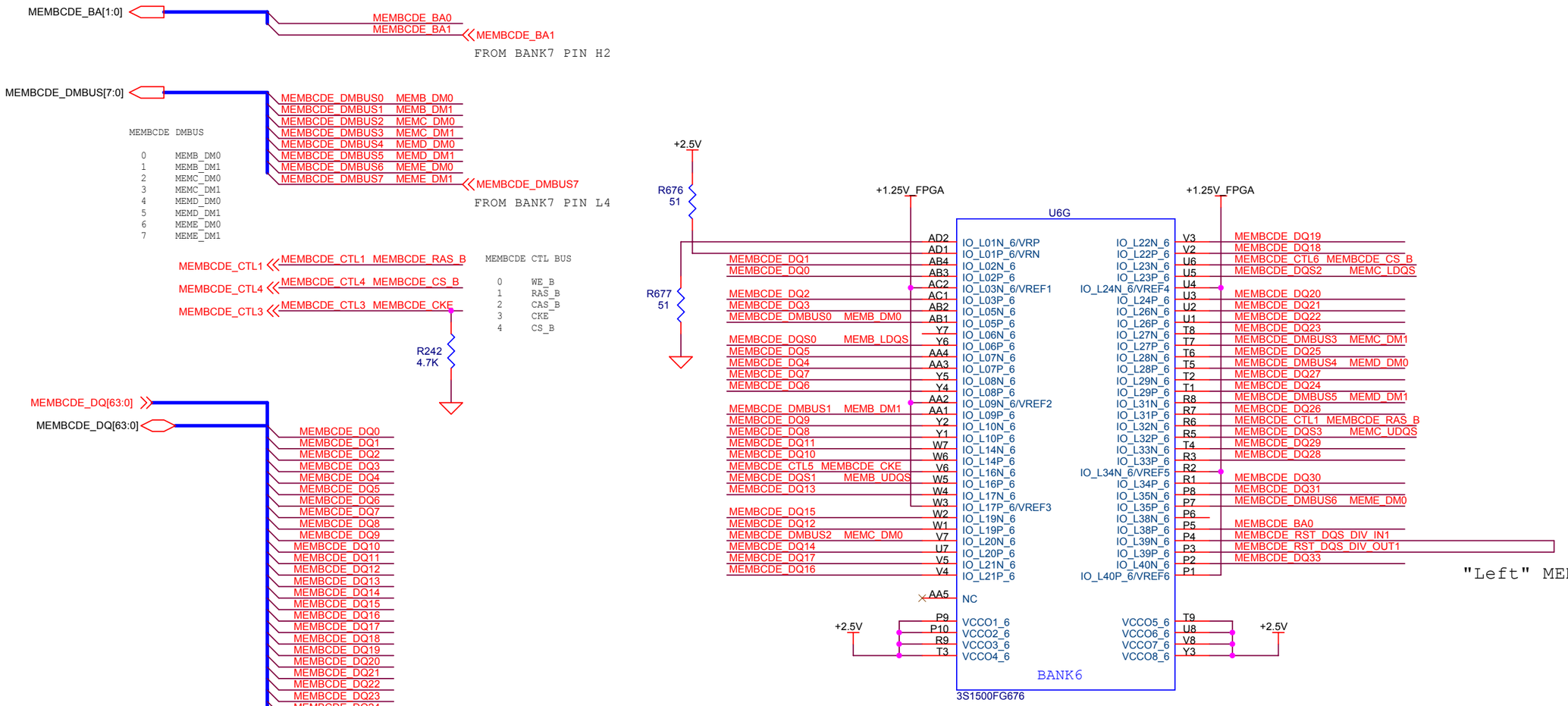
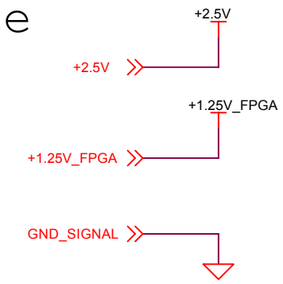


DDR1 x4 (MEMB - MEME) "Left" Side Interface

4 x 16-bit DDR-1 Mem
on the Left are designated:
MEMB = MEM DQS(0:1)
MEMC = MEM DQS(2:3)
MEMD = MEM DQS(4:5)
MEME = MEM DQS(6:7)



3S1500FG676 Bank6

Title: Spartan3 DDR-1 Board		
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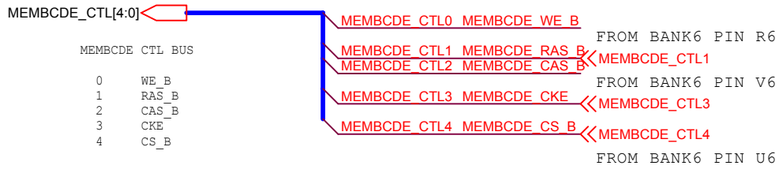
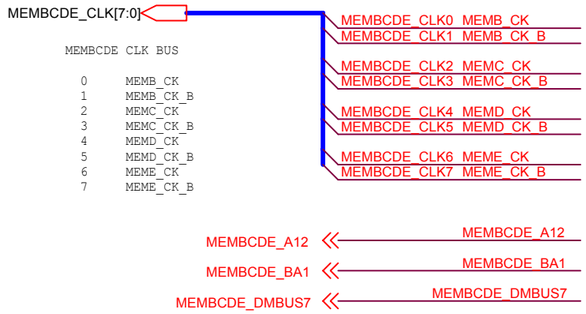
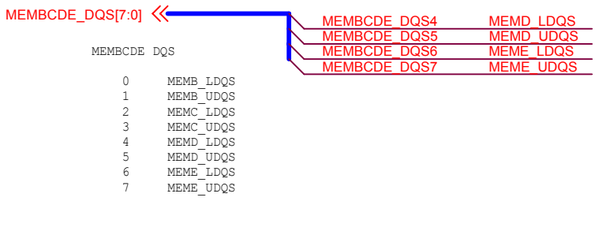
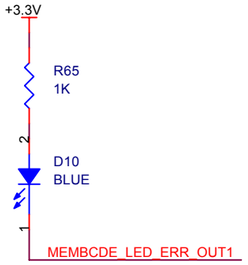
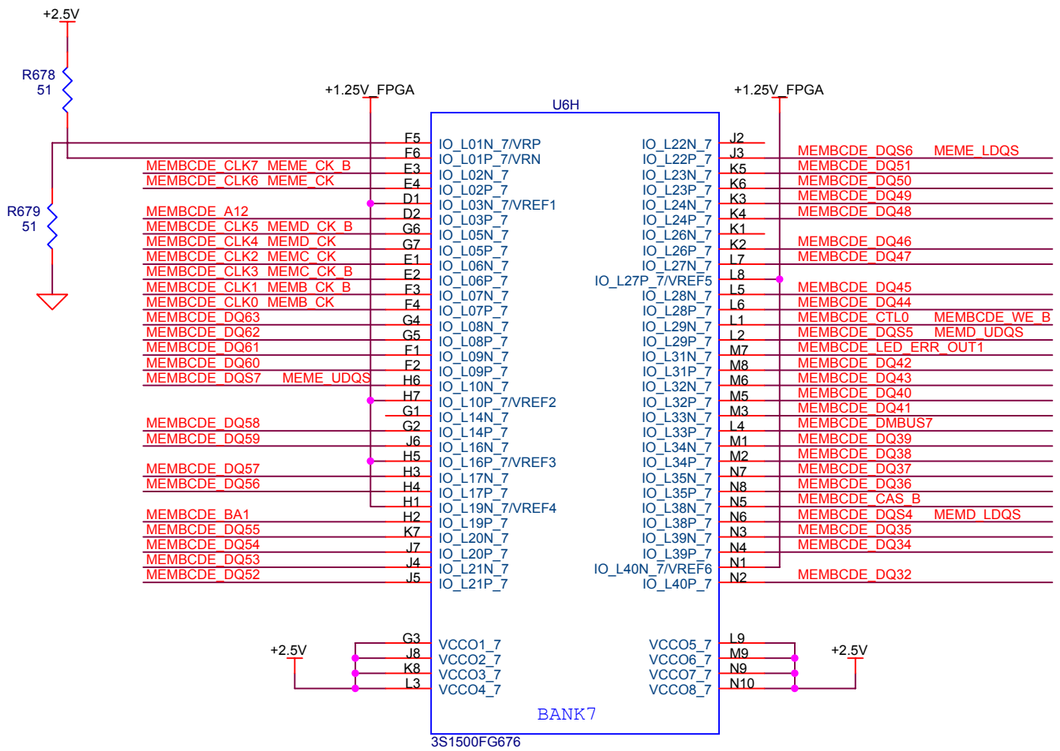




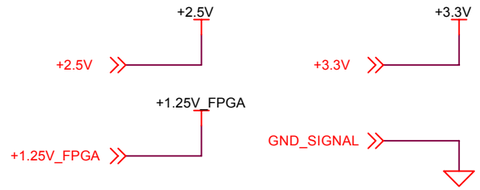






DDR1 x4 (MEMB - MEME) "Left" Side Interface

4 x 16-bit DDR-1 Mem
on the Left are designated:
MEMB = MEM DQS(0:1)
MEMC = MEM DQS(2:3)
MEMD = MEM DQS(4:5)
MEME = MEM DQS(6:7)



3S1500FG676 Bank7

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3S1500FG676 MISC

XCONFIG
P8
HEADER 9
+2.5V
GND
CCLK
DONE
DIN
PROG
INIT
R90 4.7K
10K R91
10K R92
10K R93
10K R94
PROG
SW PUSHBUTTON
SW5
SW3
SW DIP-3
M0
M1
M2
U6L
IO_L27N_4/DIN/D0
CCLK
IO_L01N_5/RDWR_B
IO_L01P_5/CS_B
M0
M1
M2
PROG_B
IO_L31N_4/INIT_B
DONE
IO_L31P_4/DOUT/BUSY
TDI
TDO
TMS
TCK
HSWAP_EN
MISC
3S1500FG676
Y15
AD26
AC5
AB5
AE3
AC3
AF3
D3
AC14
AC24
AD14
C1
D24
A24
B24
C2
R84 4.7K
FPGA_TDI
FPGA_TDO_OUT
FPGA_TMS
FPGA_TCK
R720 4.7K
R721 4.7K
R722 4.7K
R723 4.7K
SYSACE_TDO
FPGA_TDO
TCK
TMS
R363 100
R364 100
R365 100
R366 100
100 R99
100 R100
SYSACE_CFGPROG_B
SYSACE_CFGINIT_B
4.7K R86
1K R87
D11 BLUE
DONE
Q3 BSS138
4.7K R88
1K R89
D12 BLUE
INIT
Q4 BSS138
GND_SIGNAL

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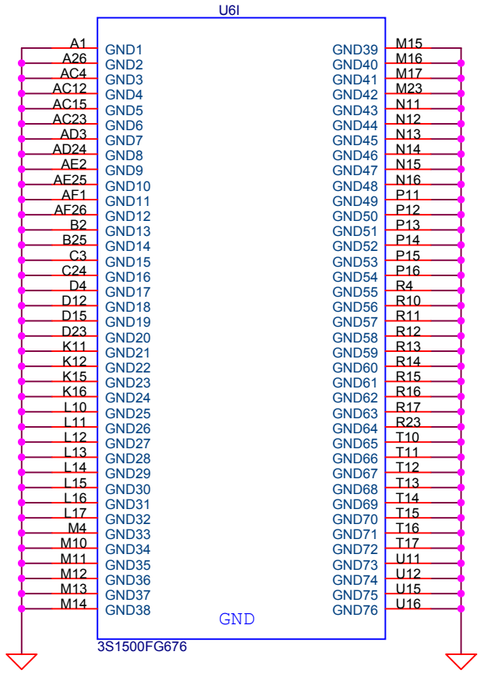

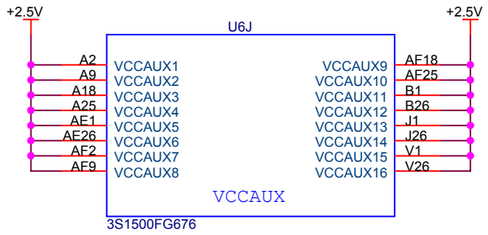

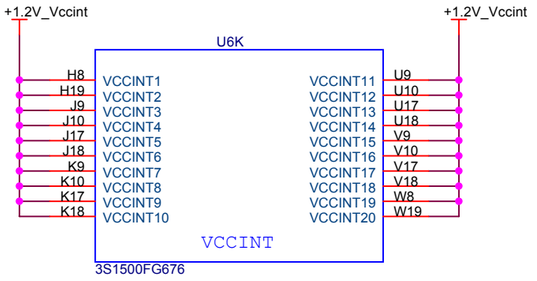

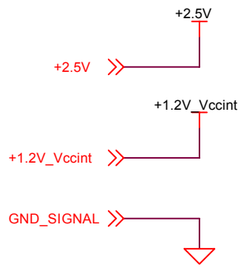

3S1500FG676 GND, VCCAUX, VCCINT

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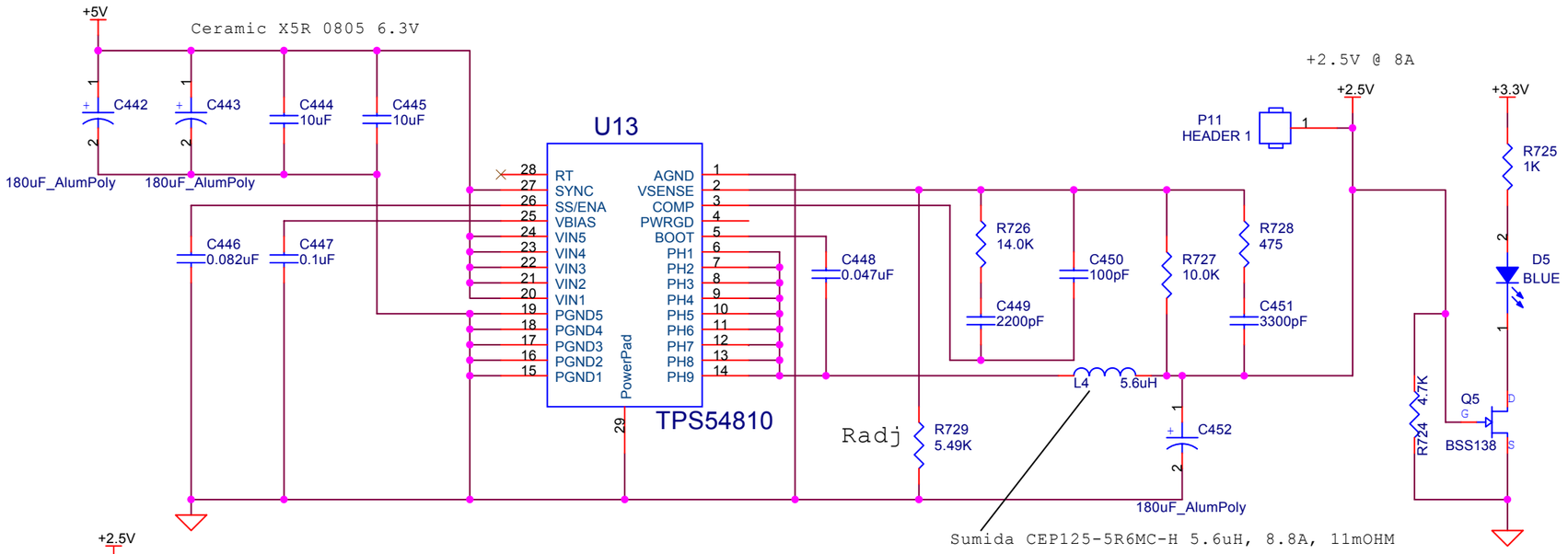
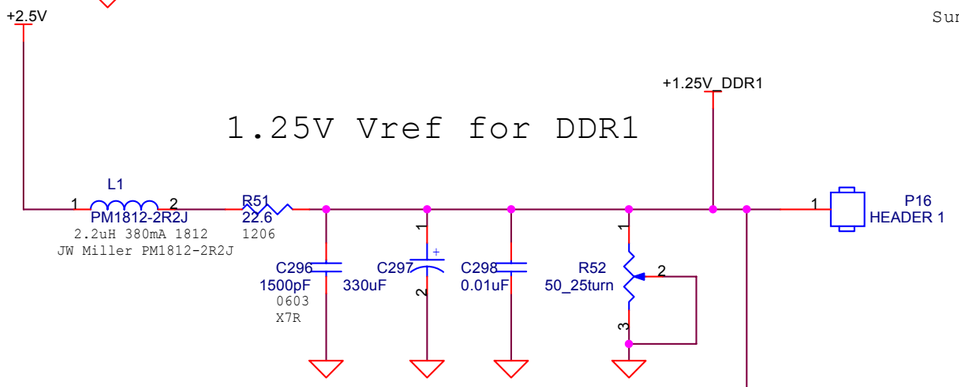
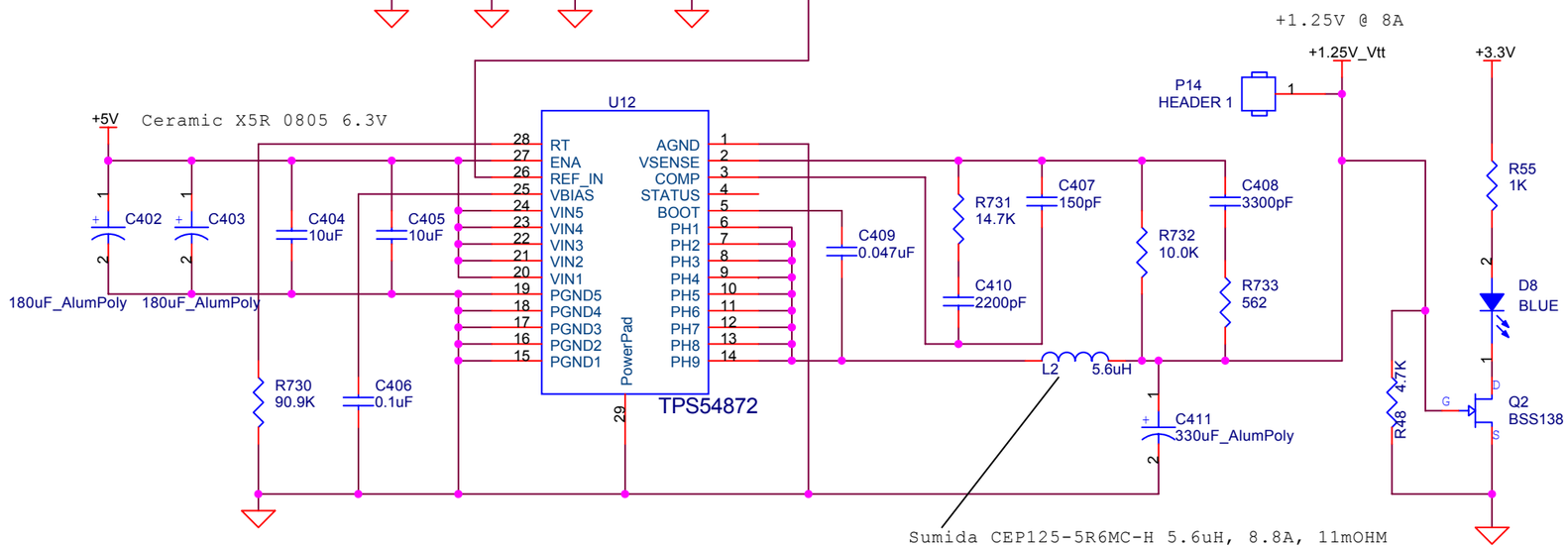
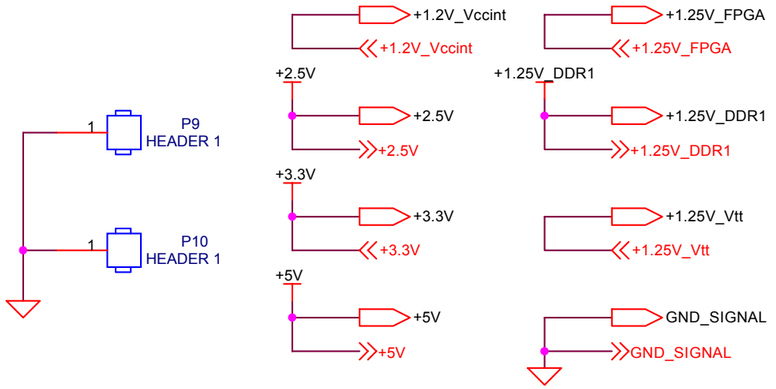


Power Requirements:			
Item:	Purpose:	Voltage:	Current:
XC3S1500	Vccaux	2.5V	70mA (typ)
	Vcco	2.5V	1.68A(typ)
	Vccint	1.2V	1.52A(typ)
MT46V16M16	Vdd/Vddq	2.5V	2.2A (wc)
MT5VDDT1672	Vdd	2.5V	2.2A (wc)
Mem.Term.R's	Vtt	1.25V	8.1A (wc)
LEDs, Misc.	3.3V	3.3V	200mA(typ)

2.5V Adjust Resistor (Radj)			
Vout		Std.1%R	Calc Vout
2.375V	-5%	6.04K	2.366V
2.500V	Nom	5.49K	2.514V
2.625V	+5%	5.11K	2.635V







LOCAL POWER REGULATION

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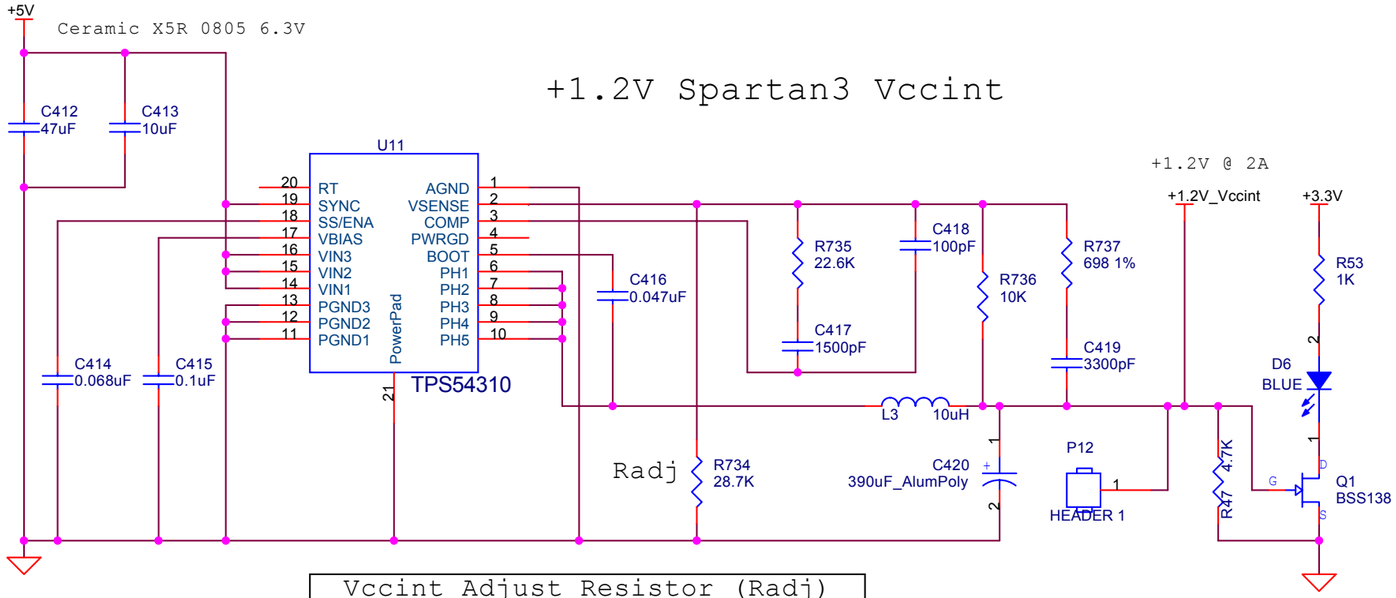
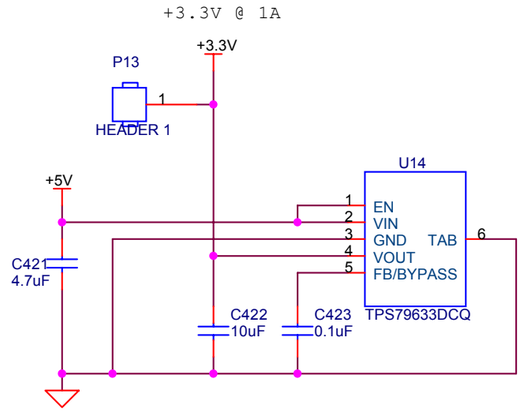
LOCAL POWER REGULATION

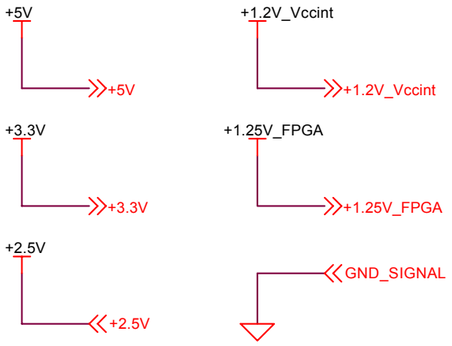
+1.2V Spartan3 Vccint

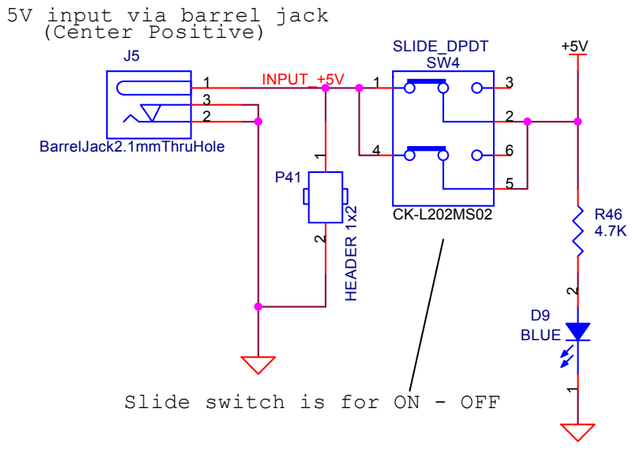


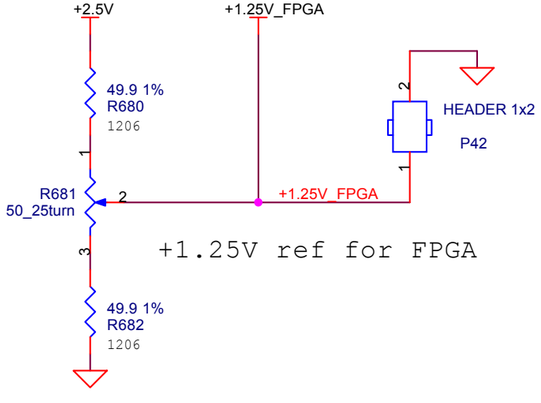
Vccint Adjust Resistor (Radj)			
Vout		Std.1%R	Calc Vout
1.140V	-5%	35.7K	1.141V
1.200V	Nom	28.7K	1.201V
1.260V	+5%	24.0K	1.262V

+3.3V (SysAce,LCD I/F,7-Seg,LED's)









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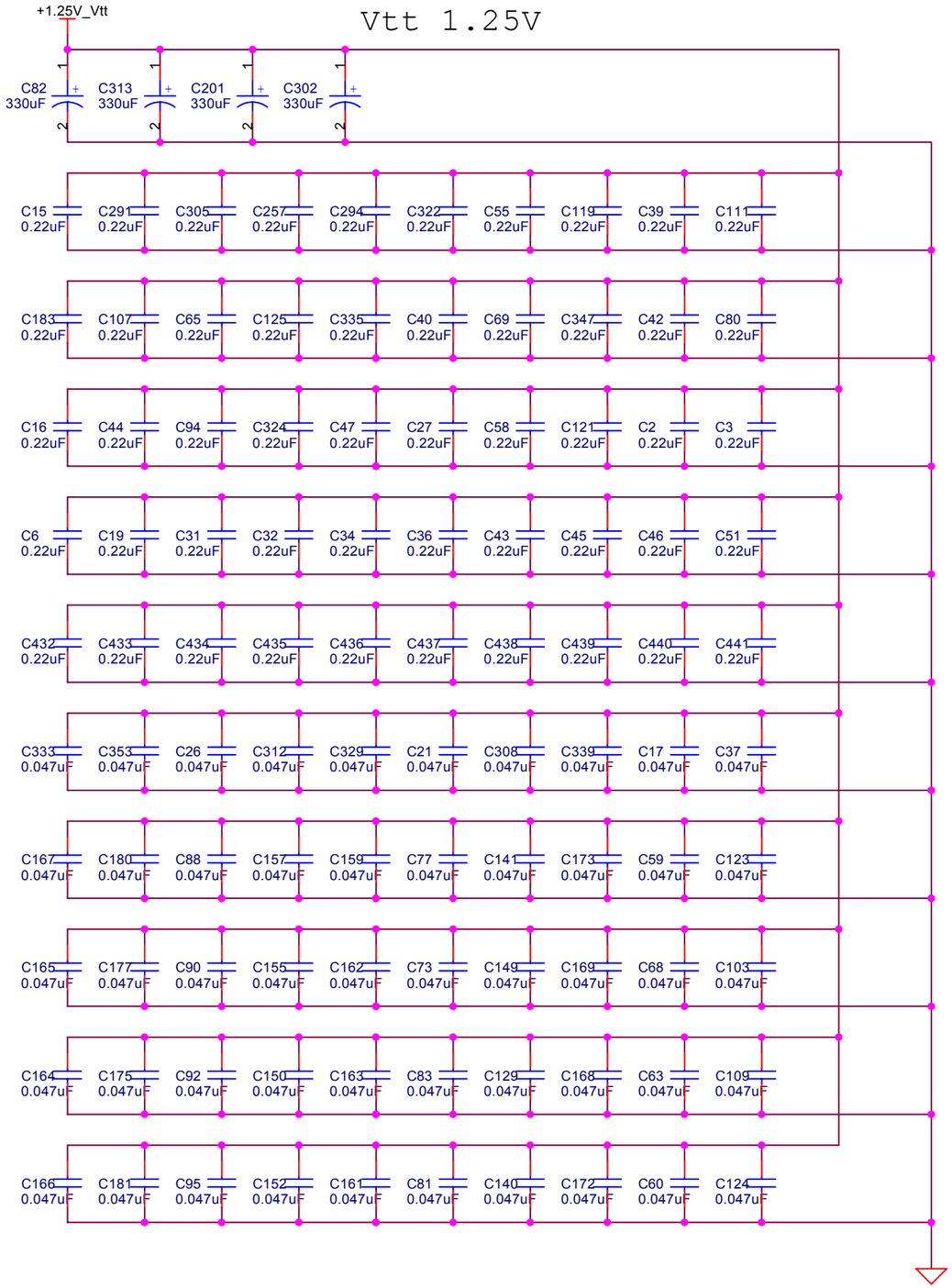
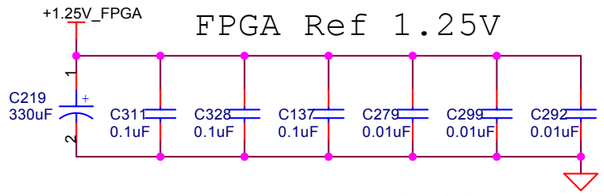
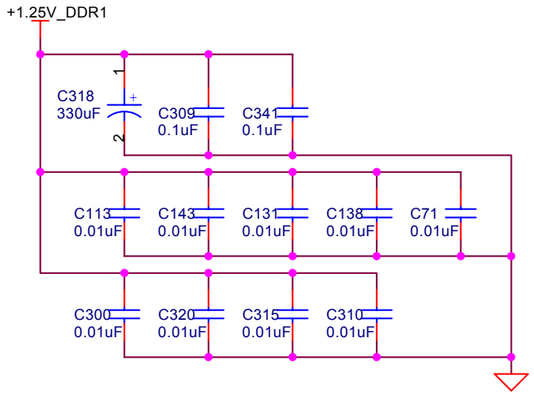
Vtt 1.25V

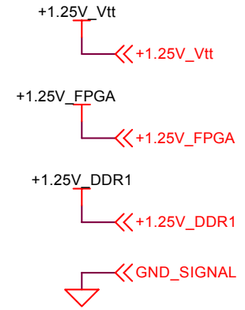


FPGA Ref 1.25V



DDR1 Ref 1.25V





DECOUPLING

ALL non-Tantalum caps are X7R or X5R

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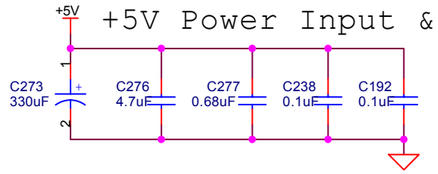
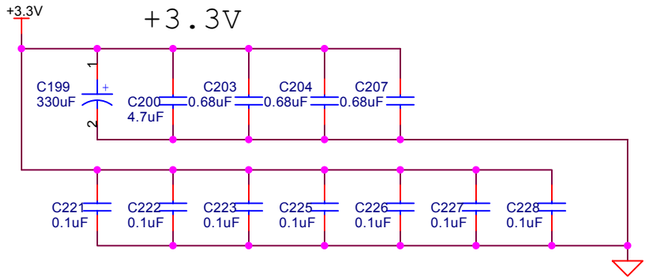
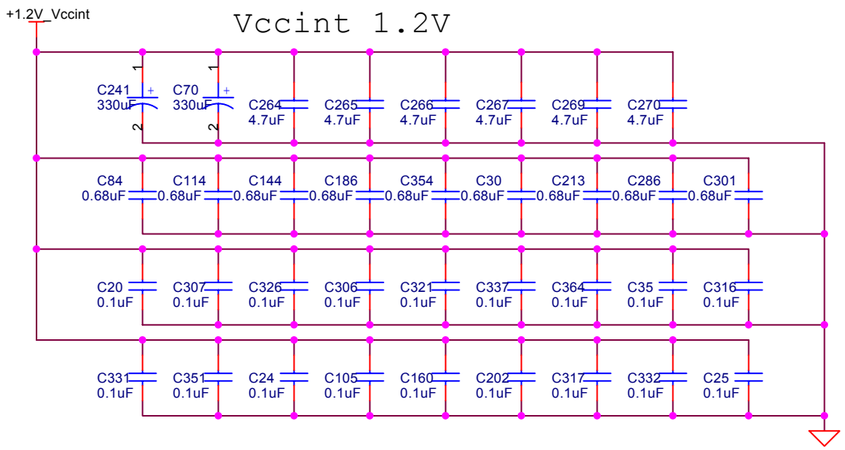
+5V Power Input & LCD



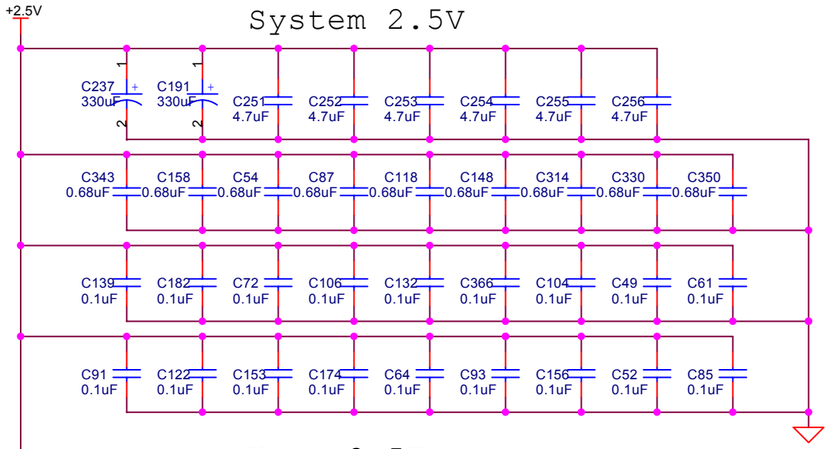
+3.3V



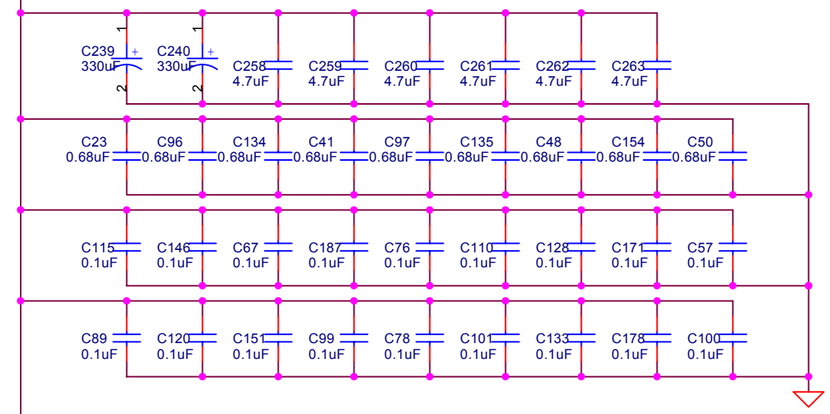
Vccint 1.2V



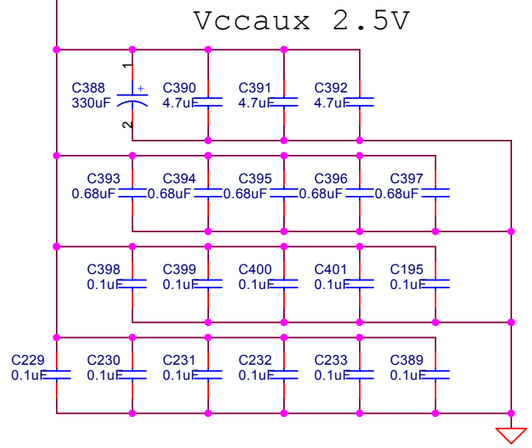
System 2.5V

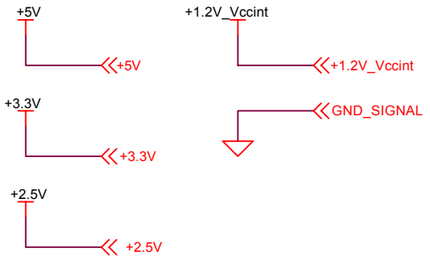


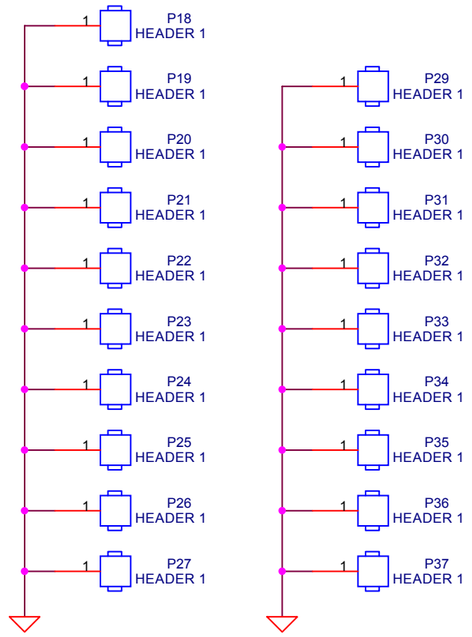
Vcco 2.5V



Vccaux 2.5V







DECOUPLING

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Rev#	Sheet#	Description
0	All	Initial Release
1	2	Changed bus widths DIMM_DQ, DIMM_DQS, DIMM_DM
	15	Changed bus widths DIMM_DQ, DIMM_DQS, DIMM_DM
	16	Changed bus widths DIMM_DQ, DIMM_DQS, DIMM_DM
	21	Changed bus widths DIMM_DQ, DIMM_DQS, DIMM_DM
	22	Changed bus widths DIMM_DQ, DIMM_DQS, DIMM_DM
2	Misc	Updates resulting from schematic review
3	Misc	Replaced discrete 0402 50 ohm memory bus term R's with Rpaks
	15	Added 0 ohm R738 connecting DIMM_CKE0 to CKE1 pin
4	27	Correct wiring error: TCK and TMS were swapped
5	30	Change R values to 50 ohms: R680,R681(trimpot),R682
6	32	Delete GND test pin P28

Rev Notes

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