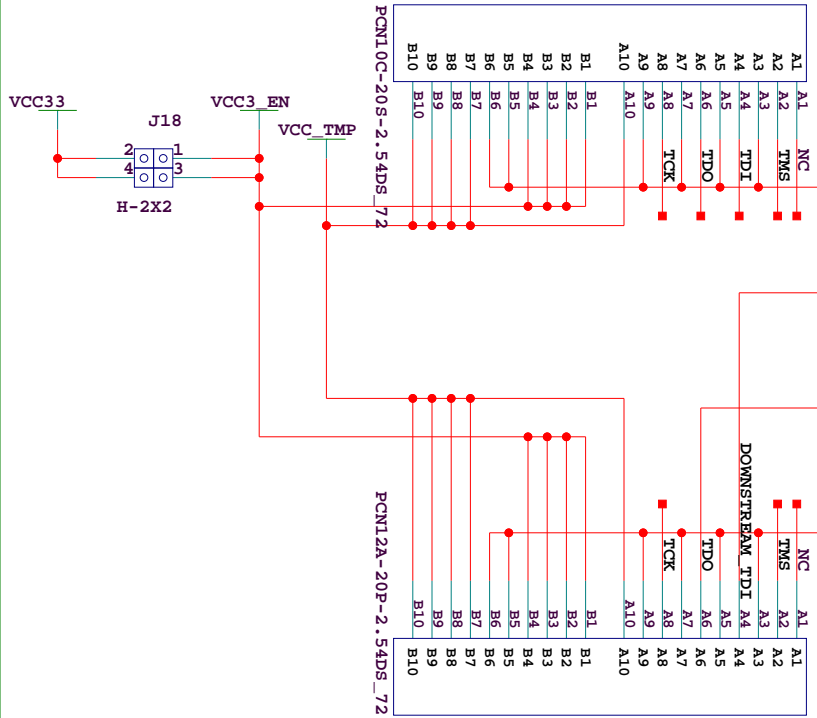
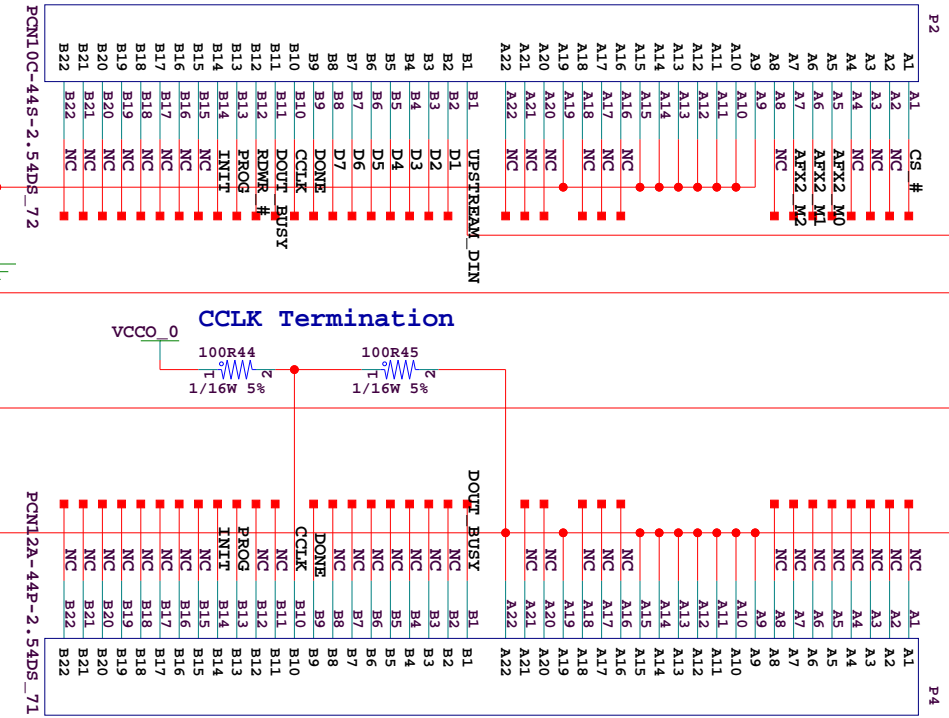
		SCH P/N	0381233
		ART P/N	0531592
		FAB P/N	1280404
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404 BLOCK DIAGRAM			
Date: 9-26-2006_10:34		Ver: C	
Sheet Size: B		Rev: 02	
Sheet 1	of 21	Drawn By s.s.	

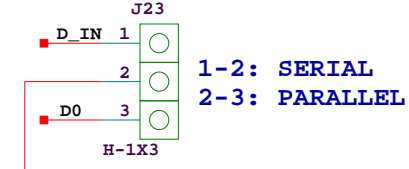
SYSTEM ACE UPSTREAM



UPSTREAM CONNECTORS

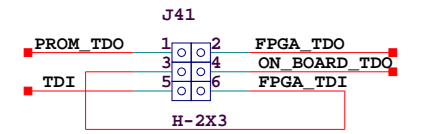


DOWNSTREAM CONFIG



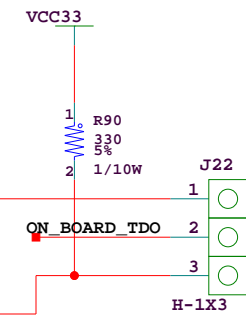
ON BOARD JTAG CHAIN SELECTION

PROM JTAG FPGA JTAG
 1-3: Enable 2-4: Enable
 3-5: Disable 4-6: Disable

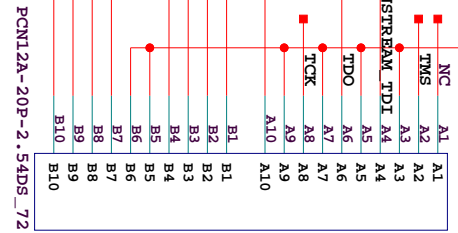


1-2: SERIAL CHAINING TO NEXT BOARD
 2-3: TERMINATION OF LAST BOARD IN THE CHAIN

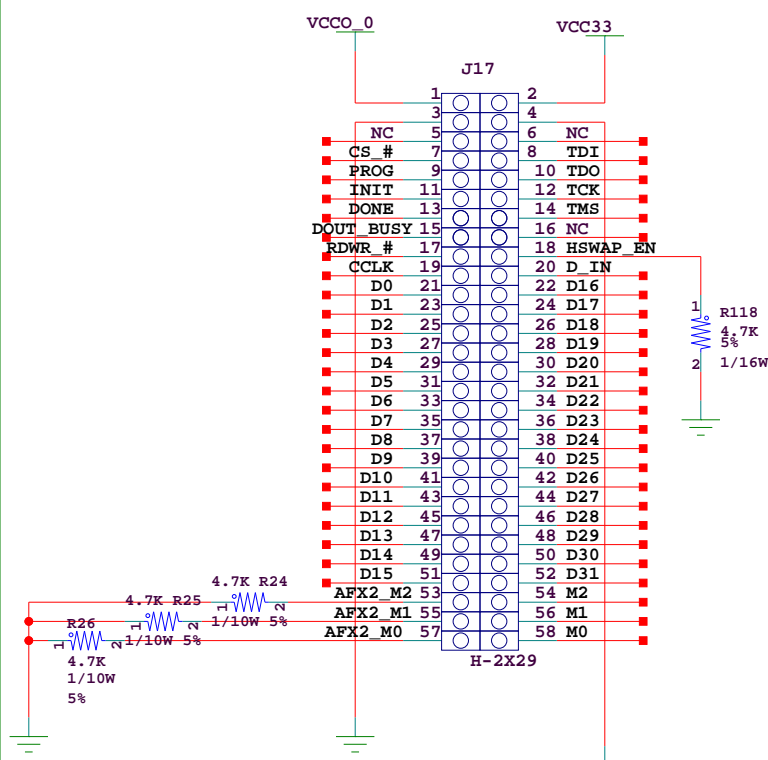
JTAG JUMPER



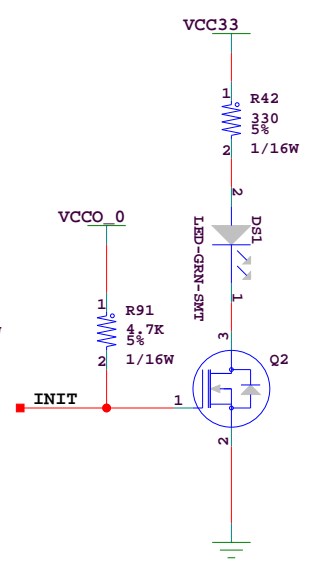
SYSTEM ACE DOWNSTREAM DOWNSTREAM CONNECTORS



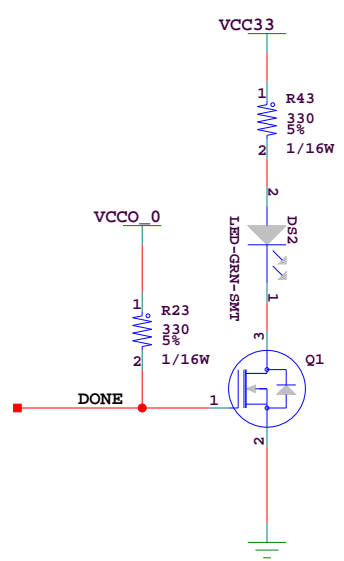
FLYING WIRE CONFIGURATION PORT



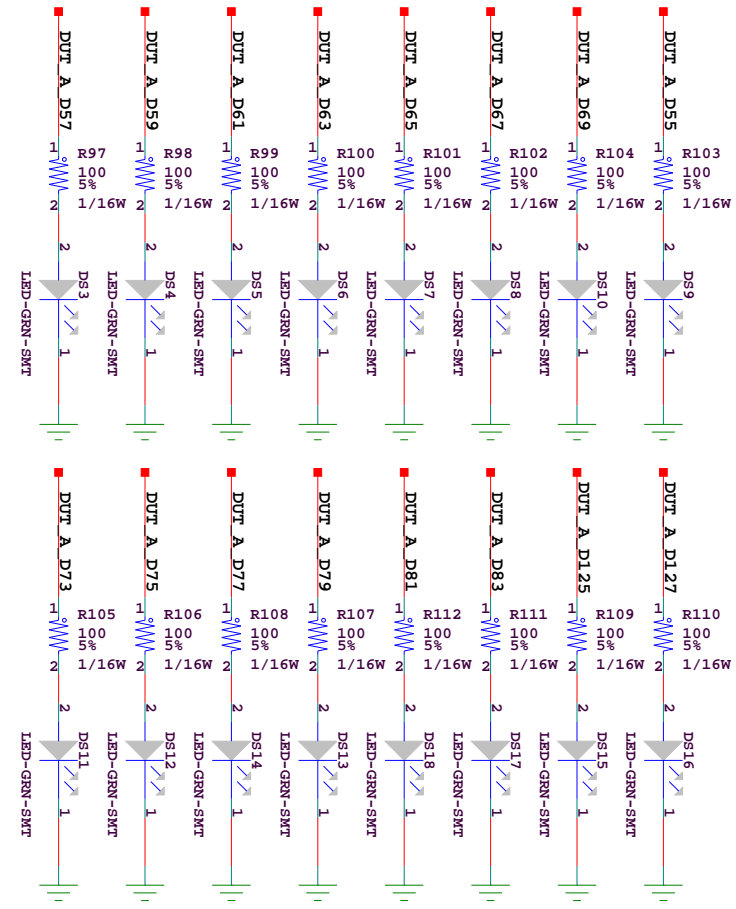
INIT LED



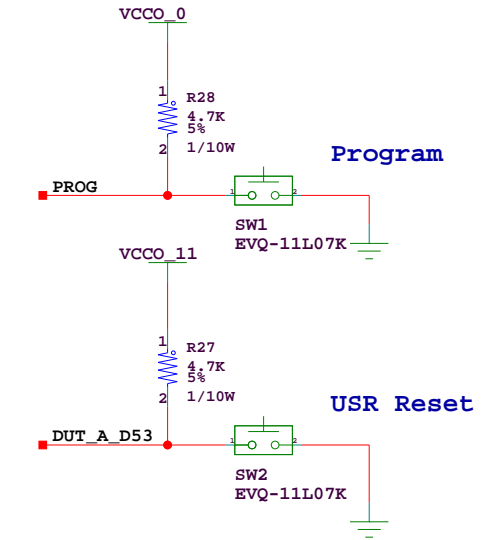
DONE LED



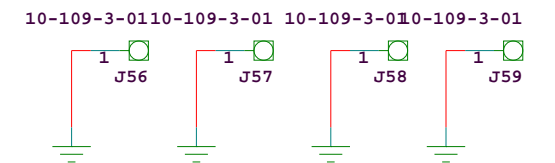
USER LED'S



SWITCHES

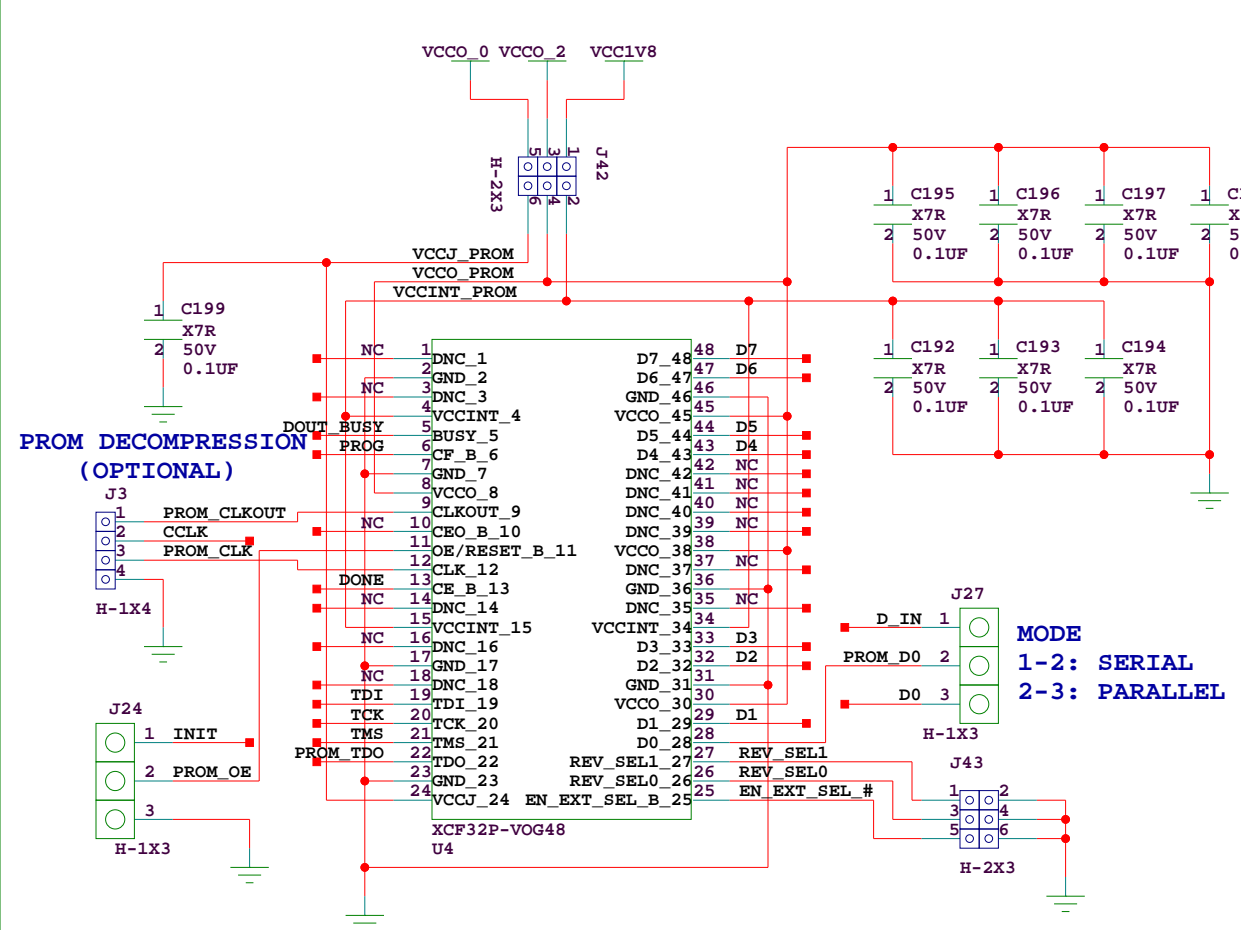


TEST POINTS

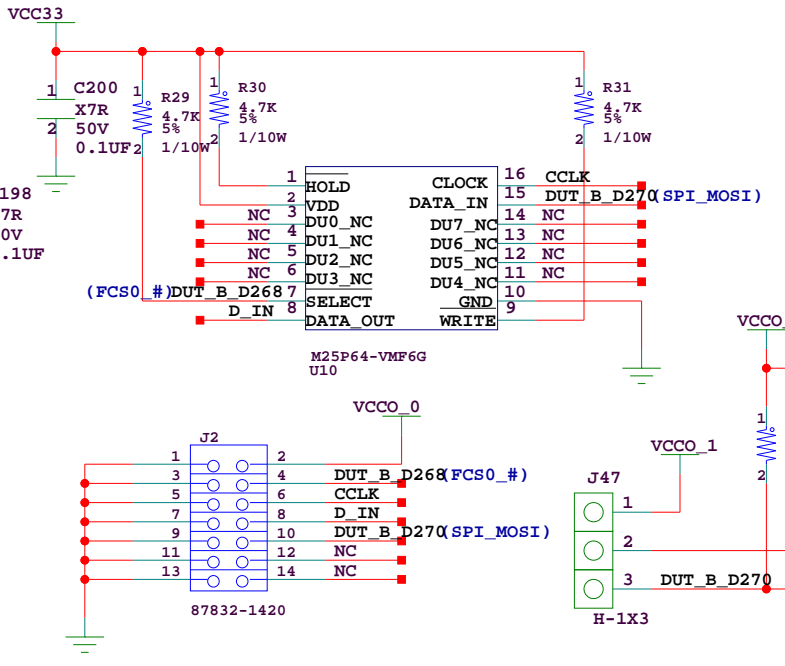


		SCH P/N	0381233
		ART P/N	0531592
		FAB P/N	1280404
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404 DIN CONN, PORTS, STATUS LEDS, SWITCHES			
Date:	2-19-2008_12:14	Ver:	C
Sheet Size:	B	Rev:	02
Sheet	2 of 21	Drawn By	s.s.

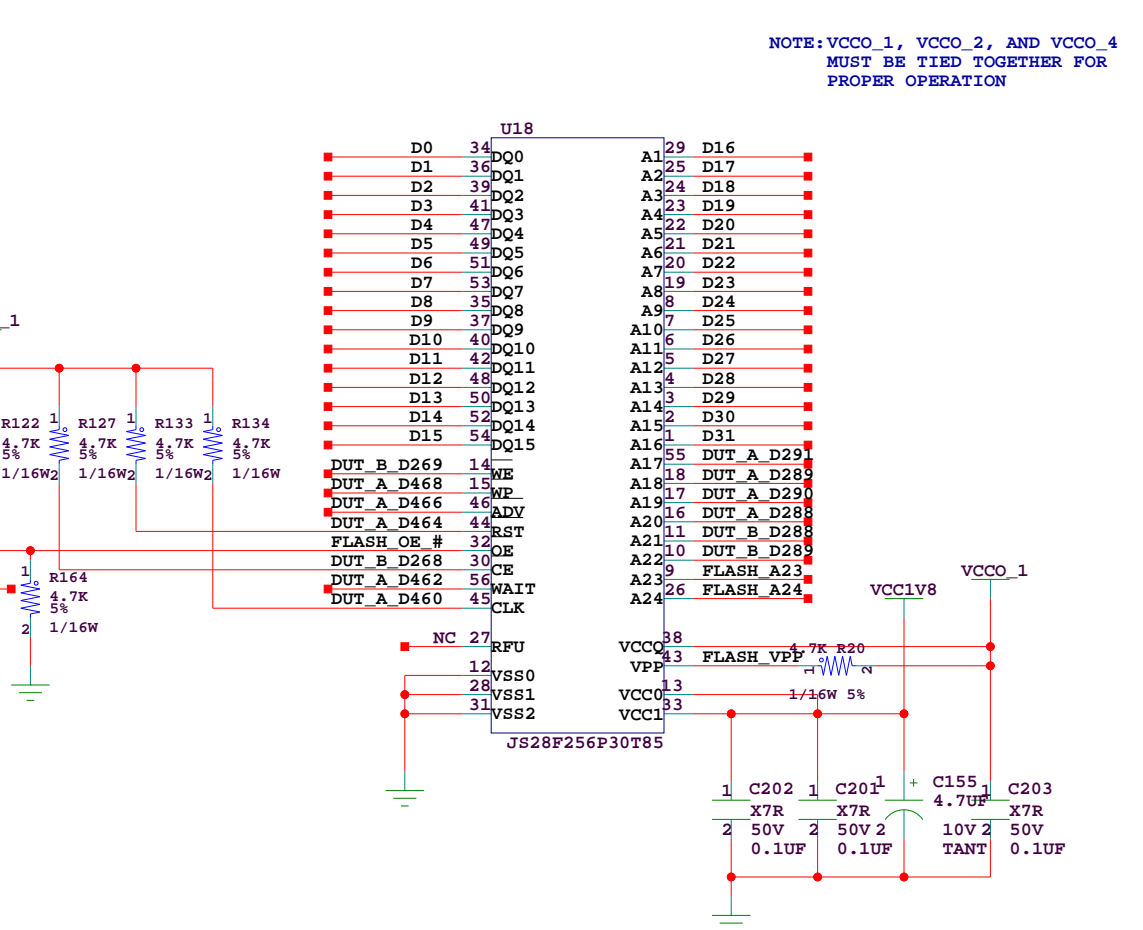
CONFIGURATION PROM



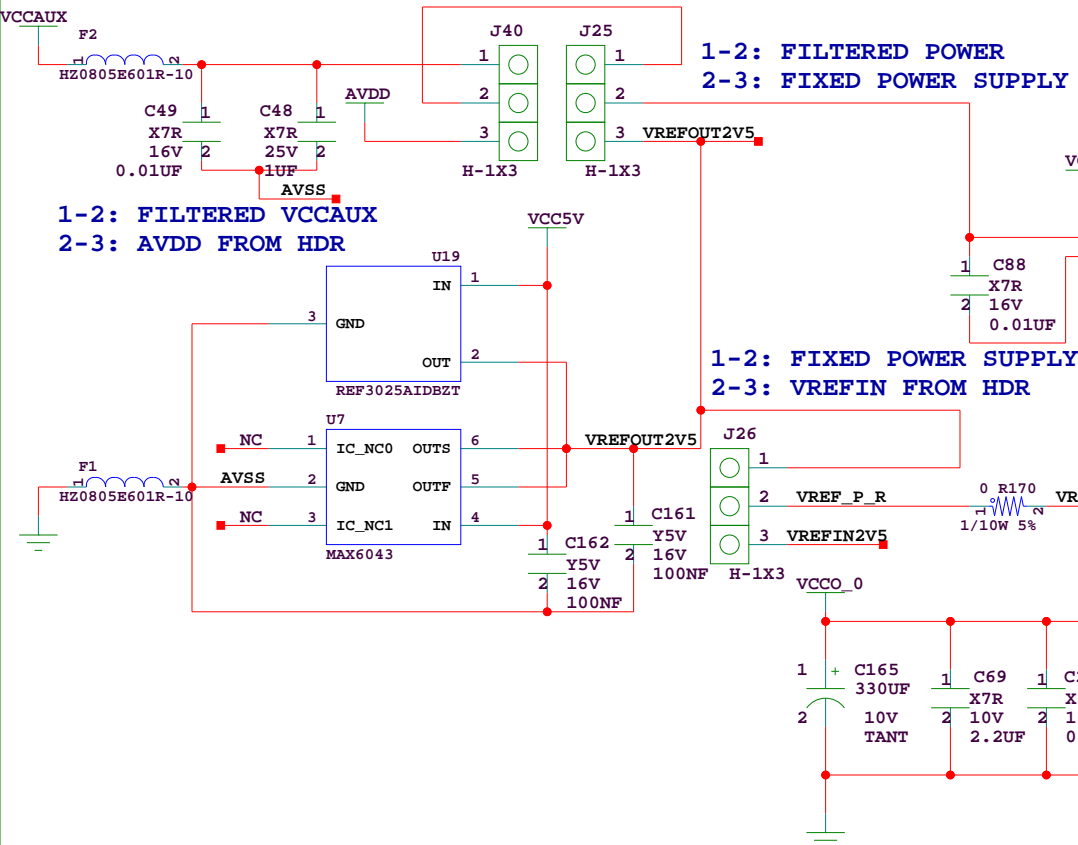
SPI INTERFACE



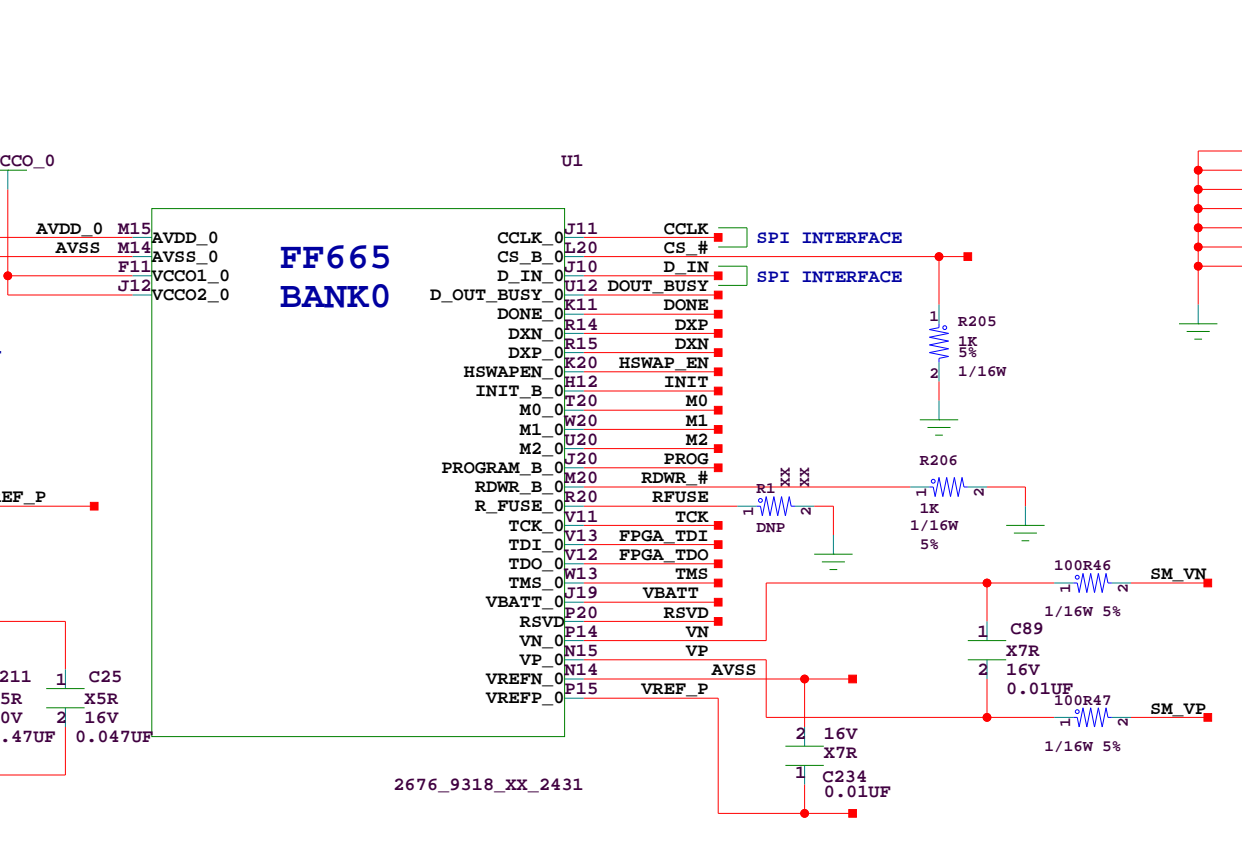
BPI INTERFACE



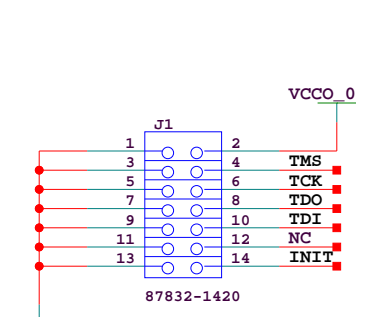
SYSTEM MONITOR SUPPLY



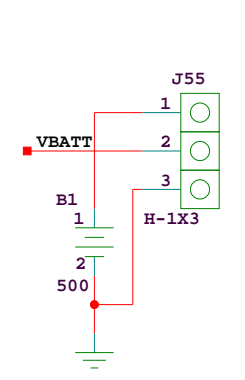
FPGA BANK0 CONFIGURATION



PARALLEL 4 CABLE CONNECTOR



VBATT Supply



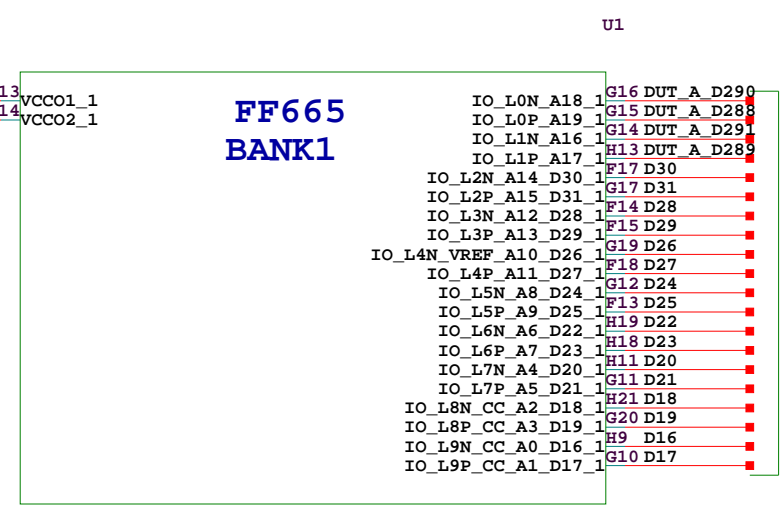
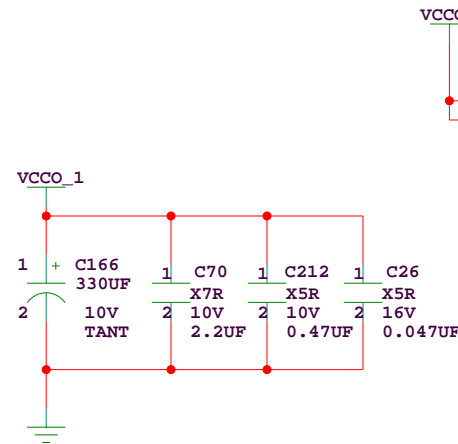
XILINX

SCH P/N 0381233
 ART P/N 0531592
 FAB P/N 1280404

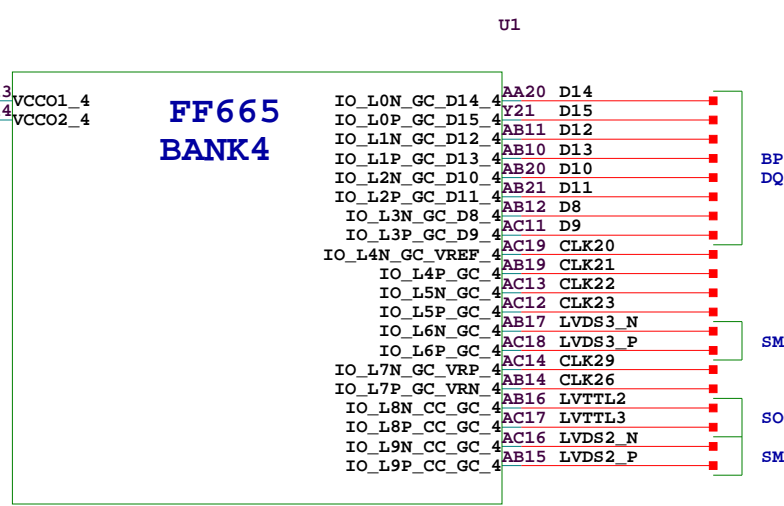
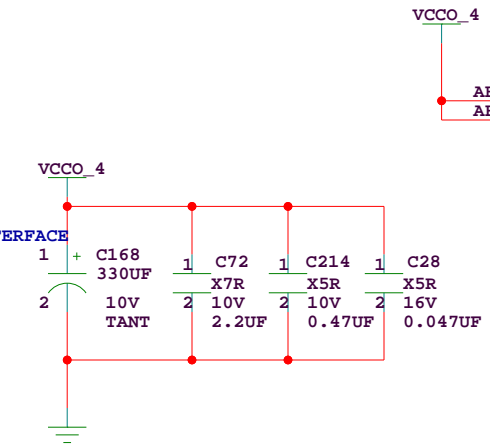
Title:
 SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404

CONFIGURATION

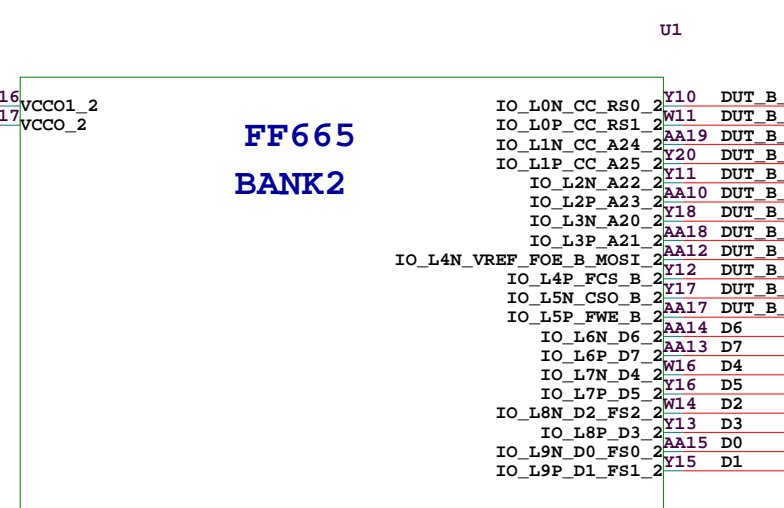
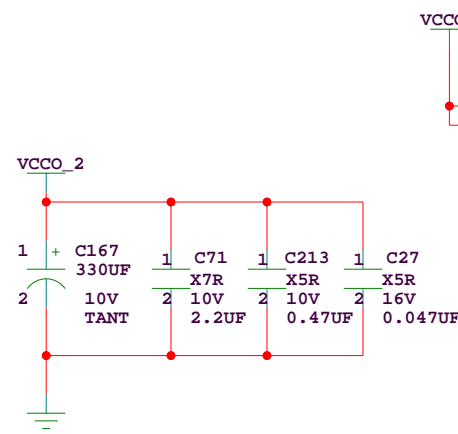
Date: 2-19-2008_12:14	Ver: C
Sheet Size: B	Rev: 02
Sheet 3 of 21	Drawn By s.s.



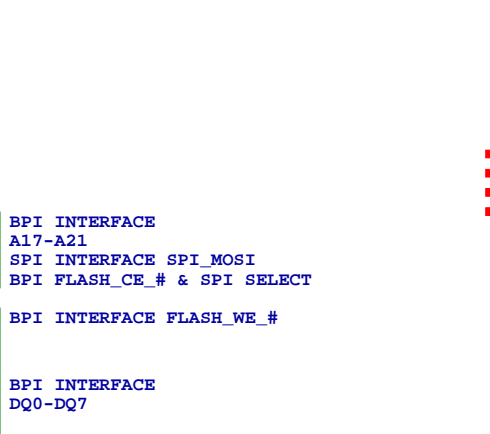
2676_9318_XX_2431



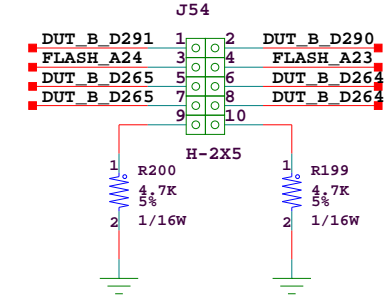
2676_9318_XX_2431



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BPI REVISION SELECT PINS

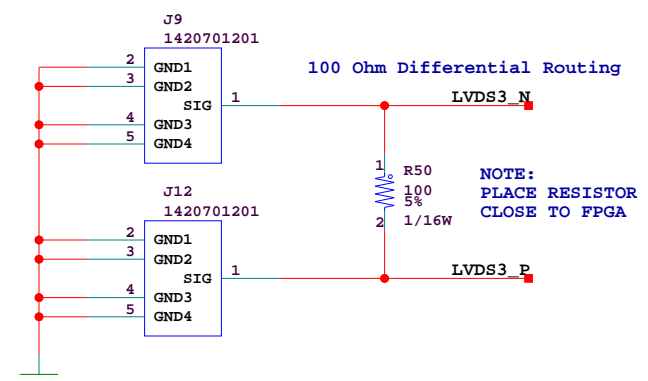
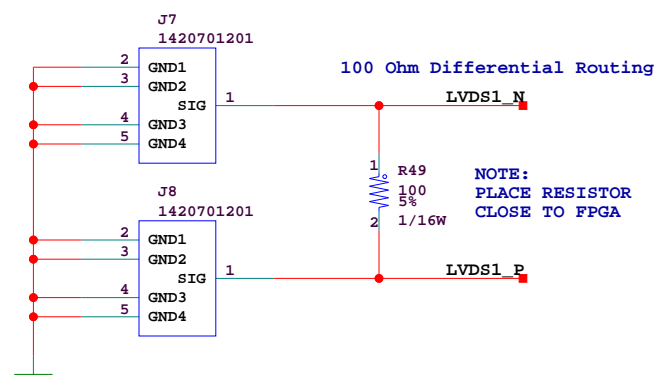
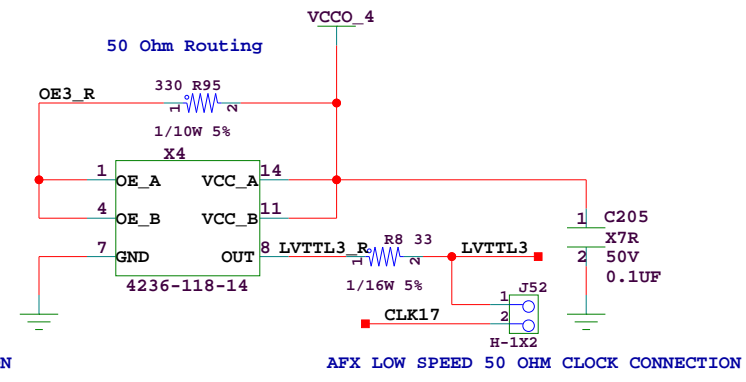
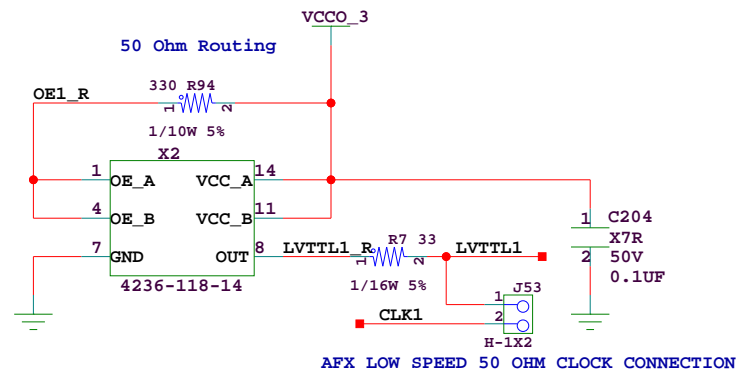
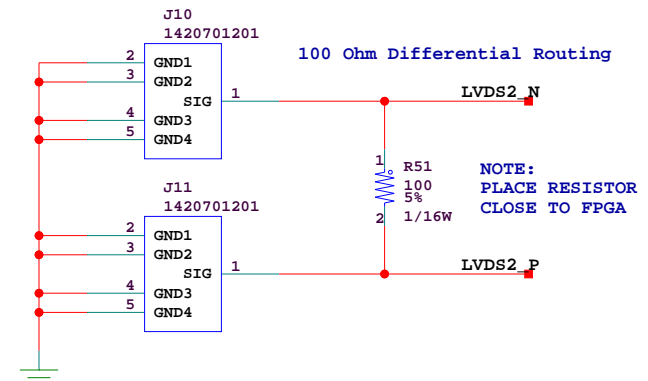
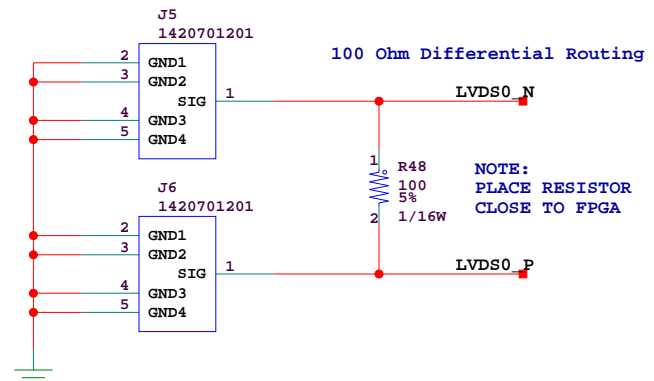
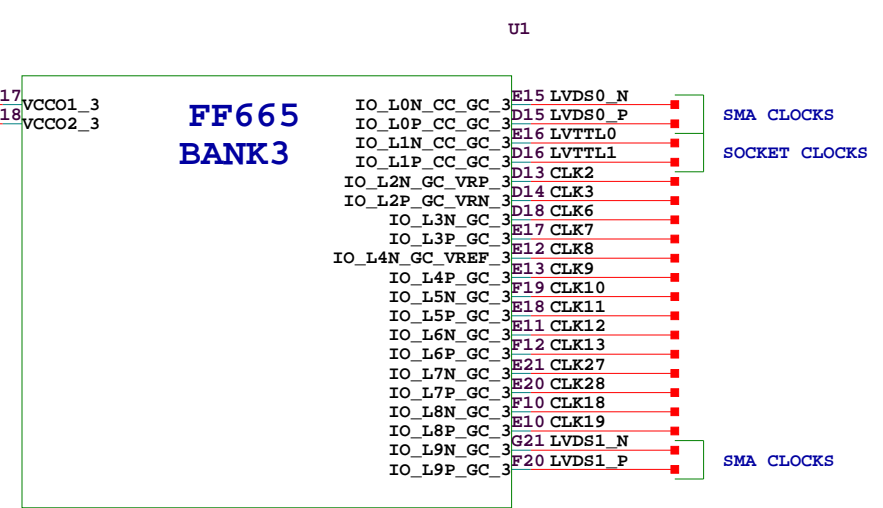
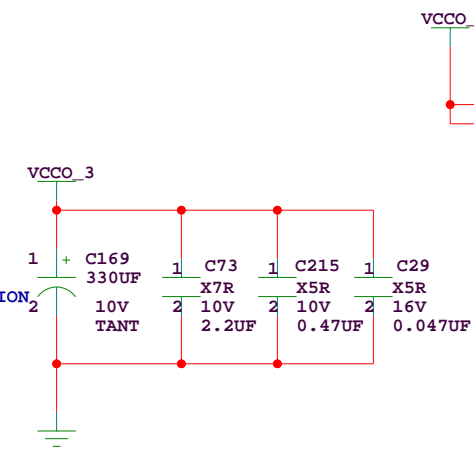
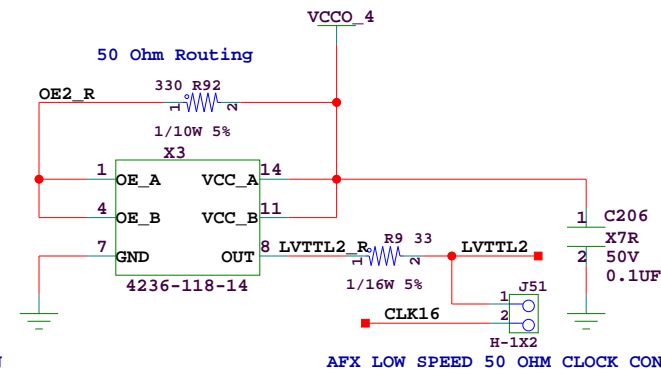
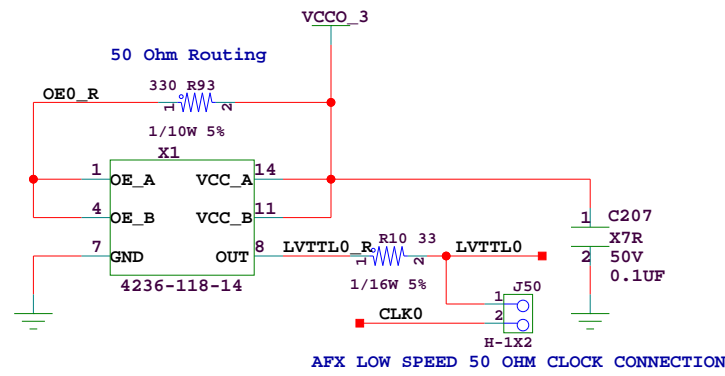


- 1-3: Selects ADDR23 from FPGA to FLASH ADDR24
- 3-5: Selects RS1 from FPGA to FLASH ADDR24
- 7-9: Pulldown for RS applications
- 2-4: Selects ADDR22 from FPGA to FLASH ADDR23
- 3-5: Selects RS0 from FPGA to FLASH ADDR23
- 8-10: Pulldown for RS applications

		SCH P/N	0381233
		ART P/N	0531592
		FAB P/N	1280404
<p>Title:</p> <p style="text-align: center;">SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404</p> <p style="text-align: center;">CONFIGURATION</p>			
Date:	2-19-2008_12:14	Ver:	C
Sheet Size:	B	Rev:	02
Sheet	4 of 21	Drawn By	s.s.

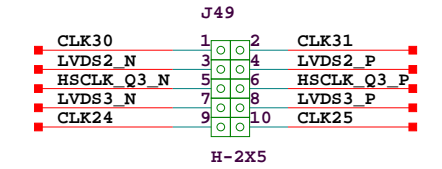
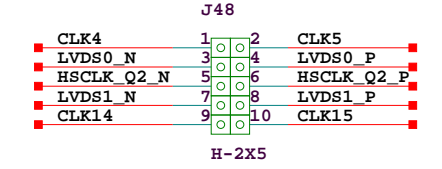
UPPER CLOCKS

BOTTOM CLOCKS



AFX CLOCK CONFIGURATION

- 1-3, 2-4: LOW SPEED 50 OHM CLOCK CONNECTION
- 3-5, 4-6: HIGH SPEED 100 OHM DIFFERENTIAL CLOCK CONNECTION TO DIFFERENTIAL PAIR
- 5-7, 6-8: HIGH SPEED 100 OHM DIFFERENTIAL CLOCK CONNECTION TO DIFFERENTIAL PAIR
- 7-9, 8-10: LOW SPEED 50 OHM CLOCK CONNECTION

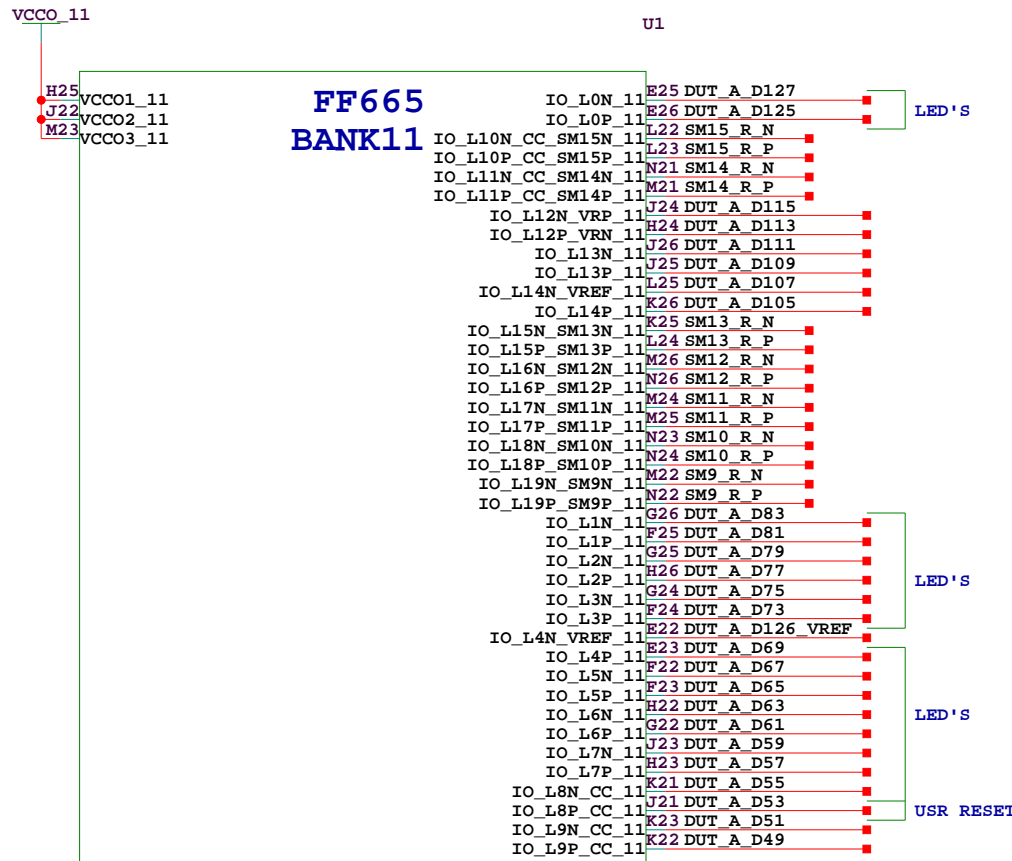


XILINX

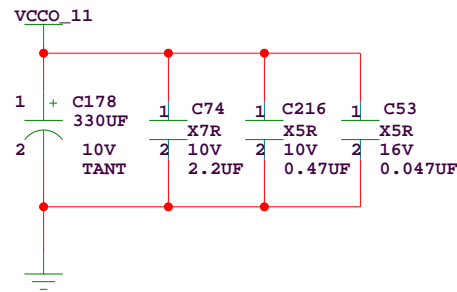
SCH P/N 0381233
ART P/N 0531592
FAB P/N 1280404

Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404
SOCKET CLOCKS, SMA DIFF CLOCKS

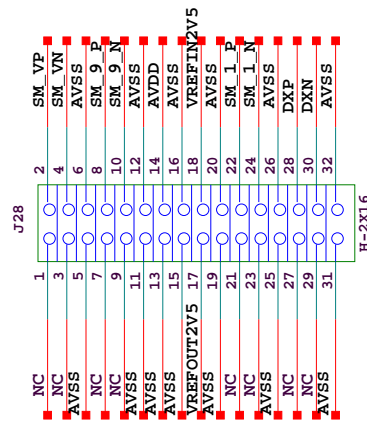
Date: 2-19-2008_12:14 Ver: C
Sheet Size: B Rev: 02
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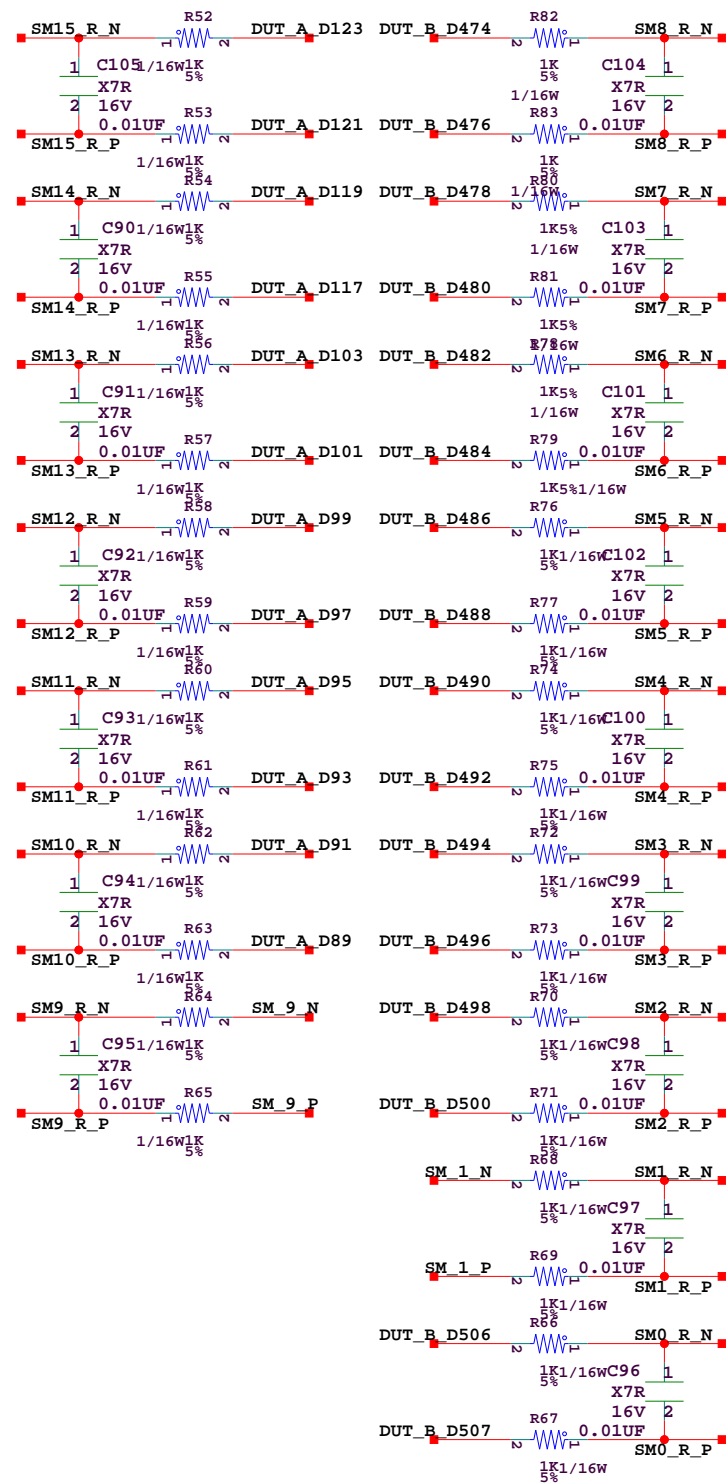
2676_9318_XX_2431



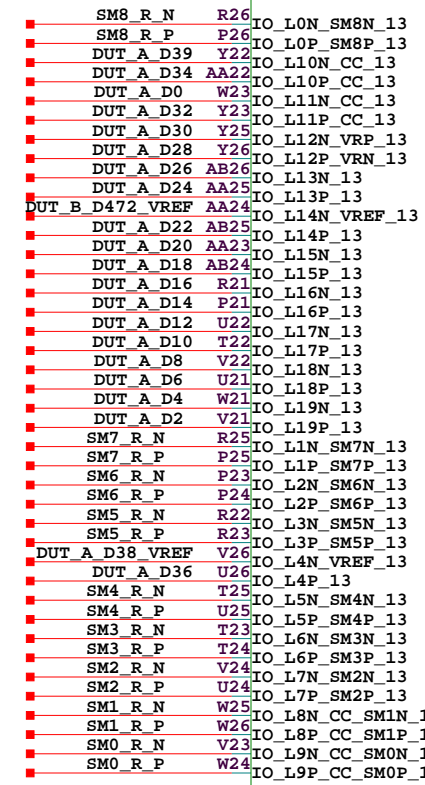
SYSTEM MONITOR MALE CONNECTOR



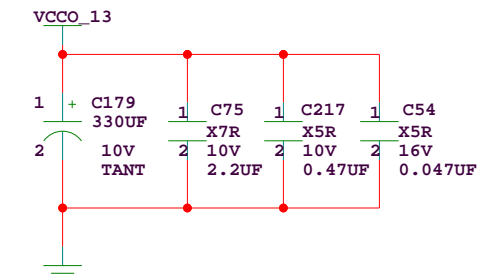
SYSTEM MONITOR FILTERS



U1



2676_9318_XX_2431

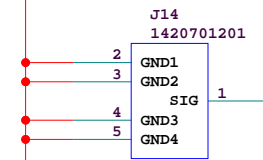
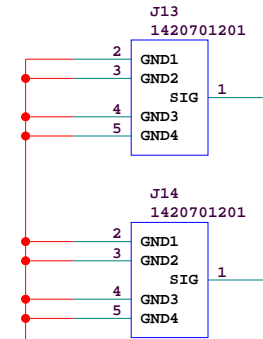
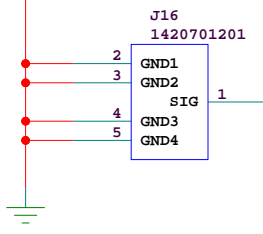
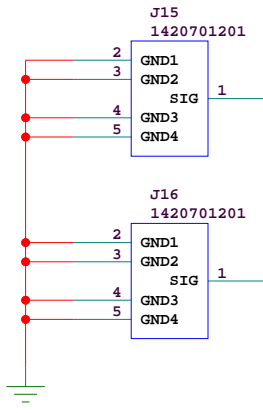
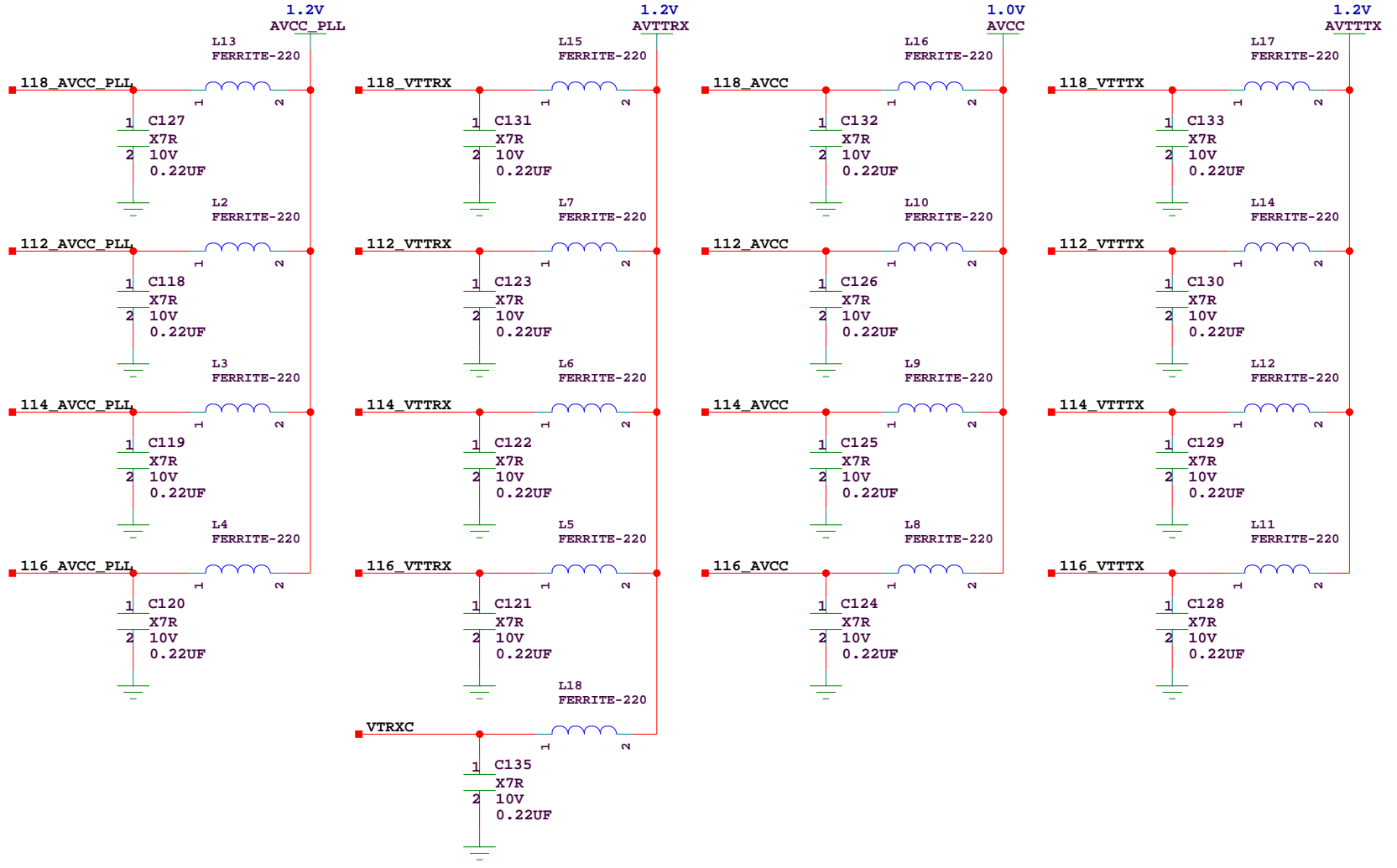
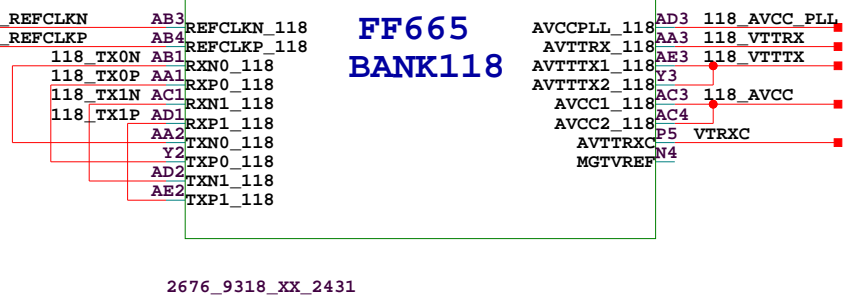
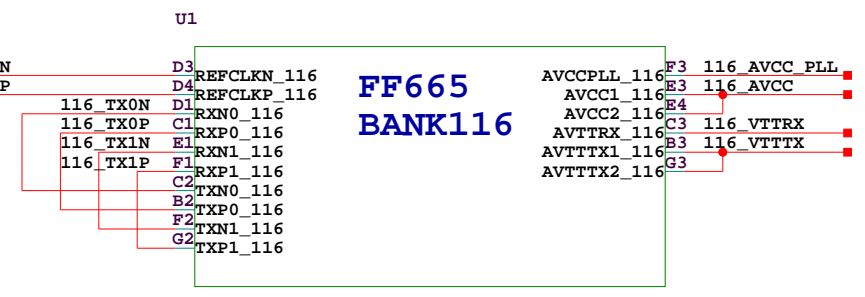
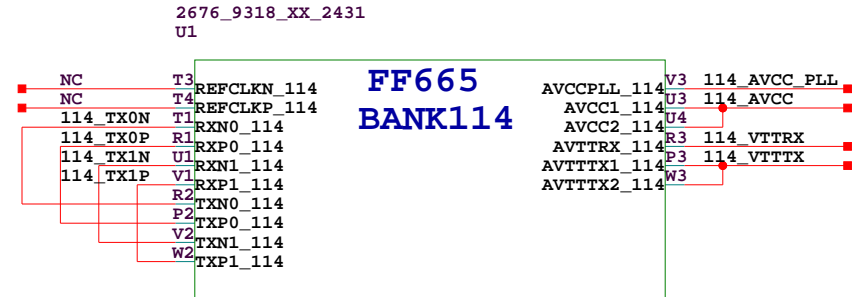
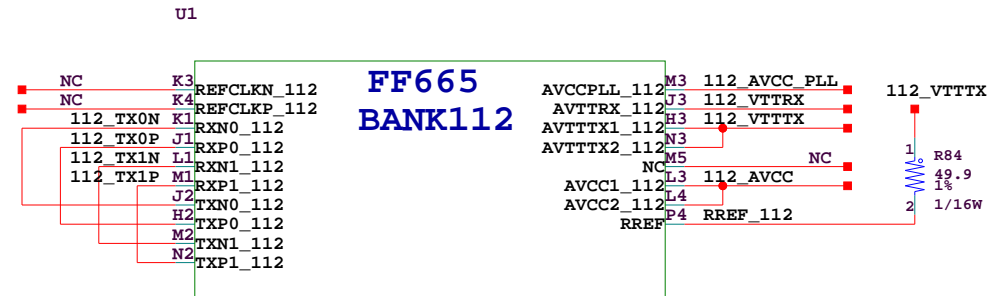


SCH P/N 0381233
 ART P/N 0531592
 FAB P/N 1280404

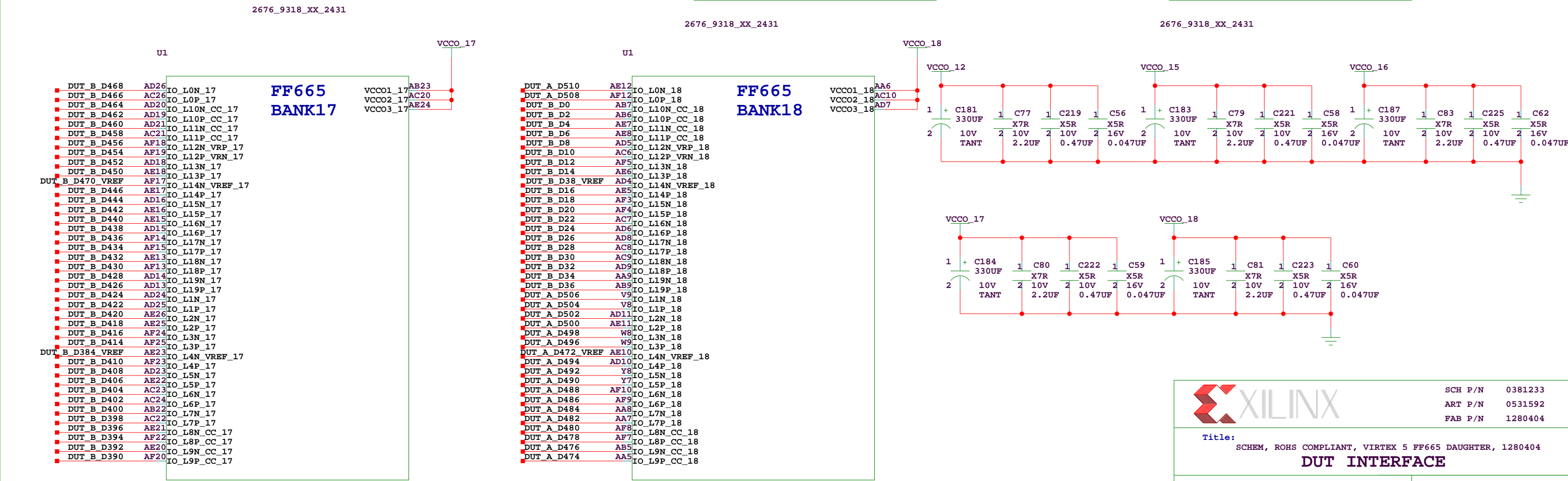
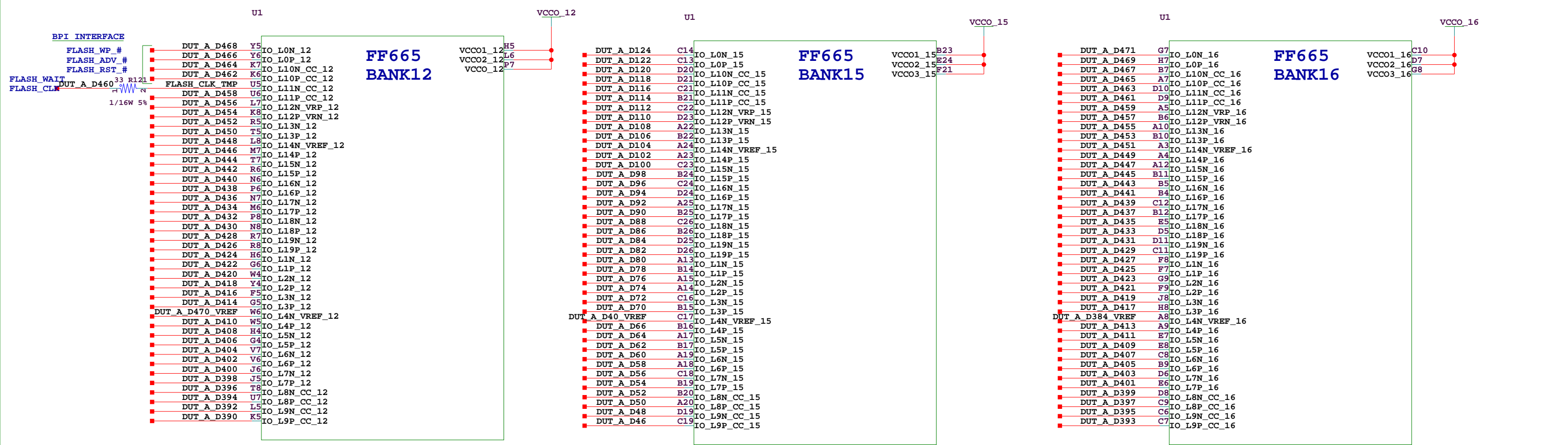
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404

SYSTEM MONITOR

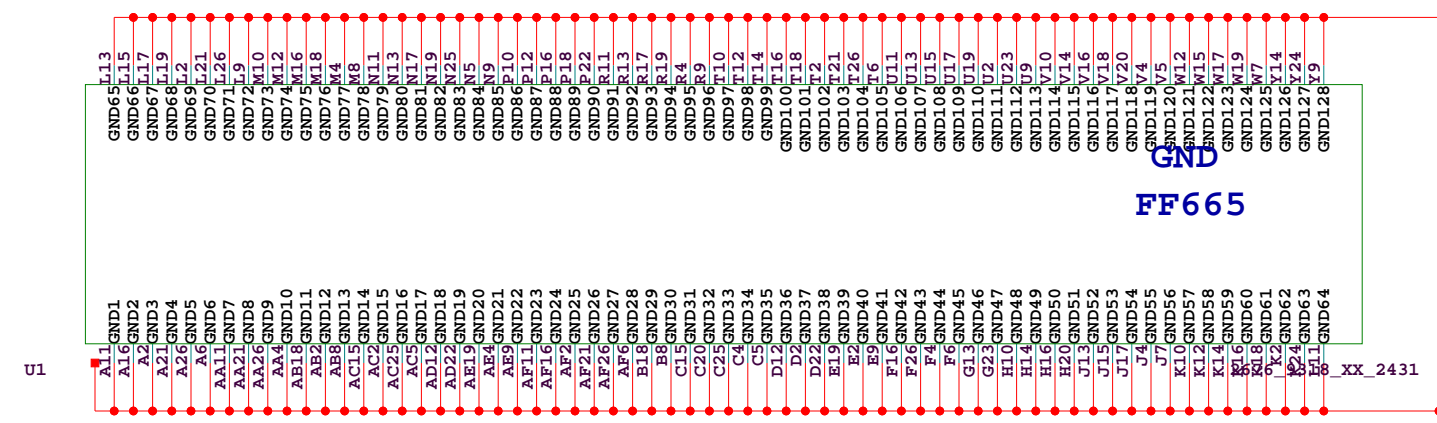
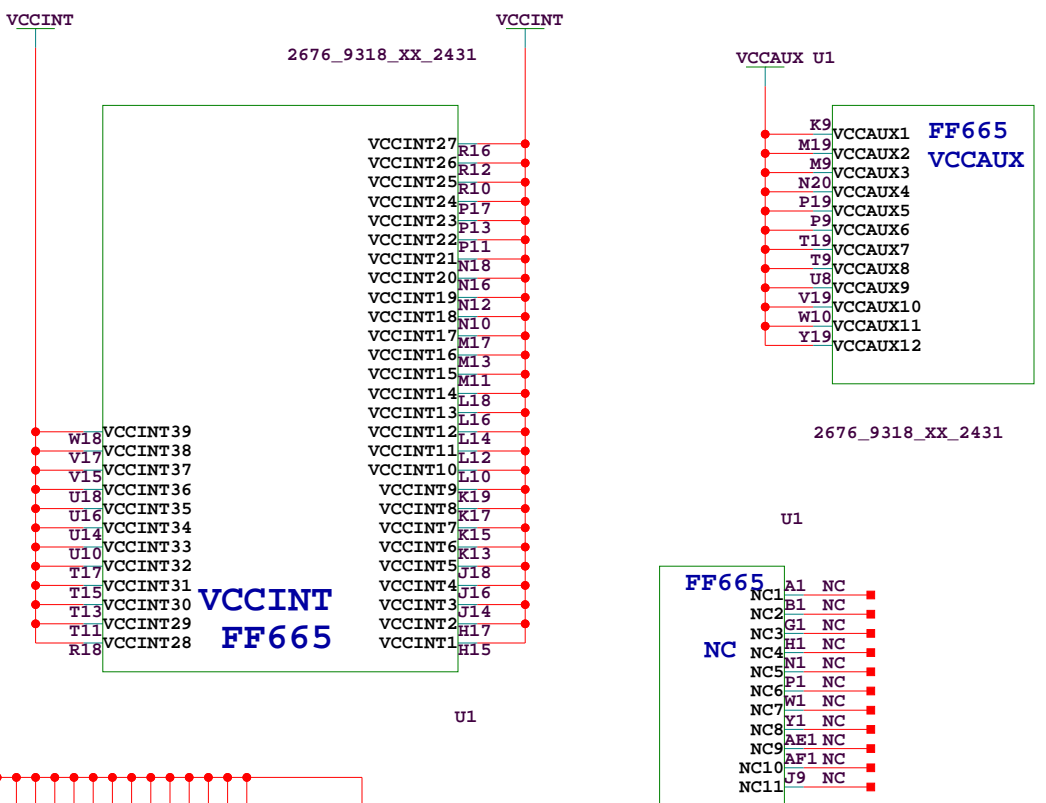
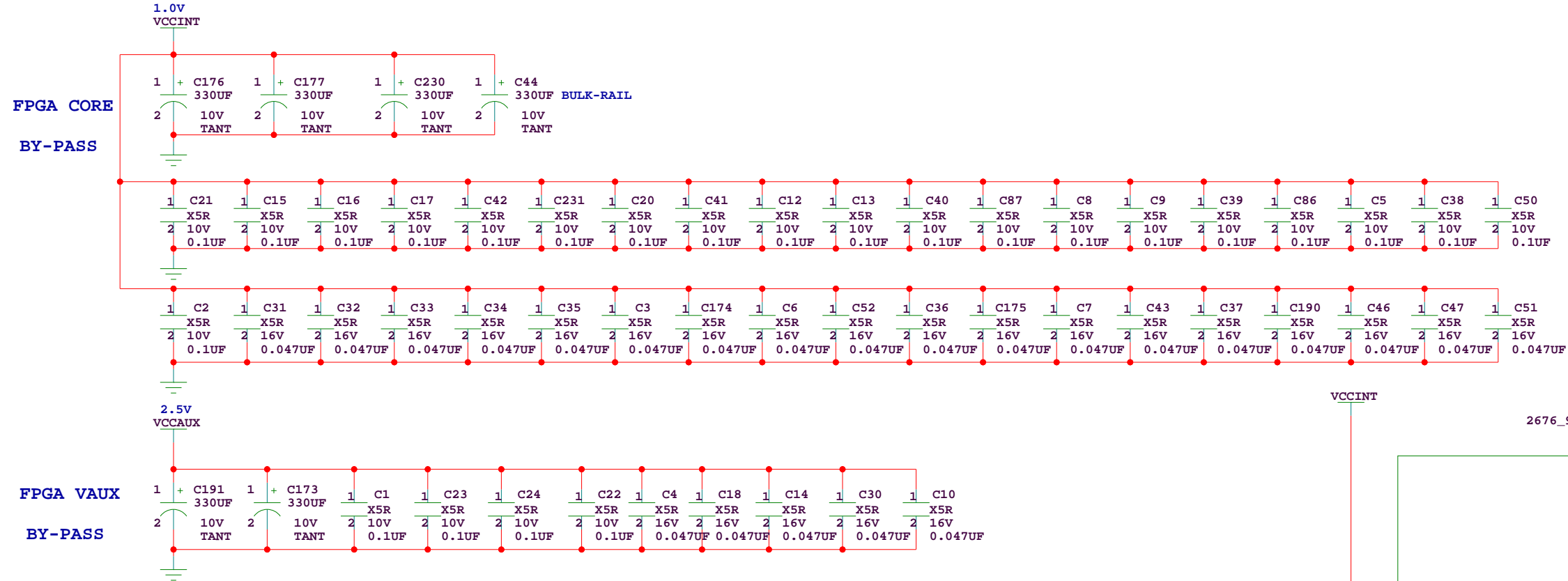
Date: 2-19-2008_12:14	Ver: C
Sheet Size: B	Rev: 02
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		SCH P/N	0381233
		ART P/N	0531592
		FAB P/N	1280404
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404 MGT LOOPBACK 112,114,116,118			
Date: 2-19-2008_12:14		Ver: C	
Sheet Size: B		Rev: 02	
Sheet 7	of 21	Drawn By s.s.	



		SCH P/N	0381233
		ART P/N	0531592
		FAB P/N	1280404
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404			
Date: 2-19-2008_12:14		Ver: C	
Sheet Size: B		Rev: 02	
Sheet 8 of 21		Drawn By s.s.	

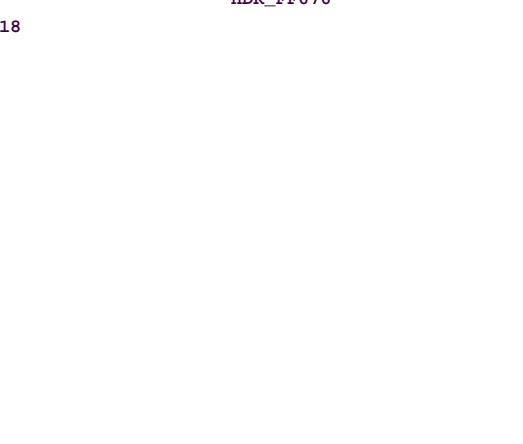
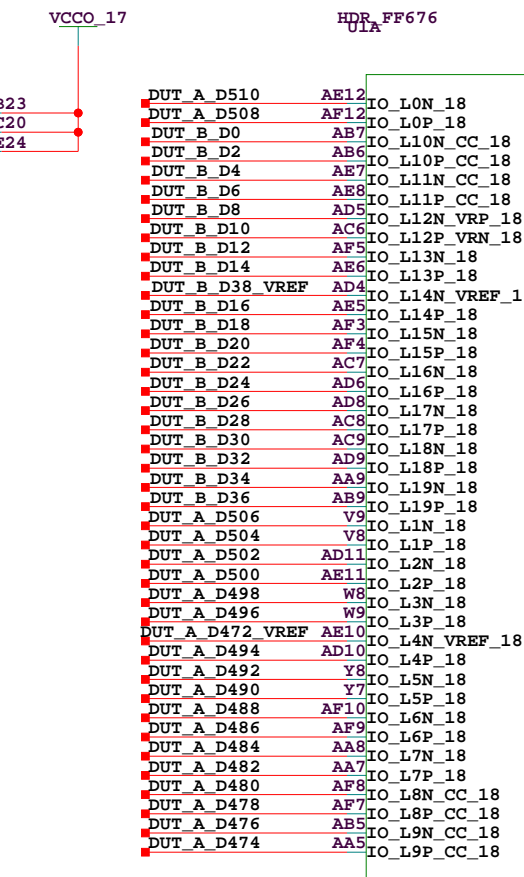
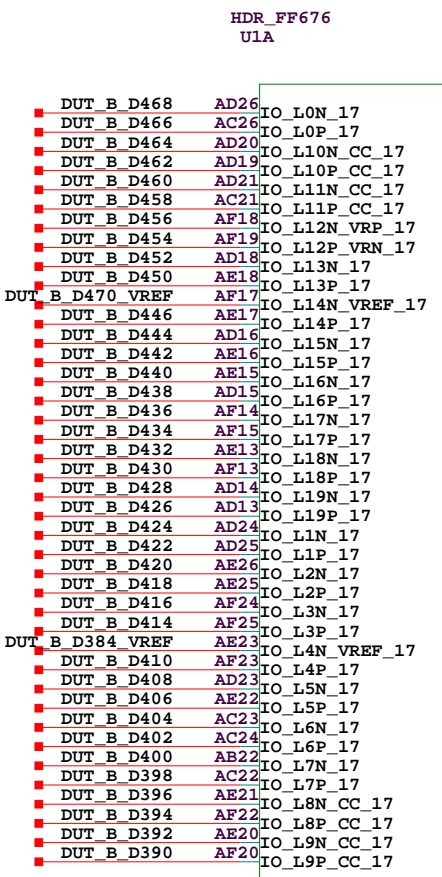
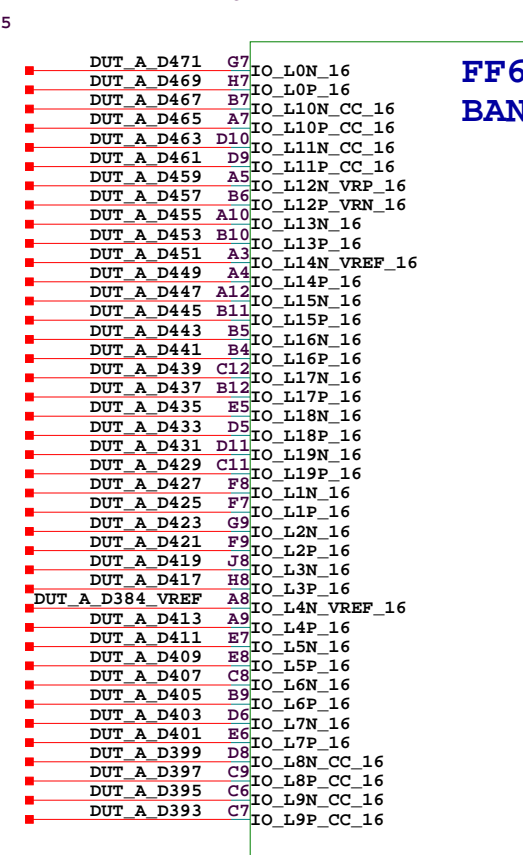
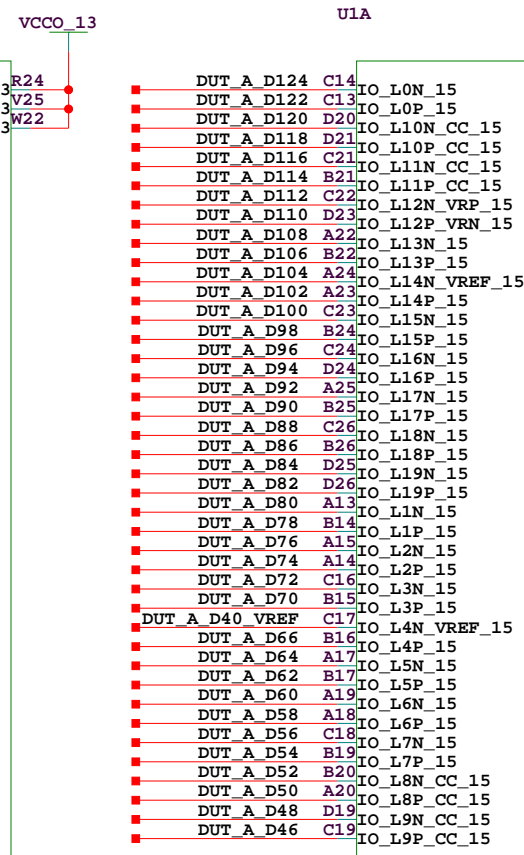
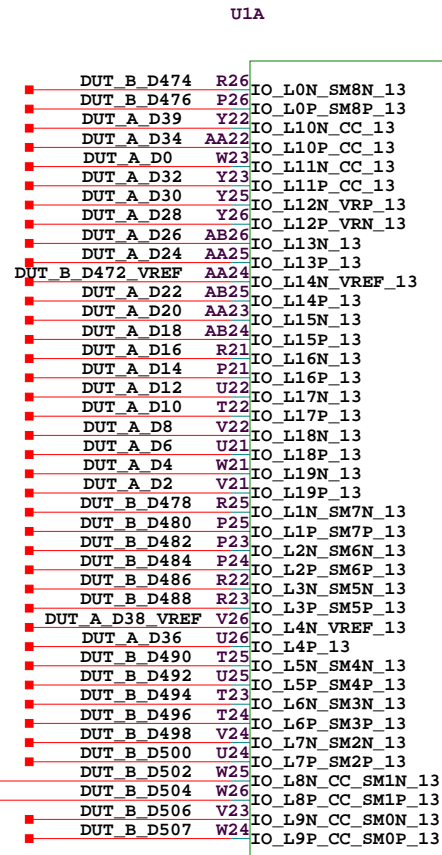


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SCH P/N 0381233
ART P/N 0531592
FAB P/N 1280404

Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404
FPGA DECOUPLING CAPACITORS

Date: 2-19-2008_12:14 Ver: C
Sheet Size: B Rev: 02
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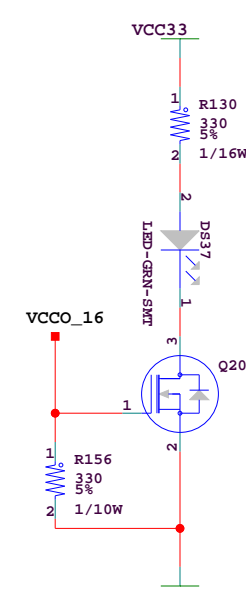
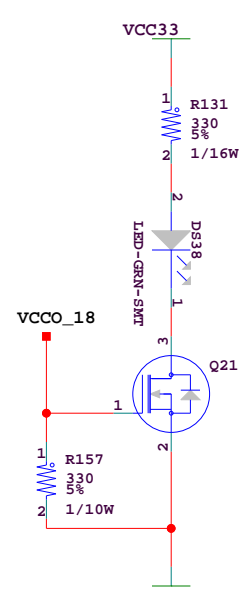
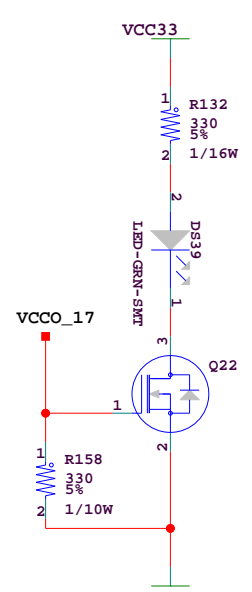
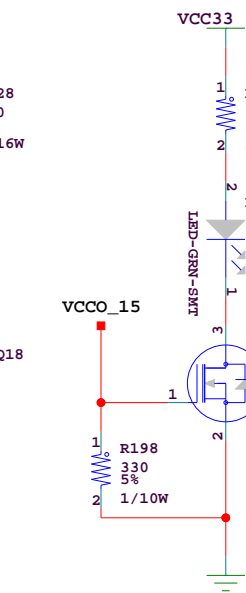
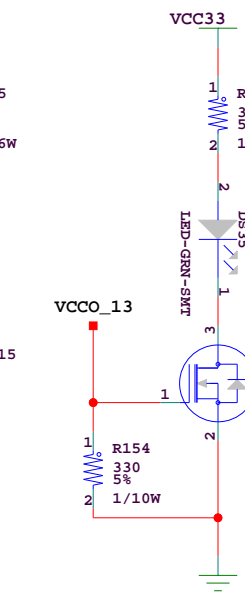
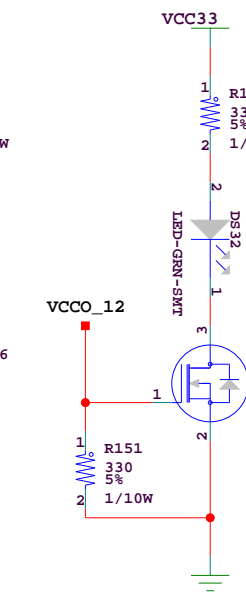
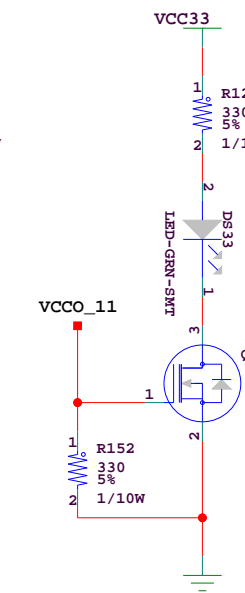
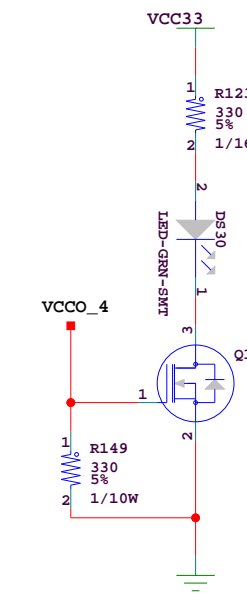
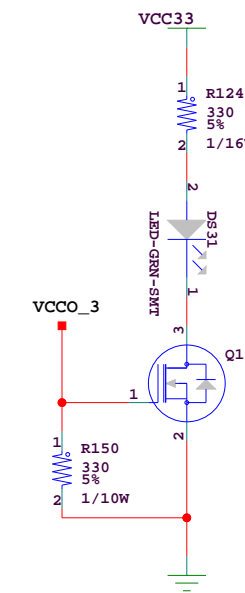
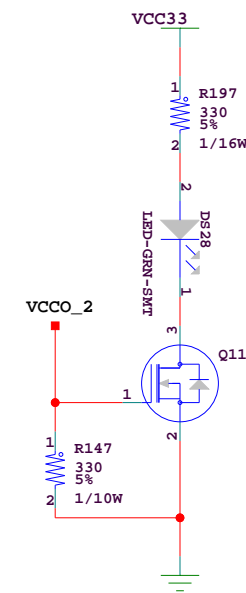
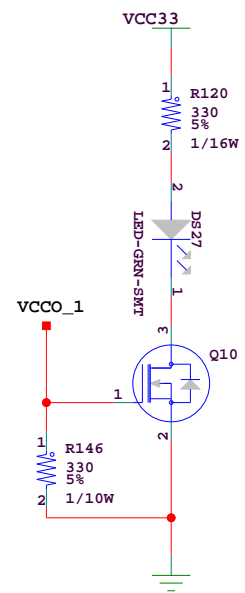
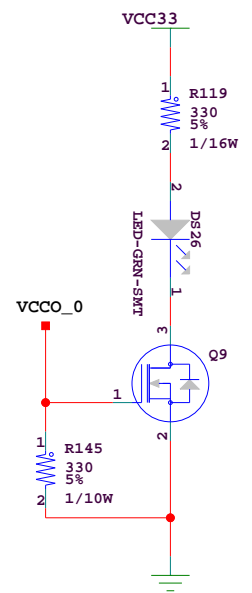
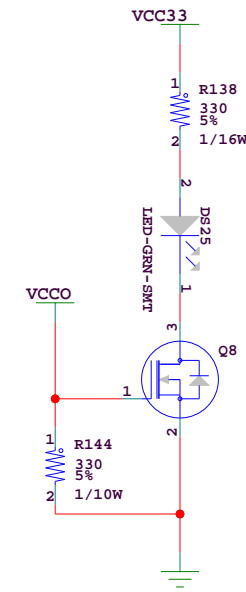
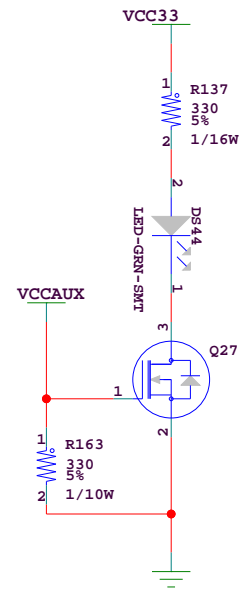
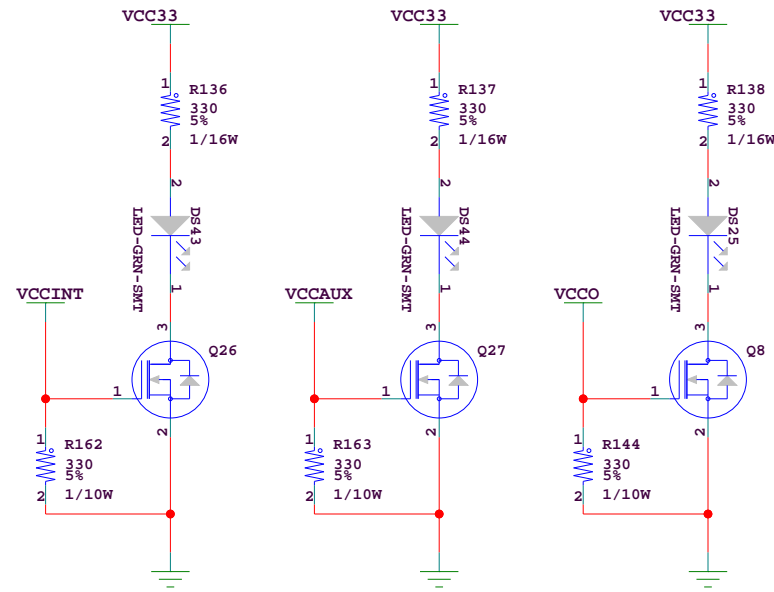
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SCH P/N 0381233
ART P/N 0531592
FAB P/N 1280404

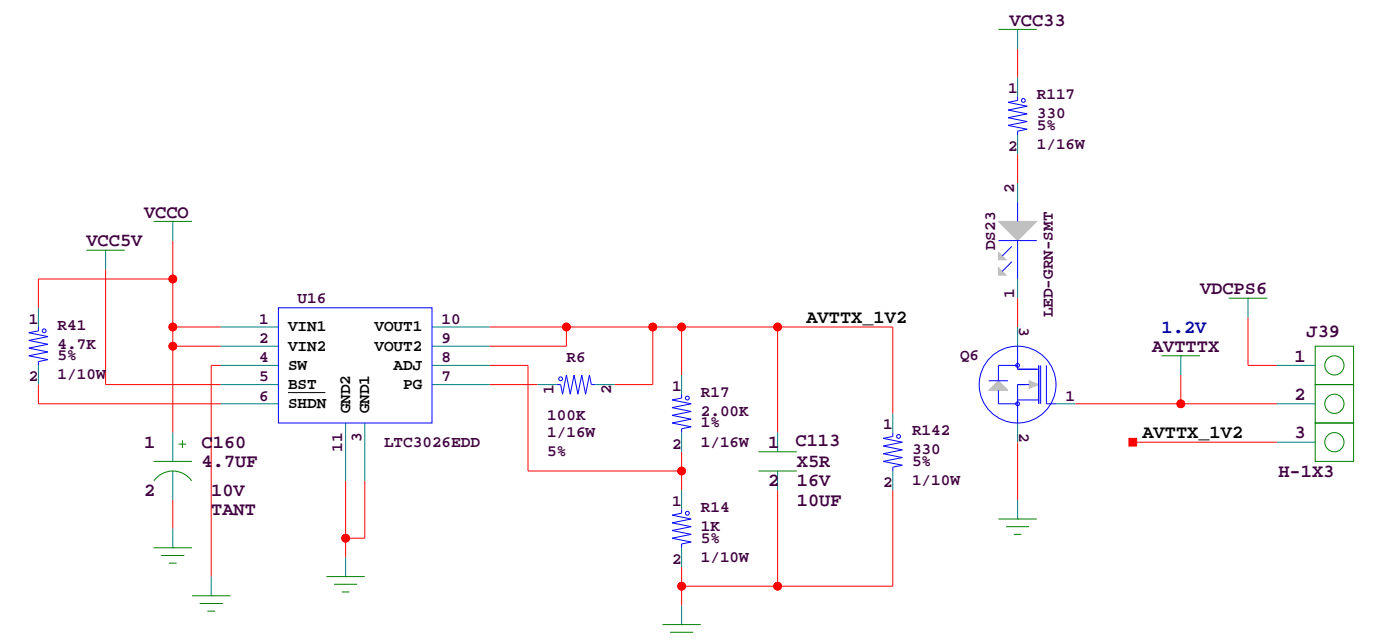
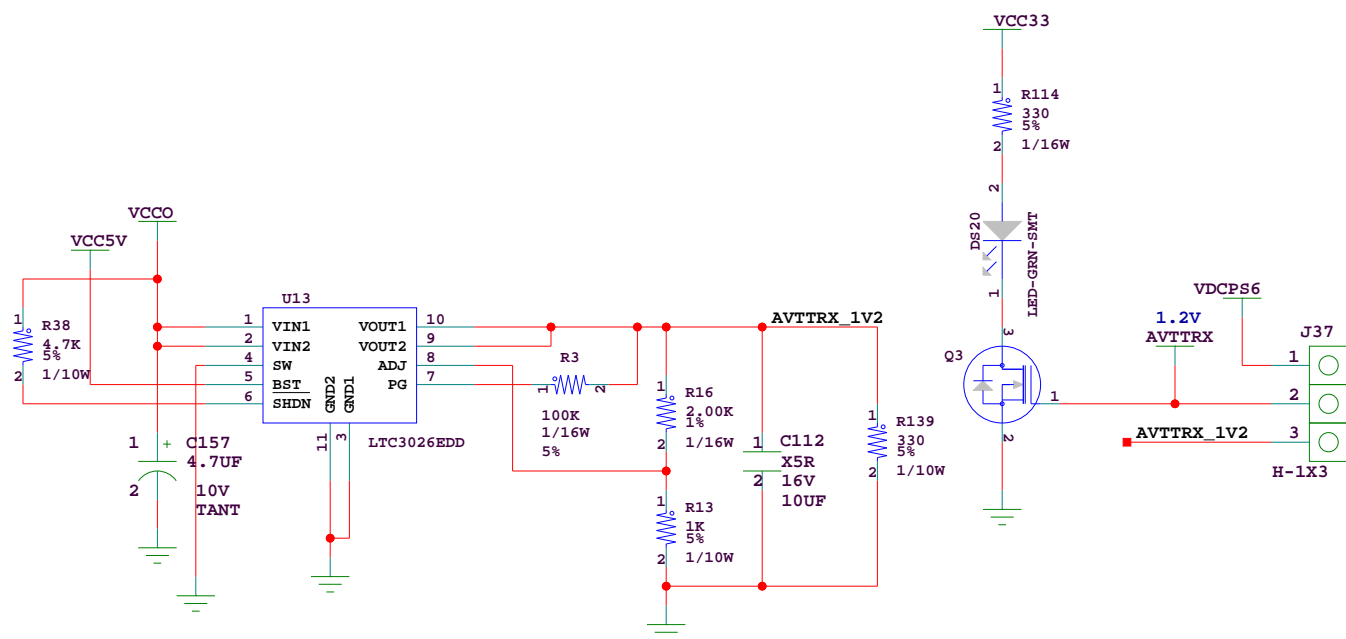
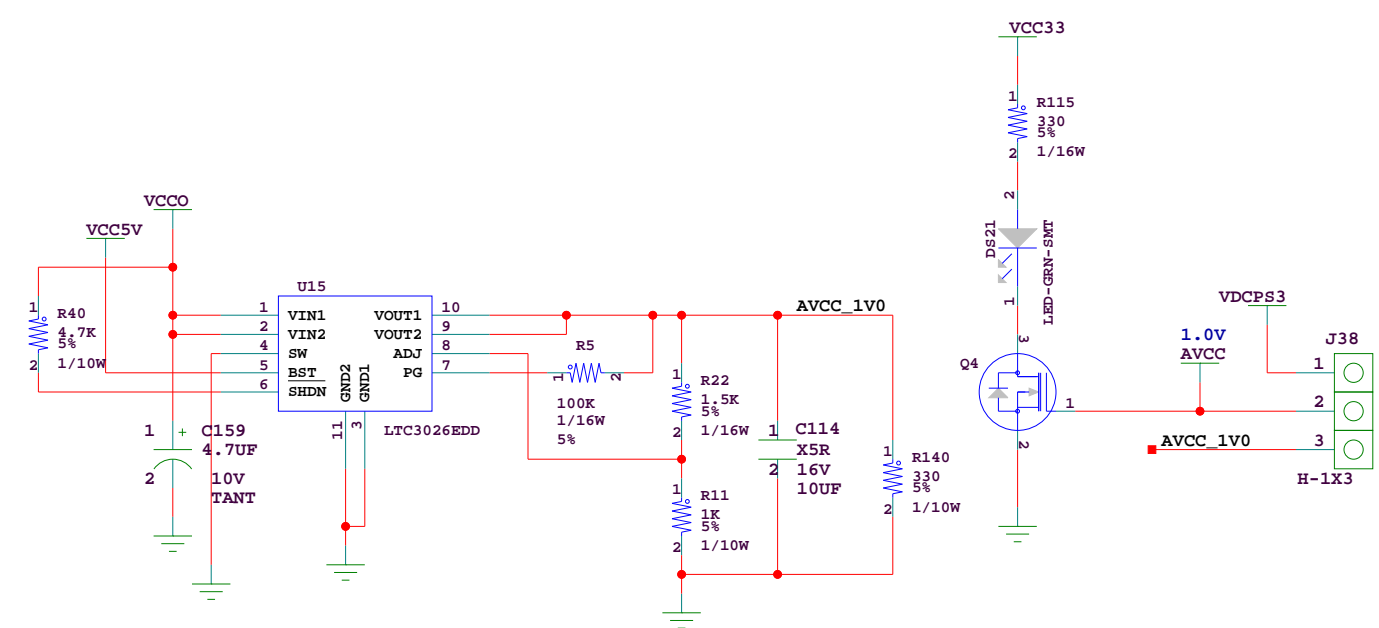
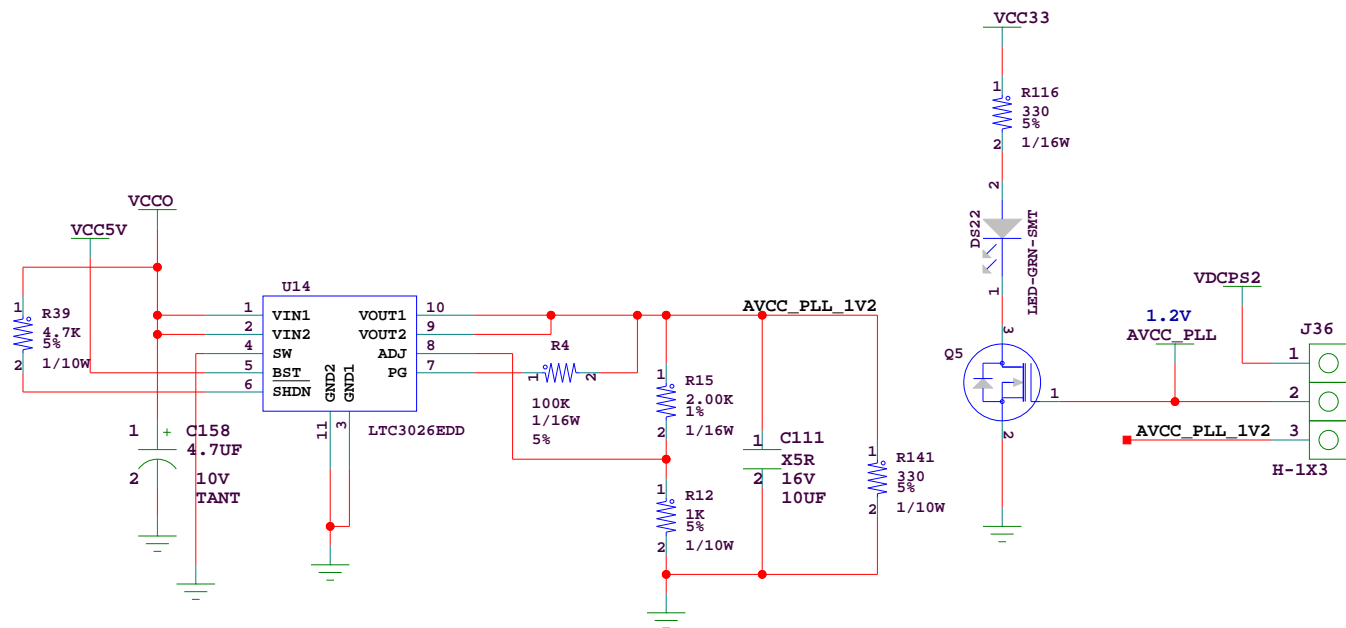
Title:
SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404


DUT TEST PINS

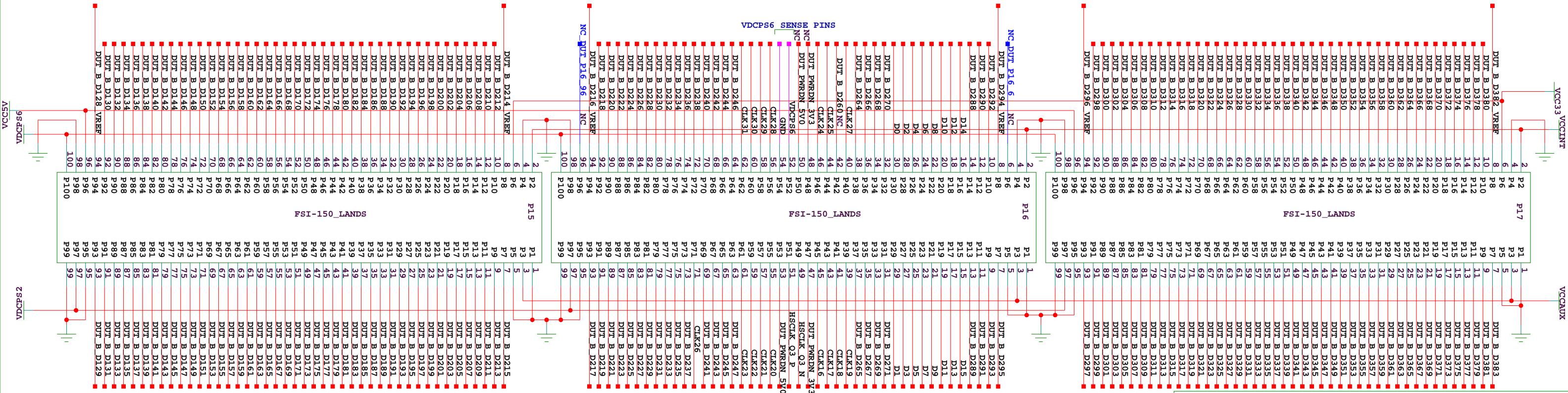
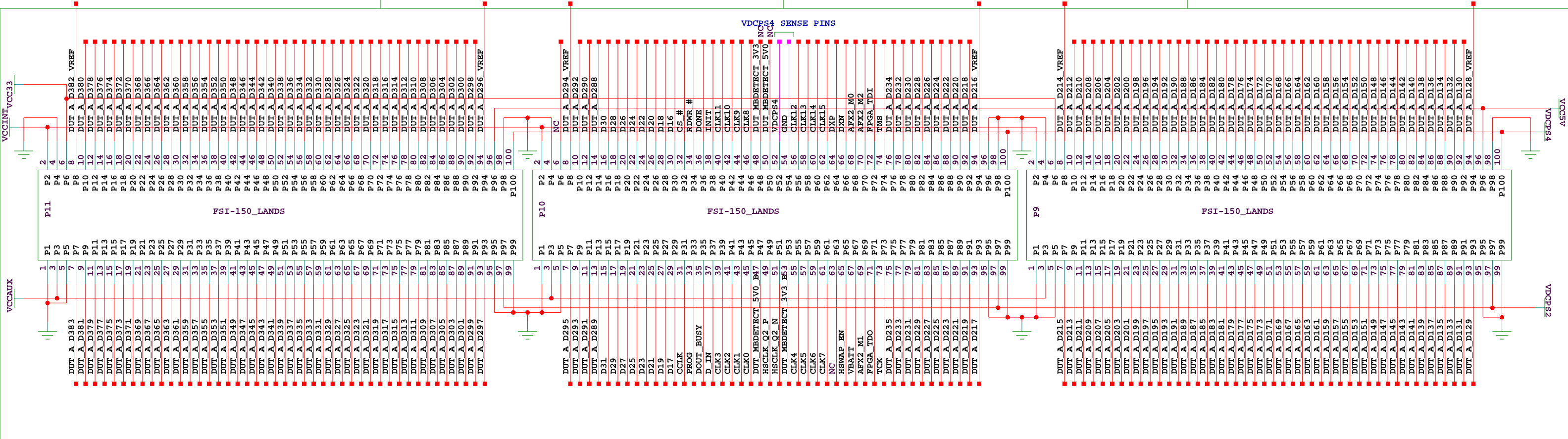
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Sheet Size: B Rev: 02
Sheet 11 of 21 Drawn By s.s.




		SCH P/N	0381233
		ART P/N	0531592
		FAB P/N	1280404
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404 POWER LED INDICATORS			
Date: 2-19-2008_12:13		Ver: C	
Sheet Size: B		Rev: 02	
Sheet 13	of 21	Drawn By s.s.	



		SCH P/N	0381233
		ART P/N	0531592
		FAB P/N	1280404
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404 MGT POWER SUPPLY			
Date: 2-19-2008_12:13		Ver: C	
Sheet Size: B		Rev: 02	
Sheet 14	of 21	Drawn By s.s.	

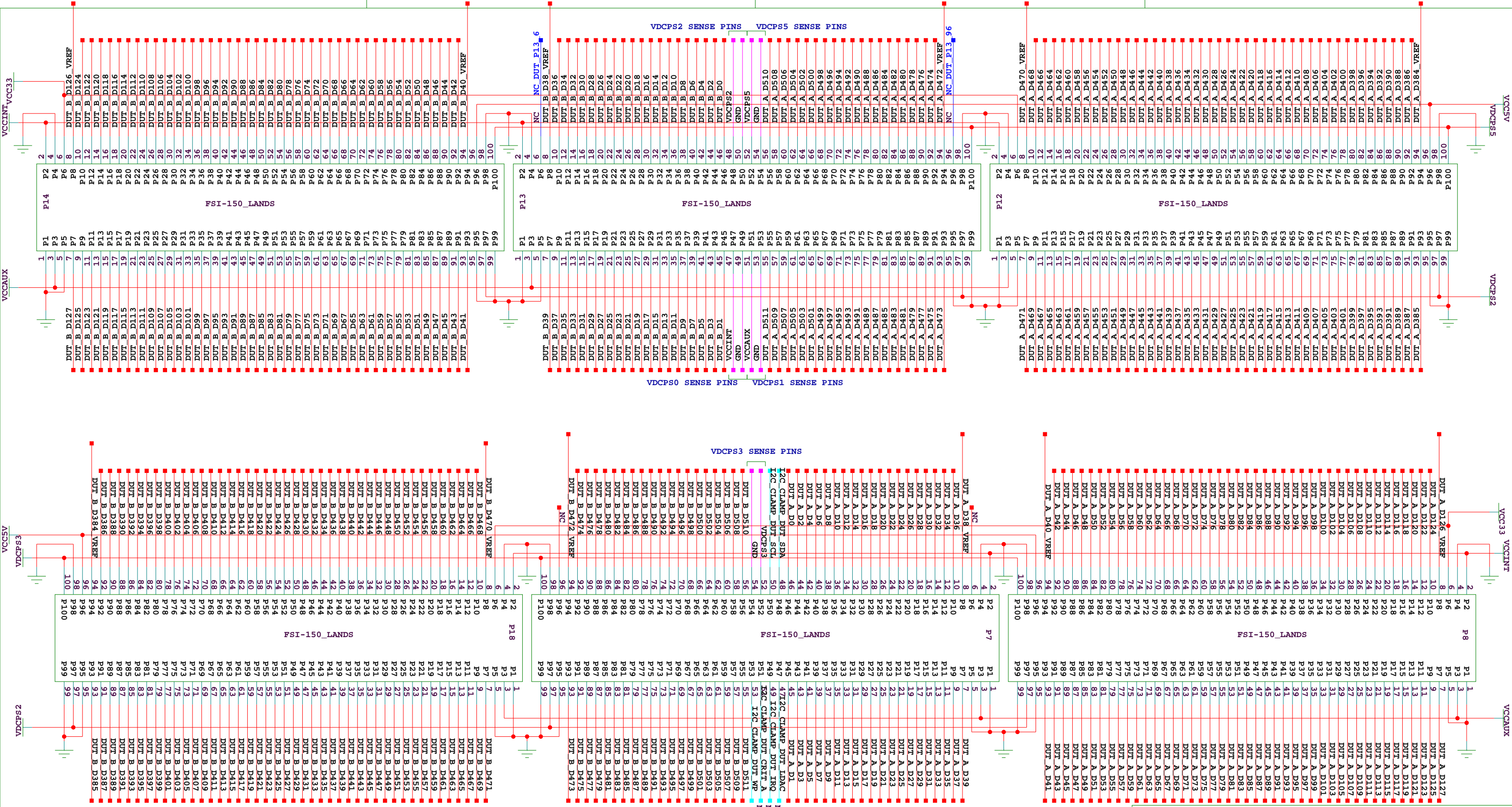





 SCH P/N 0381233
 ART P/N 0531592
 FAB P/N 1280404

Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404
AFX LANDINGS TOP AND BOTTOM

Date: 2-19-2008_12:13
Ver: C
Sheet Size: B
Rev: 02
Sheet 15 **of** 21
Drawn By s.s.





SCH P/N 0381233
ART P/N 0531592
FAB P/N 1280404

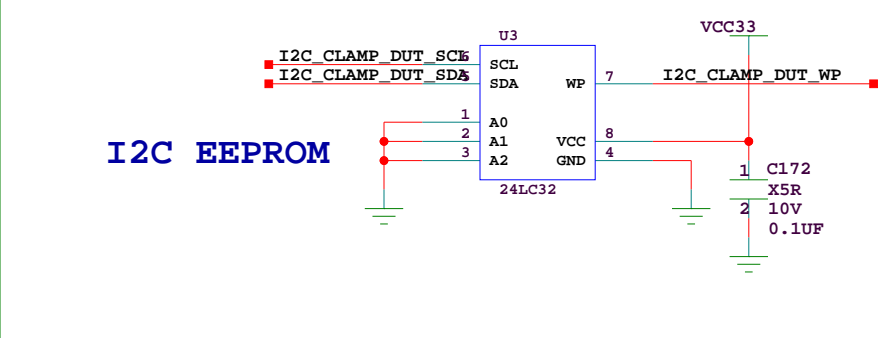
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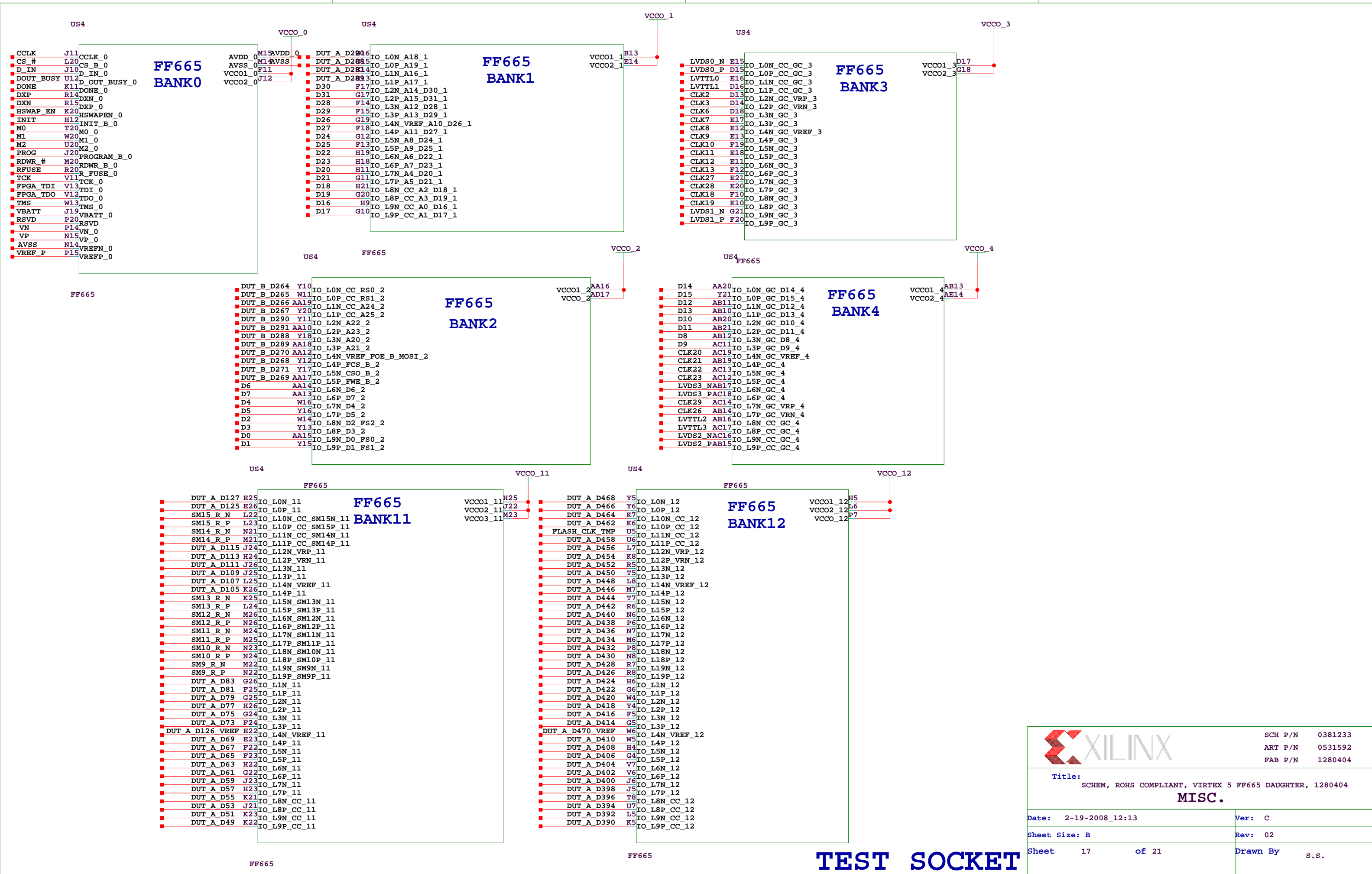
AFX LANDINGS LEFT AND RIGHT

Date: 2-19-2008_12:13 Ver: C

Sheet Size: B Rev: 02

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FF665 BANK0

FF665 BANK1

FF665 BANK3


FF665 BANK2

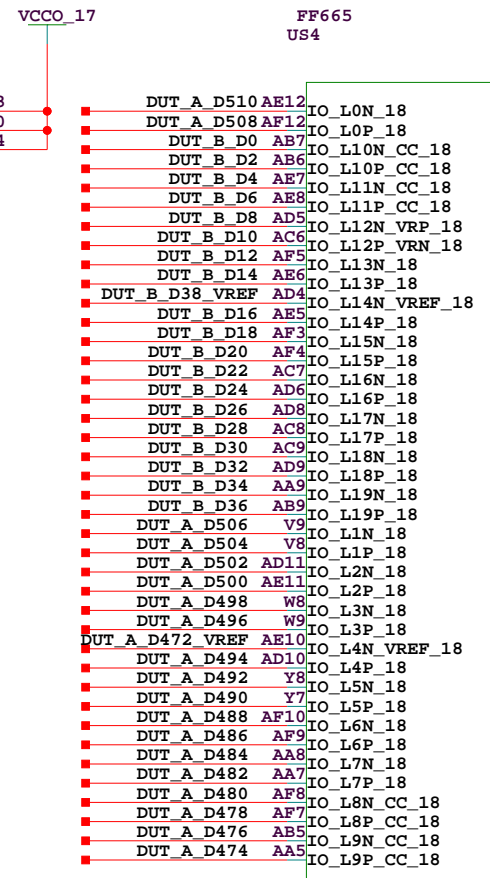
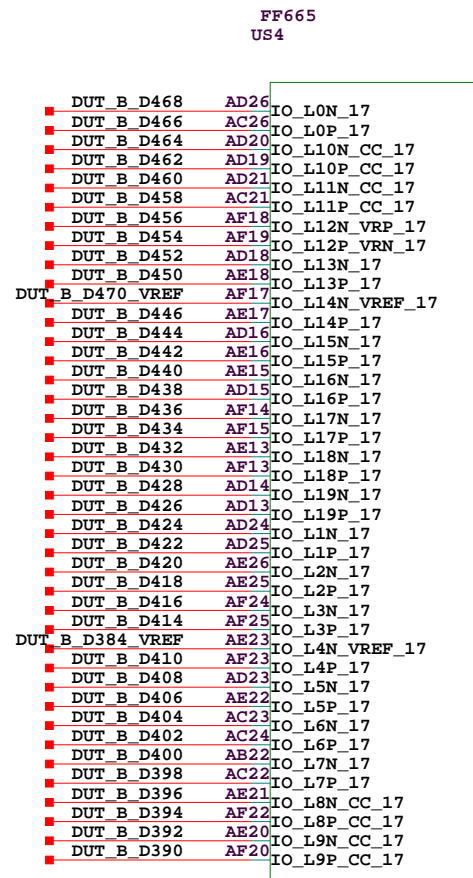
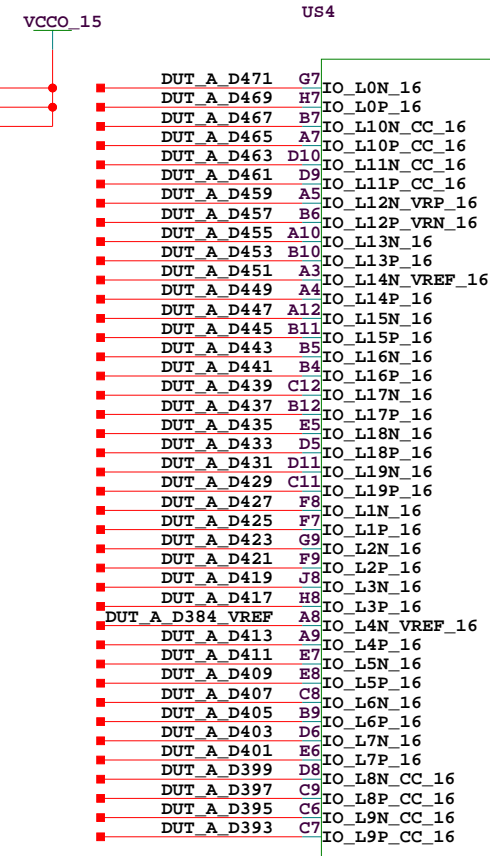
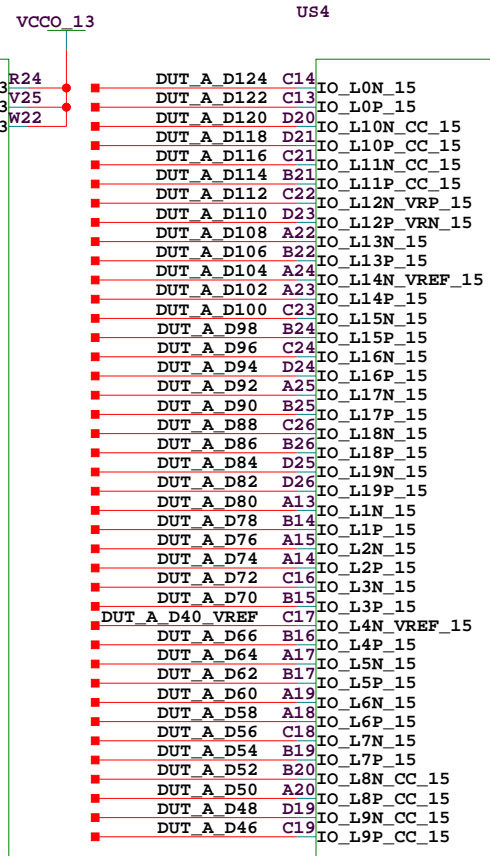
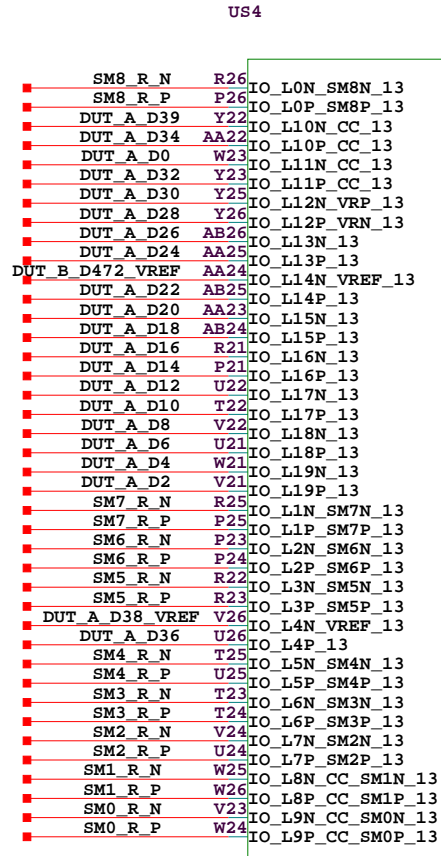
FF665 BANK4

FF665 BANK11


FF665 BANK12

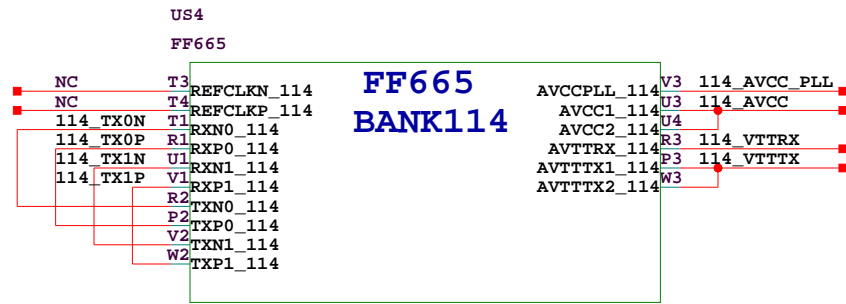
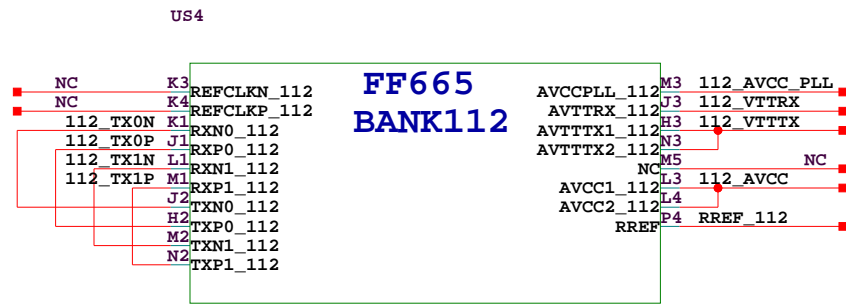
TEST SOCKET

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		ART P/N	0531592
		FAB P/N	1280404
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404 MISC.			
Date: 2-19-2008_12:13		Ver: C	
Sheet Size: B		Rev: 02	
Sheet 17	of 21	Drawn By s.s.	

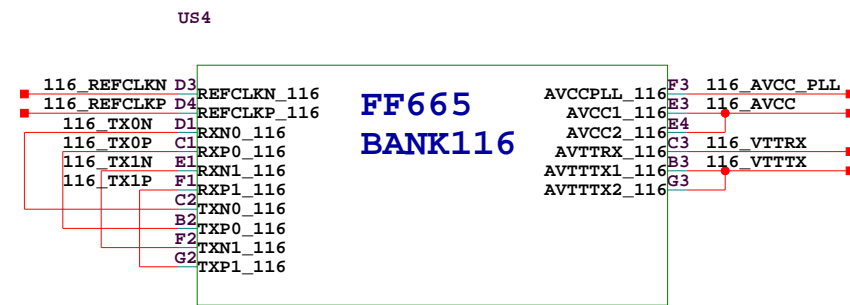


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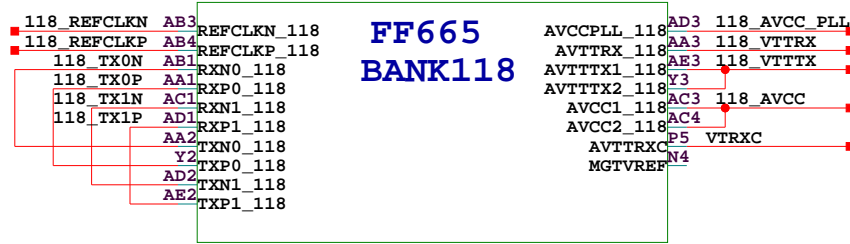
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		ART P/N	0531592
		FAB P/N	1280404
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404 MISC.			
Date: 2-19-2008_12:13		Ver: C	
Sheet Size: B		Rev: 02	
Sheet 18	of 21	Drawn By	s.s.



FF665




FF665
US4



FF665

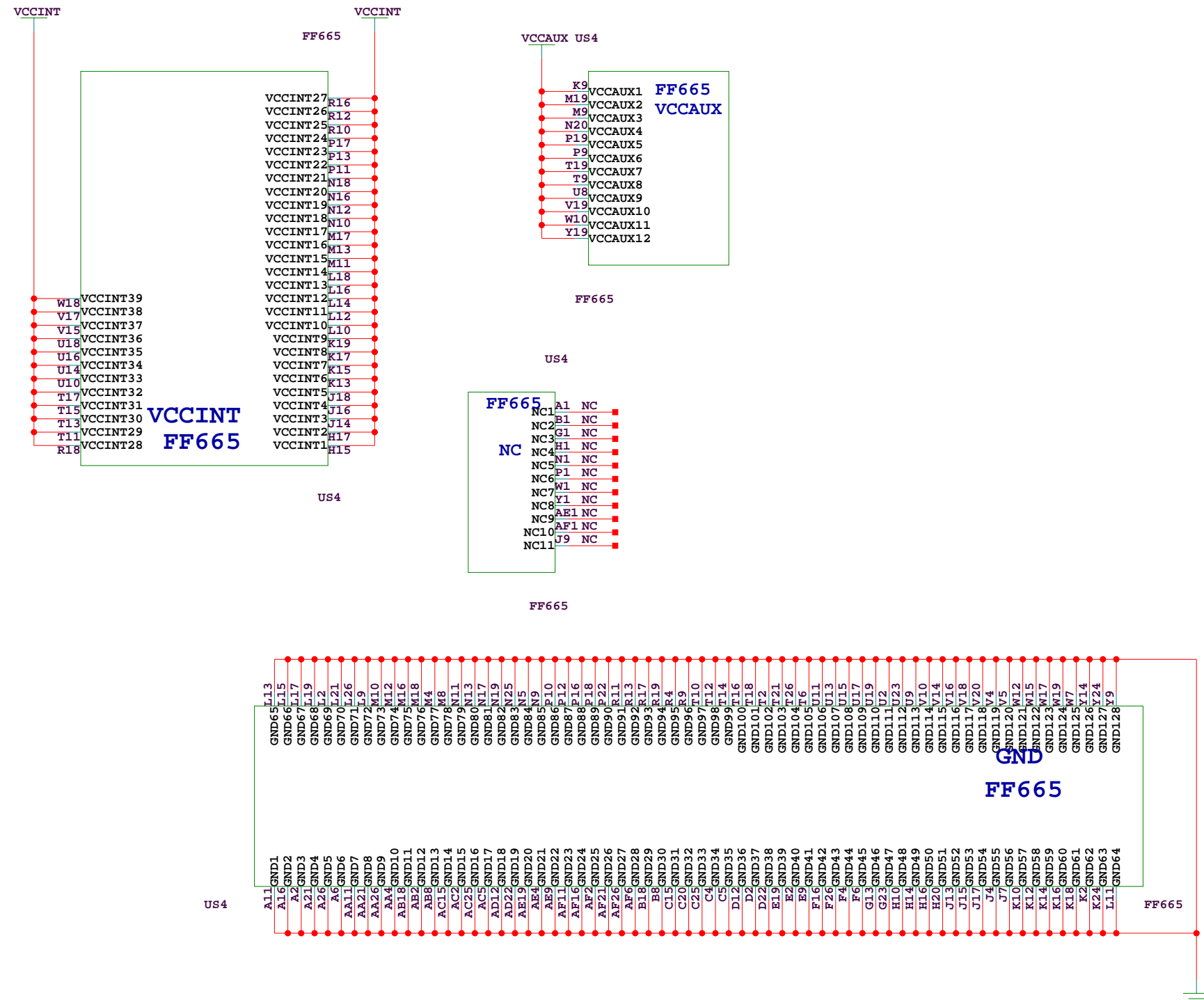
TEST SOCKET




SCH P/N 0381233
 ART P/N 0531592
 FAB P/N 1280404

Title:
 SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404
MISC.

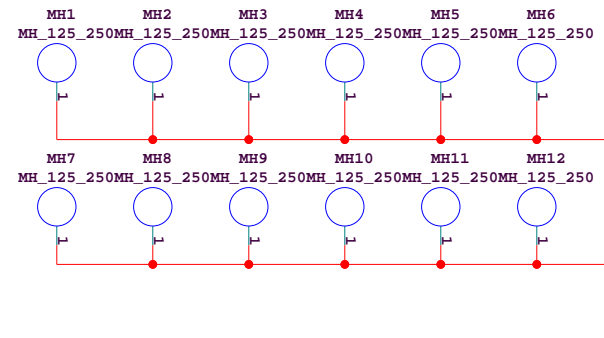
Date: 2-19-2008_12:13	Ver: C
Sheet Size: B	Rev: 02
Sheet 19 of 21	Drawn By s.s.



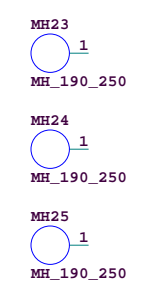
TEST SOCKET

		SCH P/N	0381233
		ART P/N	0531592
		FAB P/N	1280404
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404 MISC.			
Date: 2-19-2008_12:13		Ver: C	
Sheet Size: B		Rev: 02	
Sheet 20	of 21	Drawn By	s.s.

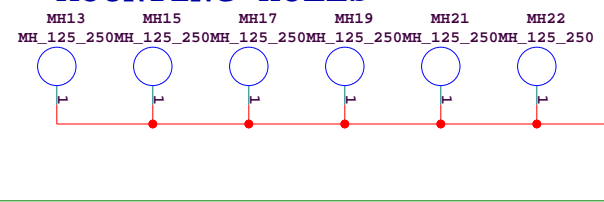
AFXII MOUNTING HOLES



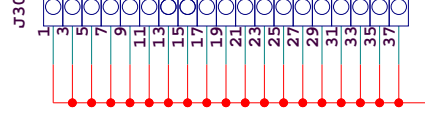
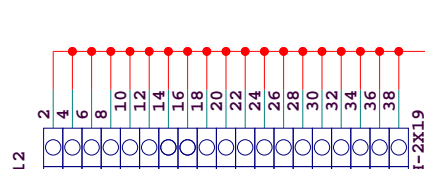
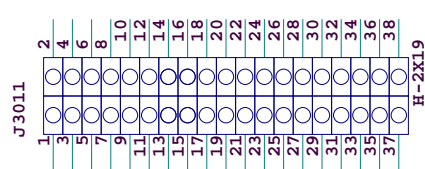
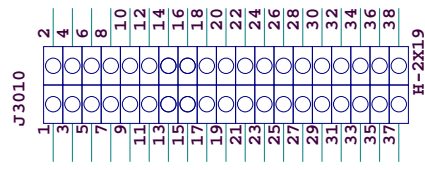
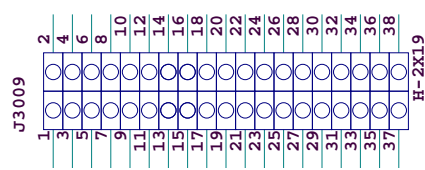
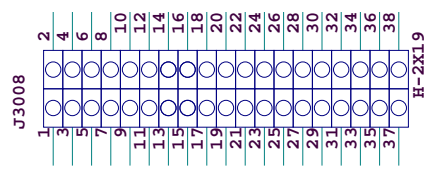
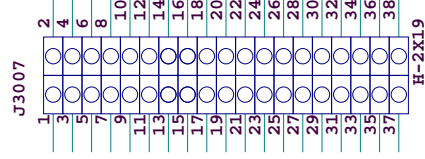
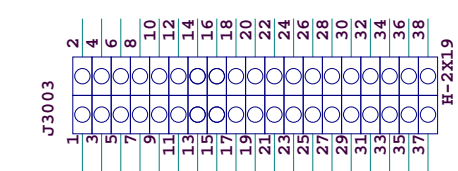
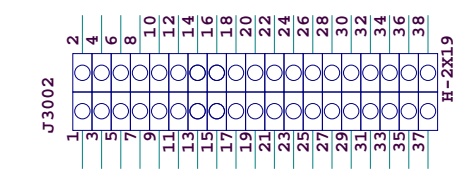
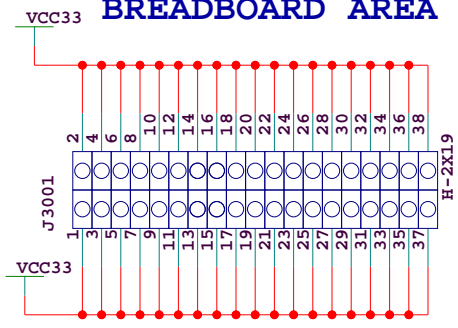
AFXII GUIDE HOLES



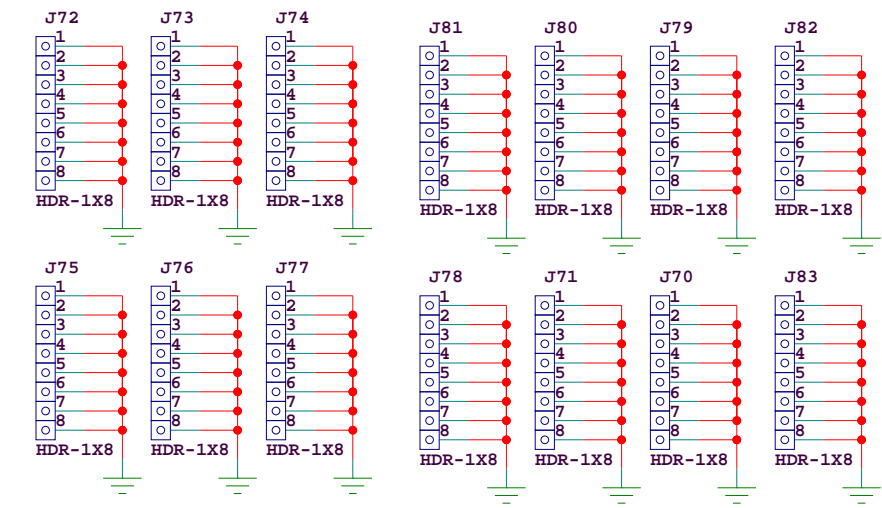
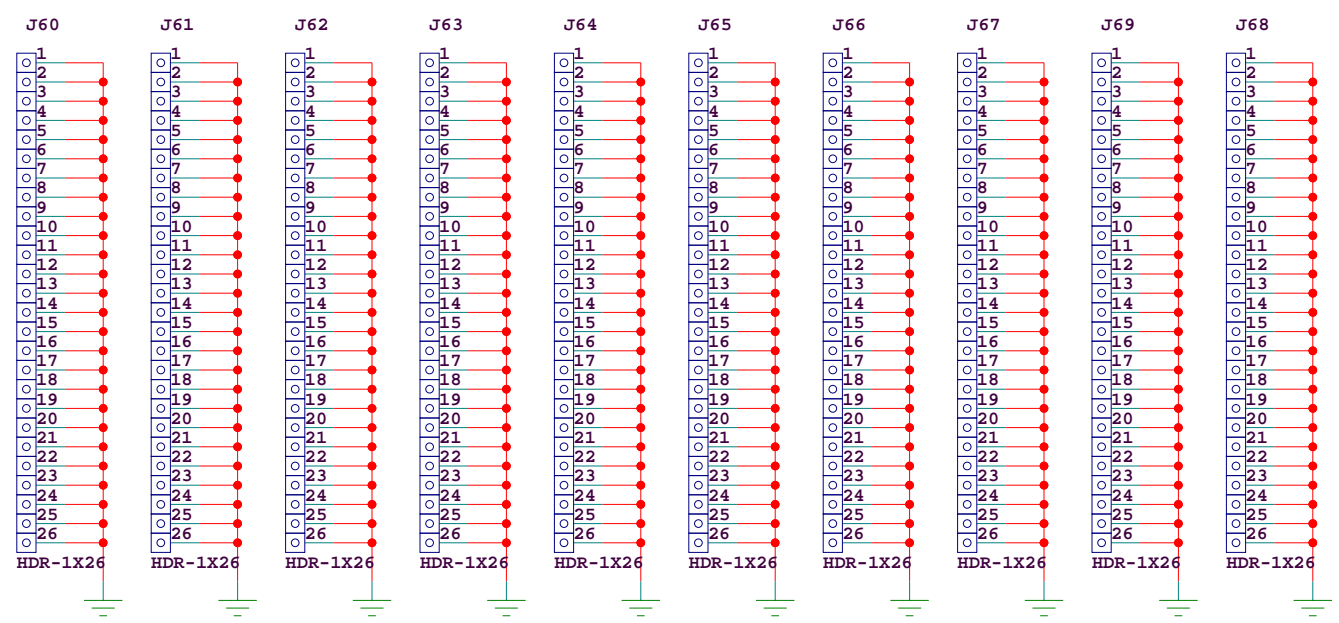
MOUNTING HOLES



BREADBOARD AREA



DUT INTERLEAVE GND'S



SCH P/N 0381233
 ART P/N 0531592
 FAB P/N 1280404

Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404
HARDWARE AND BREADBOARD AREA

Date: 2-19-2008_12:13	Ver: C
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