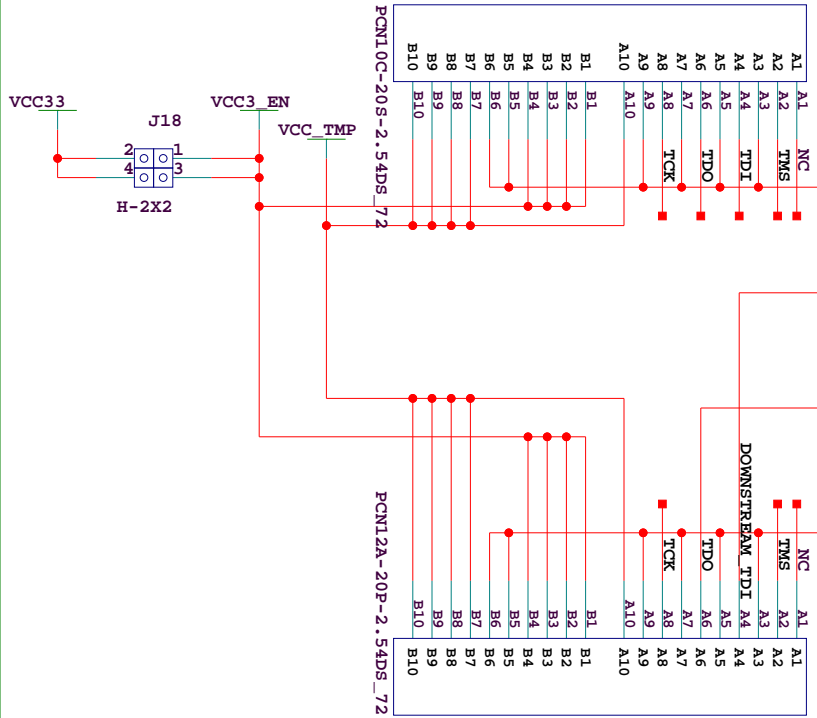
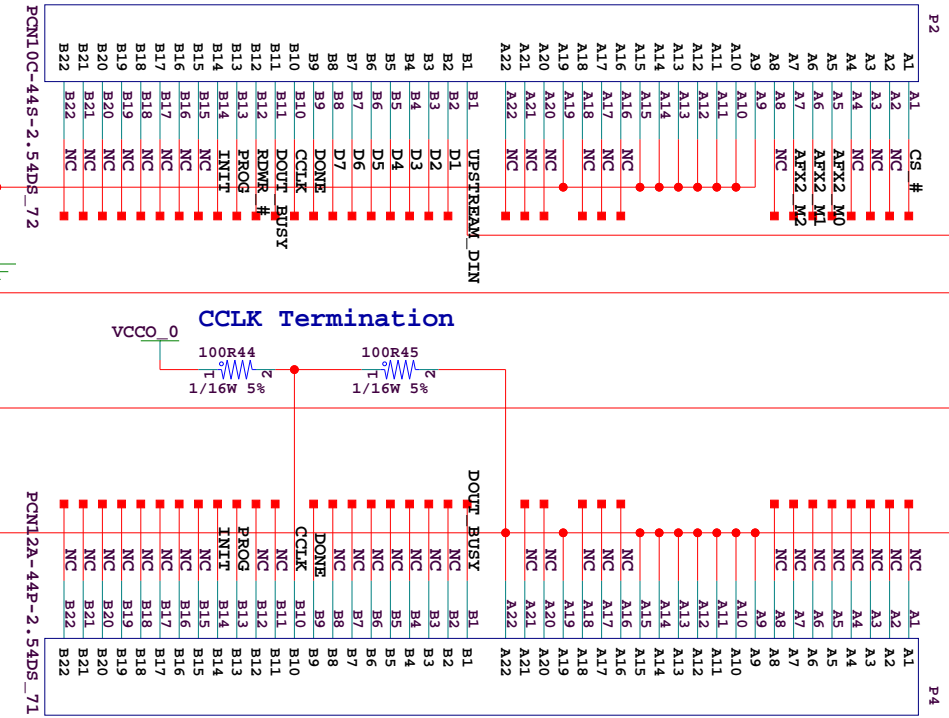


		SCH P/N	0381233
		ART P/N	0531592
		FAB P/N	1280404
<b>Title:</b> SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404			
<b>BLOCK DIAGRAM</b>			
<b>Date:</b> 9-26-2006_10:34		<b>Ver:</b> C	
<b>Sheet Size:</b> B		<b>Rev:</b> 02	
<b>Sheet</b> 1	<b>of</b> 21	<b>Drawn By</b> s.s.	

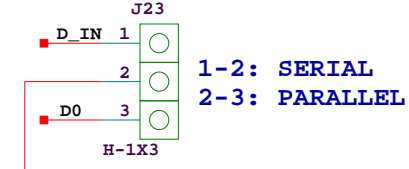
**SYSTEM ACE UPSTREAM**



**UPSTREAM CONNECTORS**

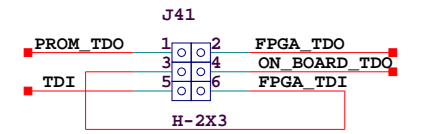


**DOWNSTREAM CONFIG**



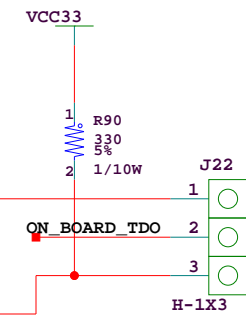
**ON BOARD JTAG CHAIN SELECTION**

PROM JTAG    FPGA JTAG  
 1-3: Enable    2-4: Enable  
 3-5: Disable    4-6: Disable

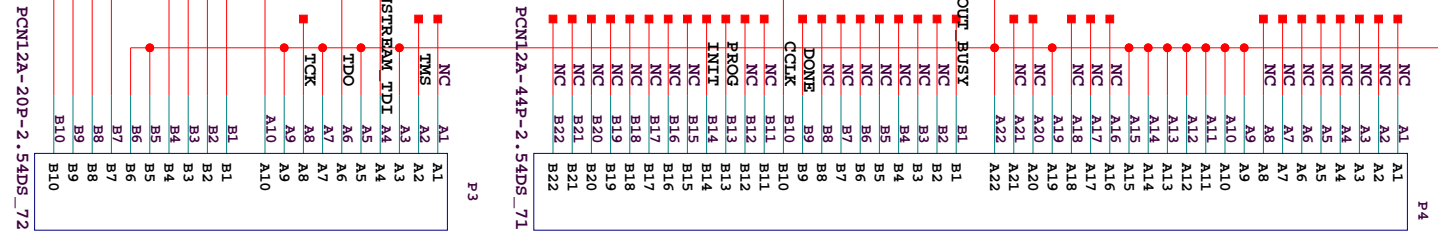


1-2: SERIAL CHAINING TO NEXT BOARD  
 2-3: TERMINATION OF LAST BOARD IN THE CHAIN

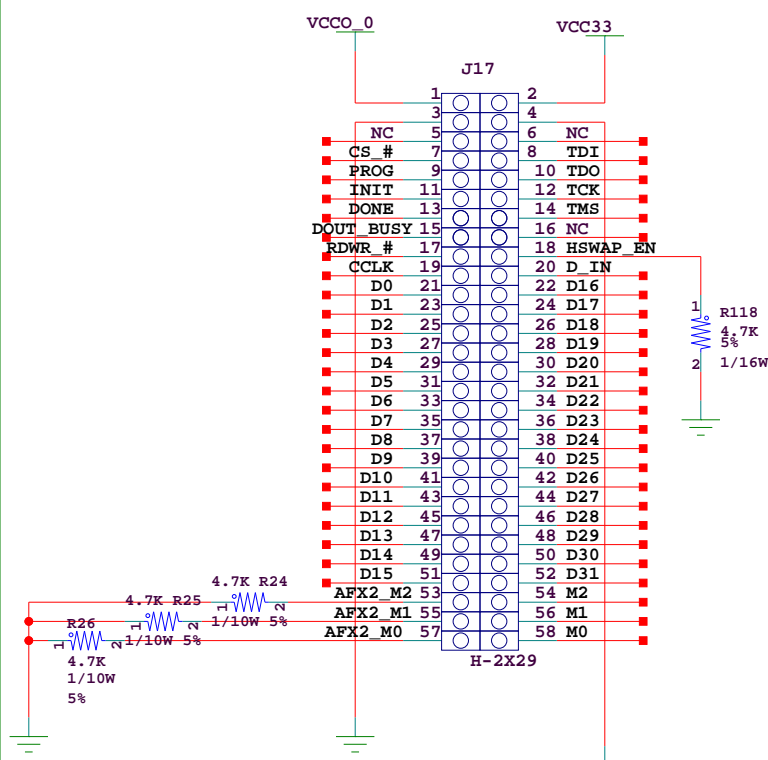
**JTAG JUMPER**



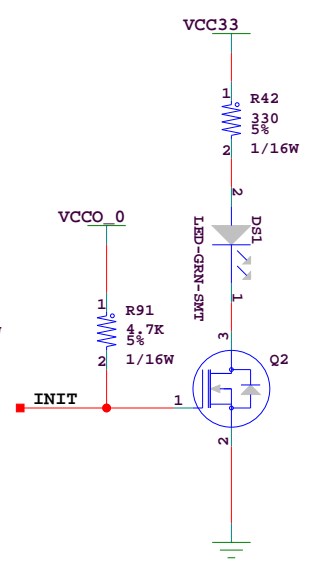
**SYSTEM ACE DOWNSTREAM DOWNSTREAM CONNECTORS**



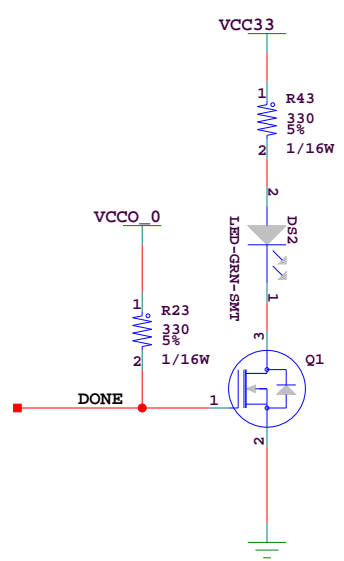
**FLYING WIRE CONFIGURATION PORT**



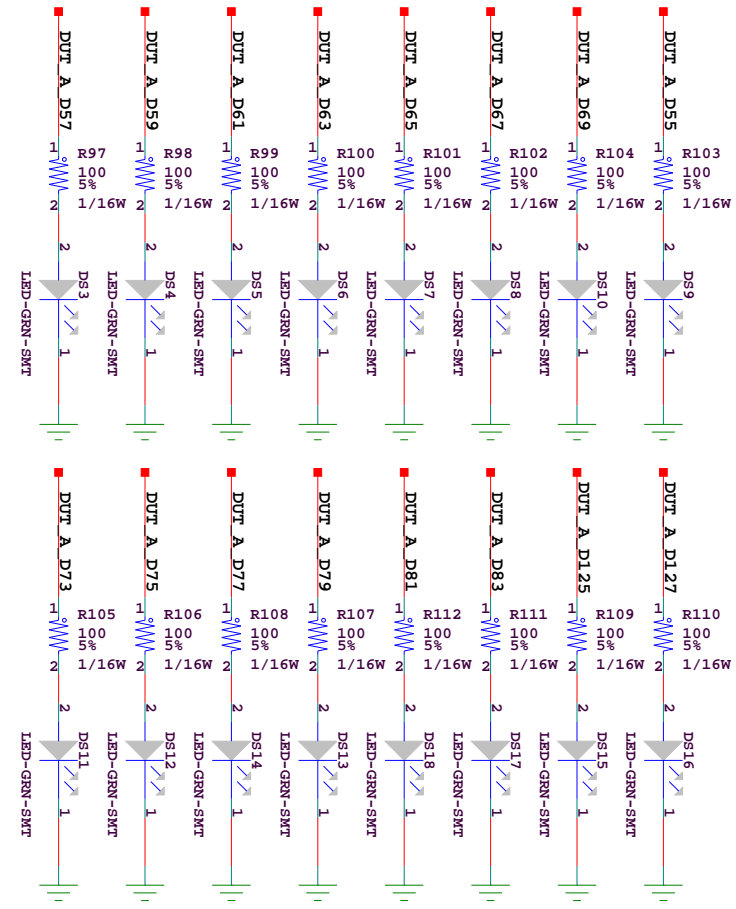
**INIT LED**



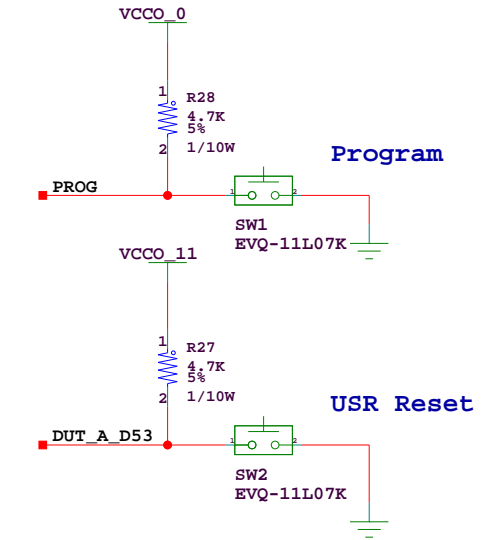
**DONE LED**



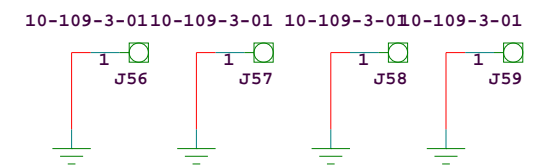
**USER LED'S**



**SWITCHES**

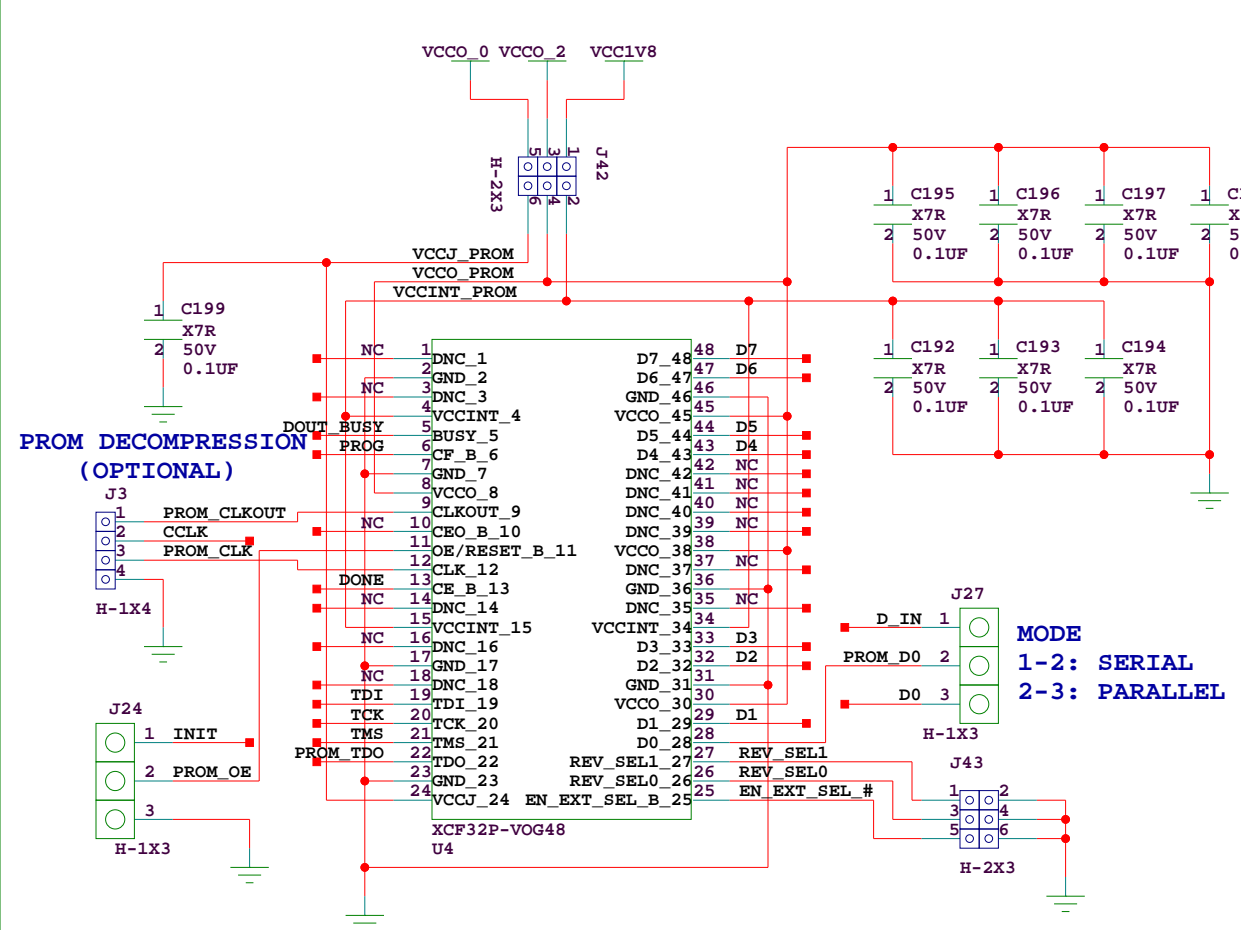


**TEST POINTS**

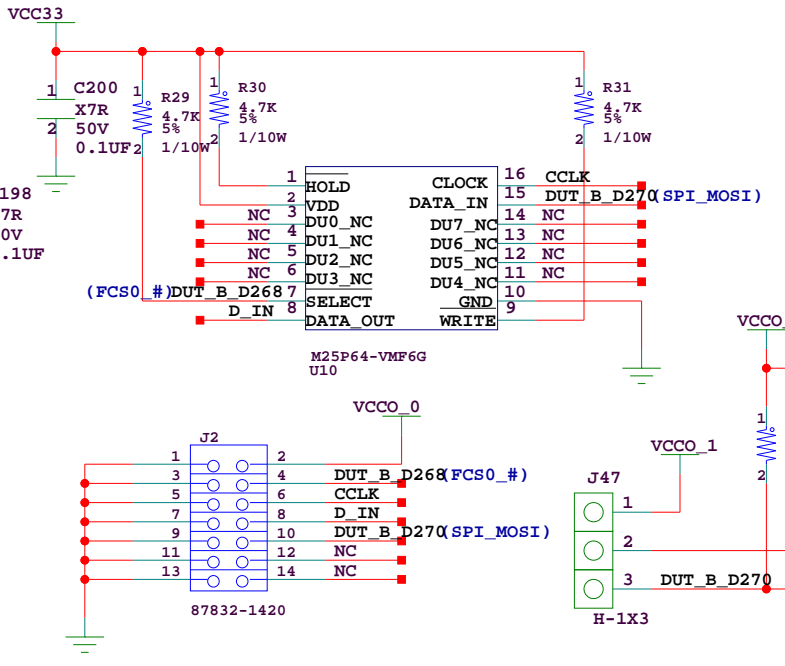


		SCH P/N	0381233
		ART P/N	0531592
		FAB P/N	1280404
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404 DIN CONN, PORTS, STATUS LEDS, SWITCHES			
Date:	2-19-2008_12:14	Ver:	C
Sheet Size:	B	Rev:	02
Sheet	2 of 21	Drawn By	s.s.

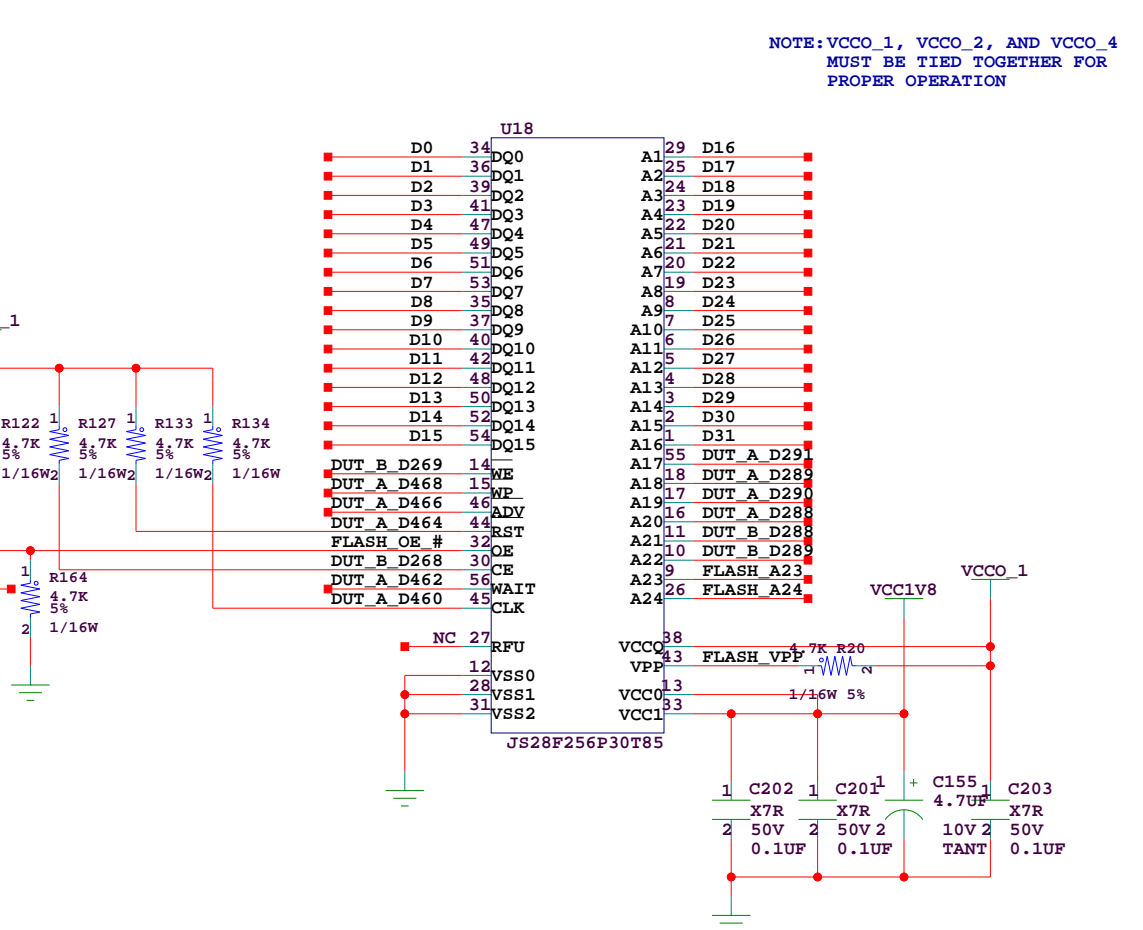
### CONFIGURATION PROM



### SPI INTERFACE



### BPI INTERFACE



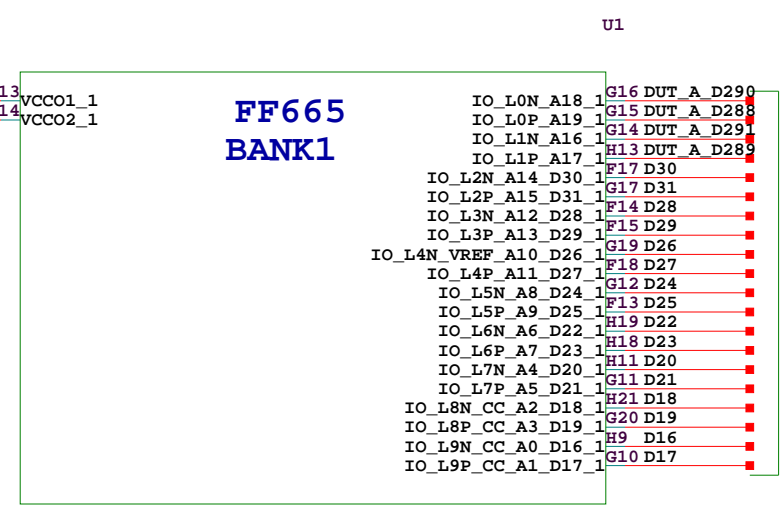
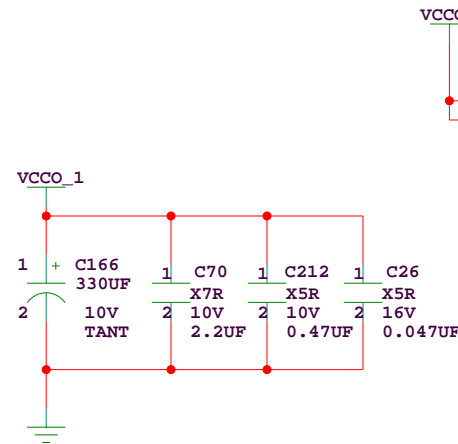
NOTE: VCCO\_1, VCCO\_2, AND VCCO\_4 MUST BE TIED TOGETHER FOR PROPER OPERATION

SCH P/N 0381233  
ART P/N 0531592  
FAB P/N 1280404

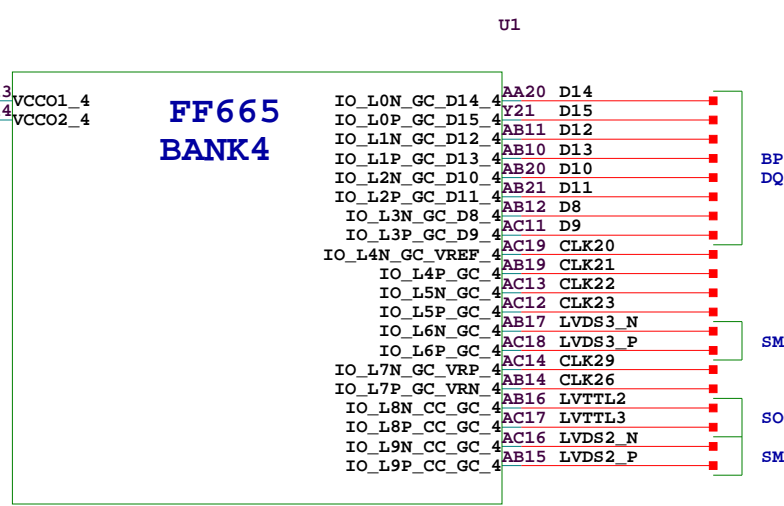
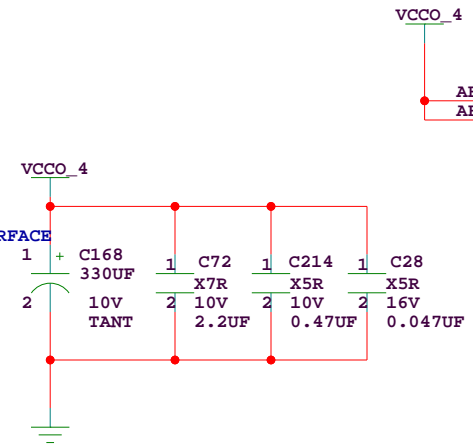
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404

## CONFIGURATION

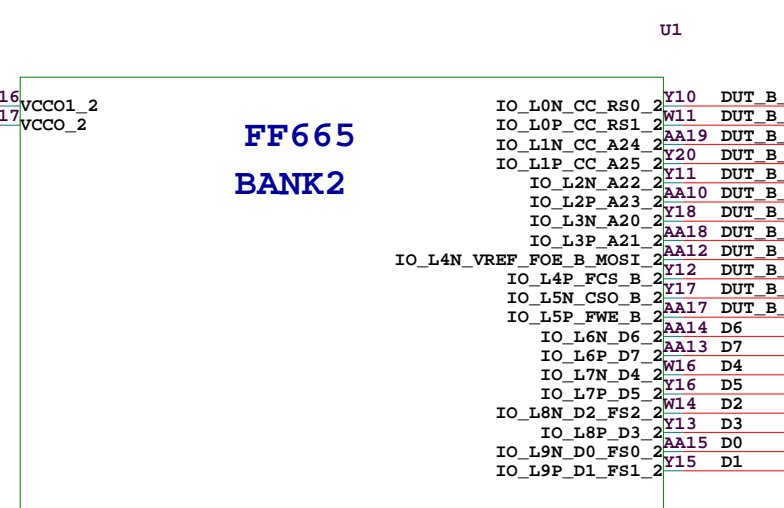
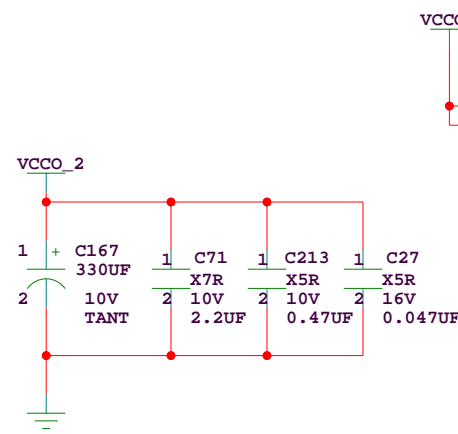
Date: 2-19-2008_12:14	Ver: C
Sheet Size: B	Rev: 02
Sheet 3 of 21	Drawn By s.s.



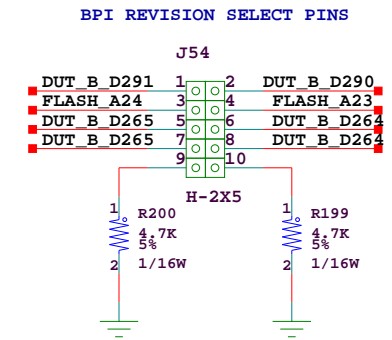
2676\_9318\_XX\_2431



2676\_9318\_XX\_2431



2676\_9318\_XX\_2431

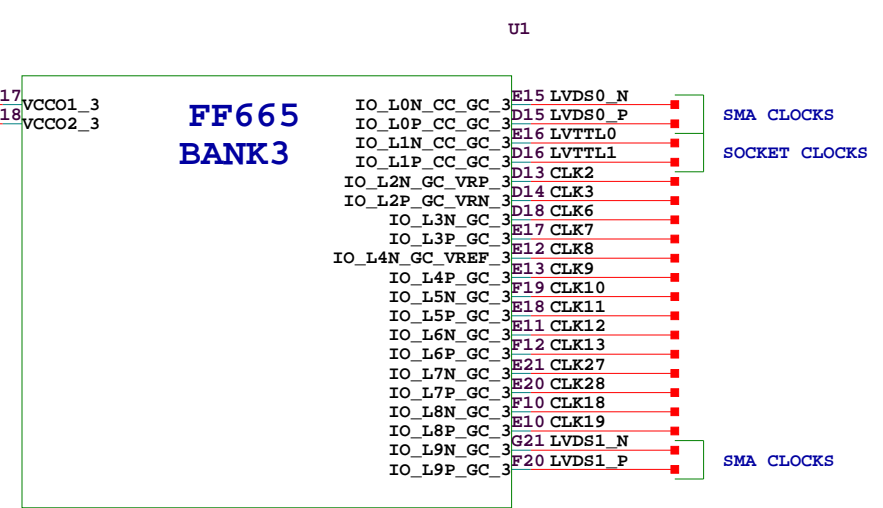
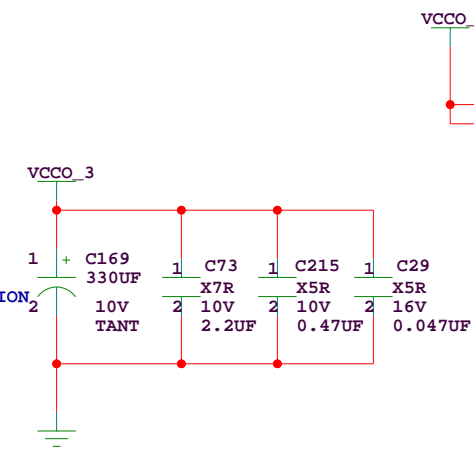
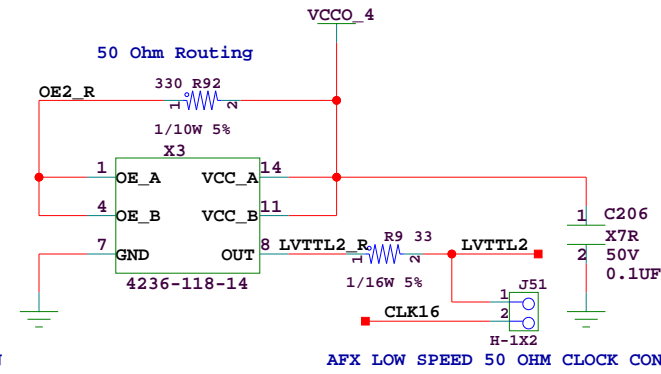
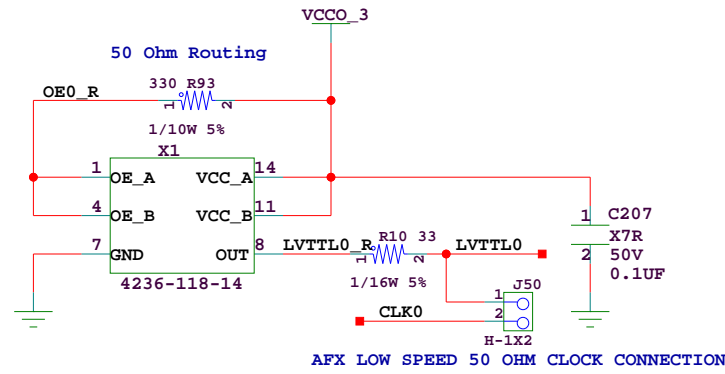


1-3: Selects ADDR23 from FPGA to FLASH ADDR24  
 3-5: Selects RS1 from FPGA to FLASH ADDR24  
 7-9: Pulldown for RS applications  
 2-4: Selects ADDR22 from FPGA to FLASH ADDR23  
 3-5: Selects RS0 from FPGA to FLASH ADDR23  
 8-10: Pulldown for RS applications

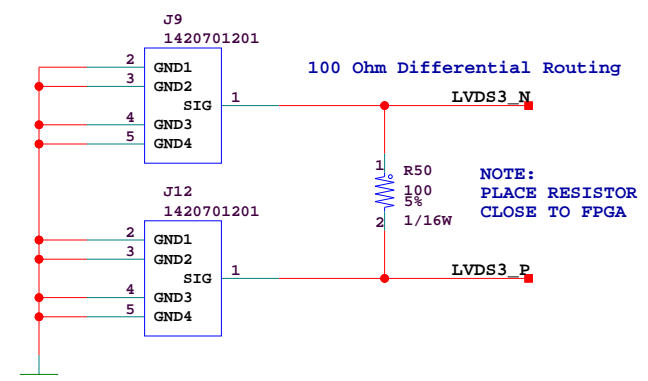
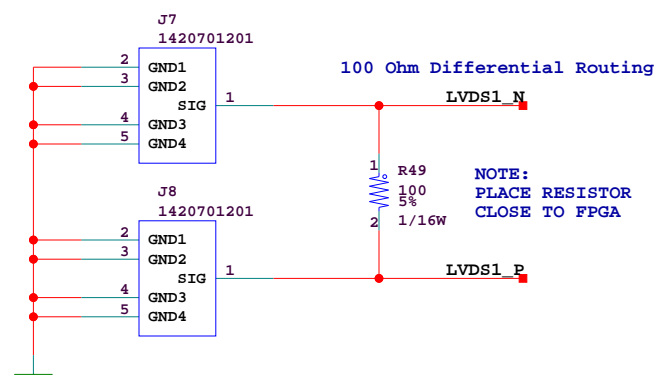
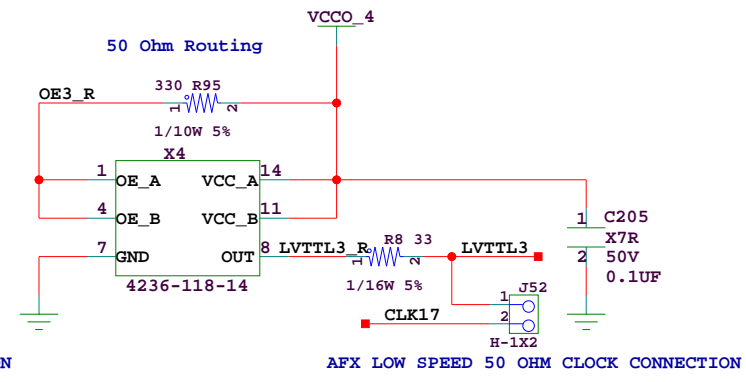
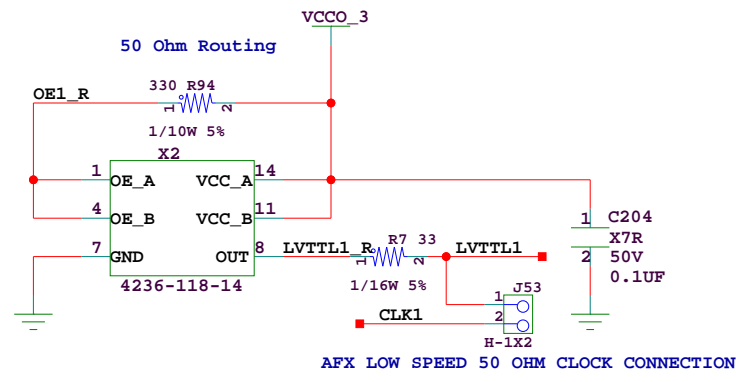
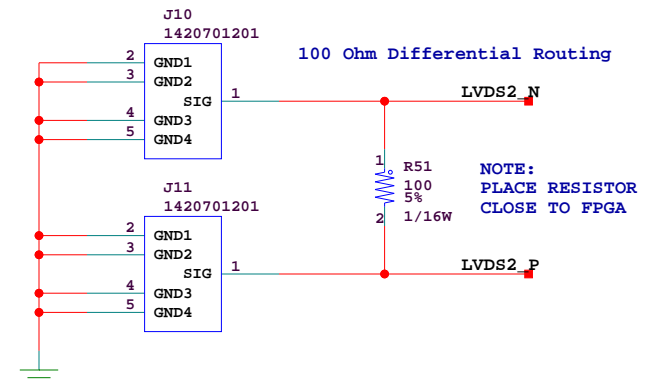
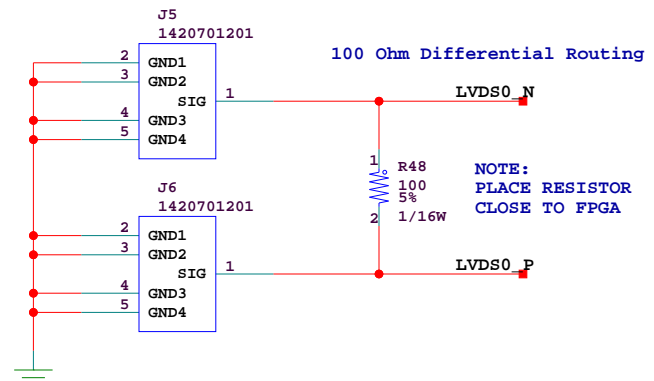
		SCH P/N	0381233
		ART P/N	0531592
		FAB P/N	1280404
<b>Title:</b> SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404			
<b>CONFIGURATION</b>			
Date: 2-19-2008_12:14		Ver: C	
Sheet Size: B		Rev: 02	
Sheet 4	of 21	Drawn By	s.s.

UPPER CLOCKS

BOTTOM CLOCKS

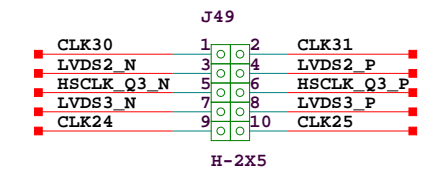
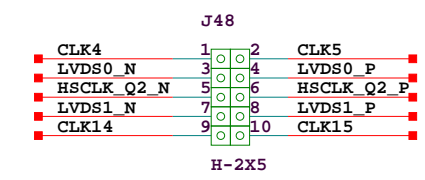


2676\_9318\_XX\_2431



AFX CLOCK CONFIGURATION

- 1-3, 2-4: LOW SPEED 50 OHM CLOCK CONNECTION
- 3-5, 4-6: HIGH SPEED 100 OHM DIFFERENTIAL CLOCK CONNECTION TO DIFFERENTIAL PAIR
- 5-7, 6-8: HIGH SPEED 100 OHM DIFFERENTIAL CLOCK CONNECTION TO DIFFERENTIAL PAIR
- 7-9, 8-10: LOW SPEED 50 OHM CLOCK CONNECTION



SCH P/N 0381233

ART P/N 0531592

FAB P/N 1280404

Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404

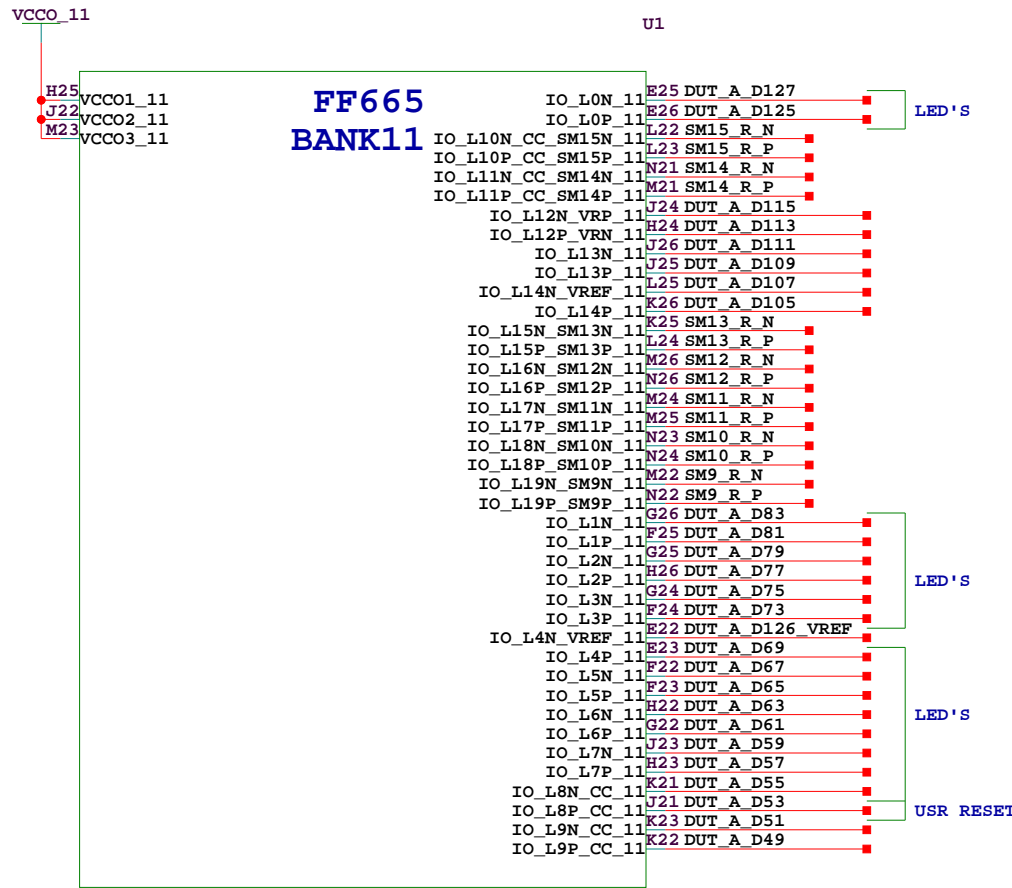
**SOCKET CLOCKS, SMA DIFF CLOCKS**

Date: 2-19-2008\_12:14 Ver: C

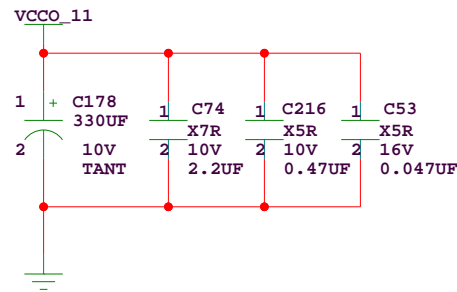
Sheet Size: B Rev: 02

Sheet 5 of 21 Drawn By s.s.

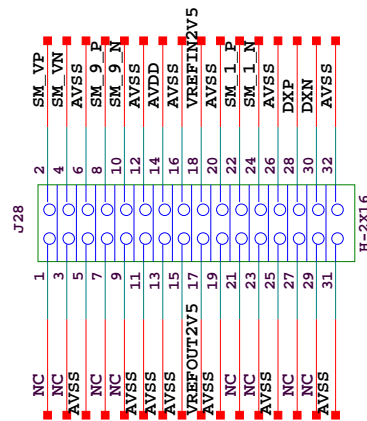




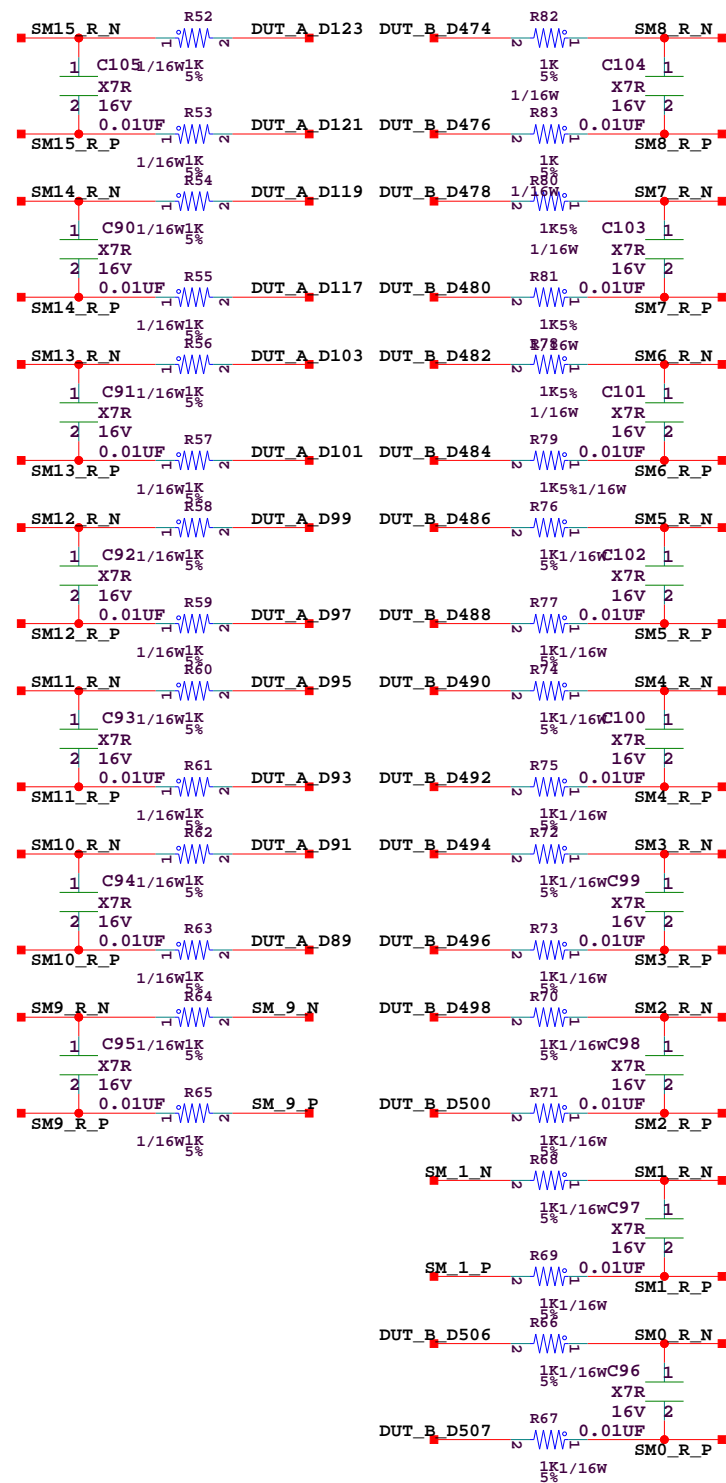
2676\_9318\_XX\_2431



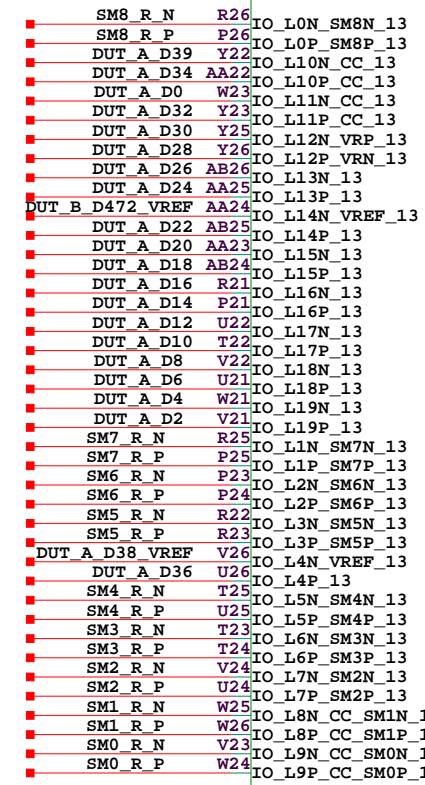
SYSTEM MONITOR MALE CONNECTOR



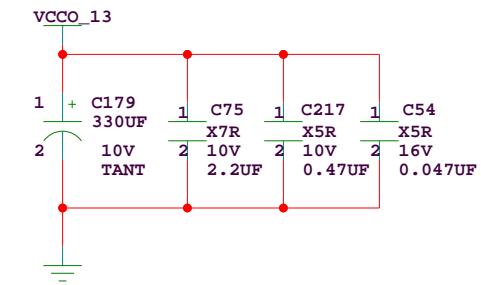
SYSTEM MONITOR FILTERS



U1



2676\_9318\_XX\_2431



SCH P/N 0381233  
ART P/N 0531592  
FAB P/N 1280404

Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404

SYSTEM MONITOR

Date: 2-19-2008\_12:14

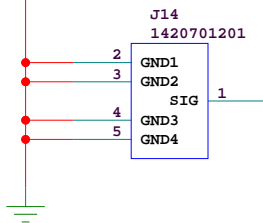
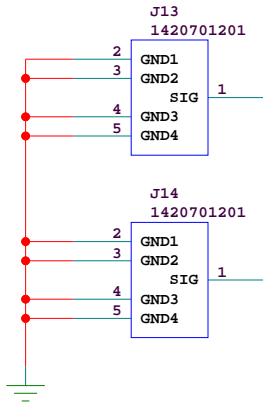
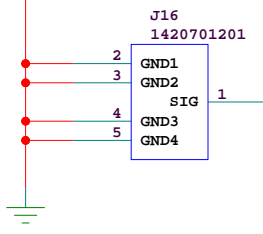
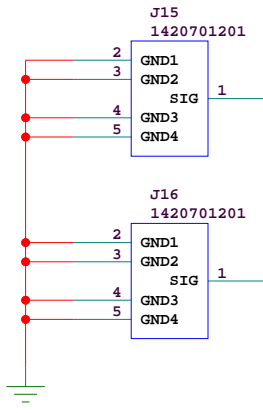
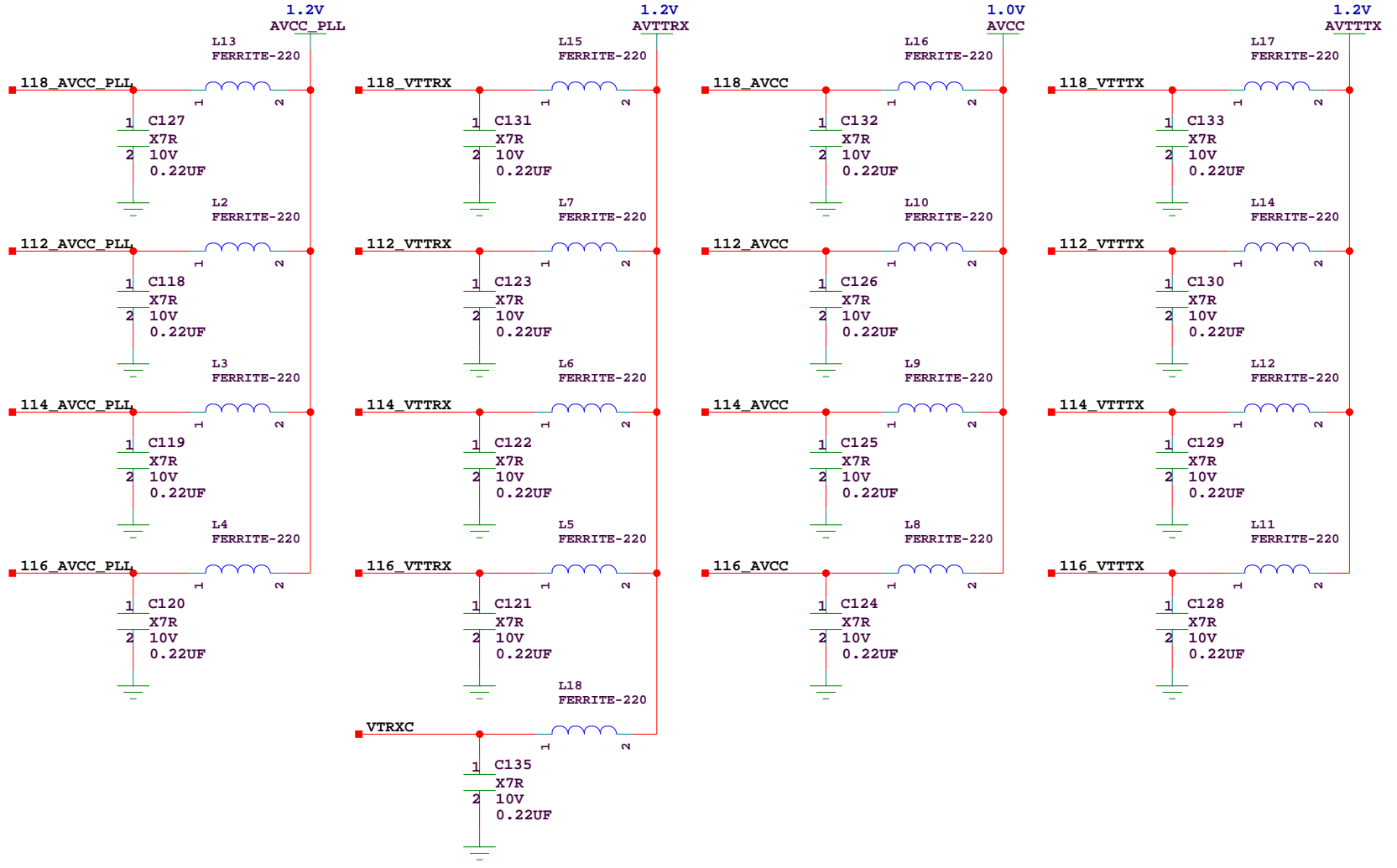
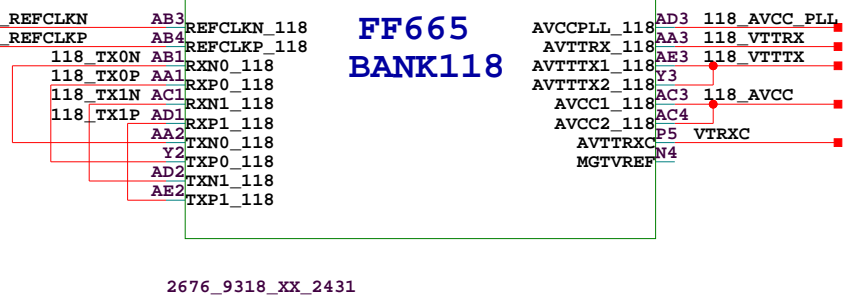
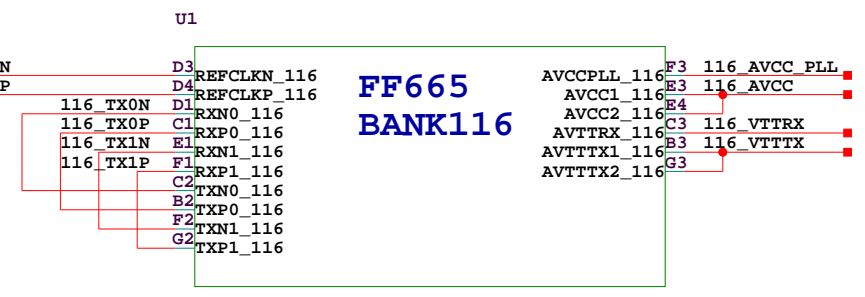
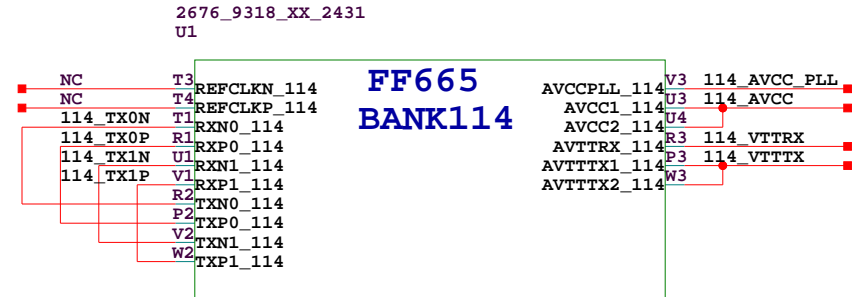
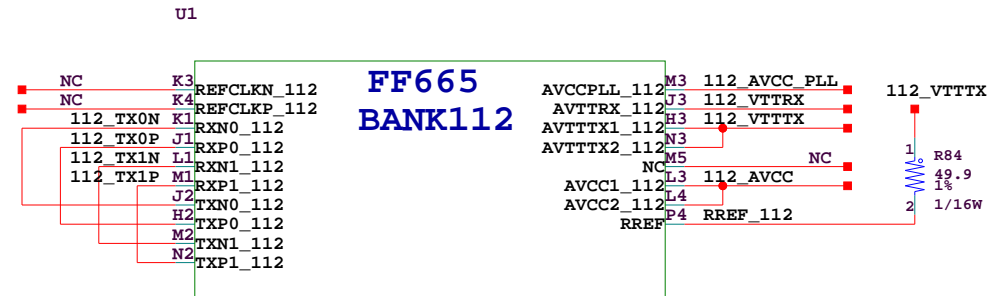
Ver: C

Sheet Size: B

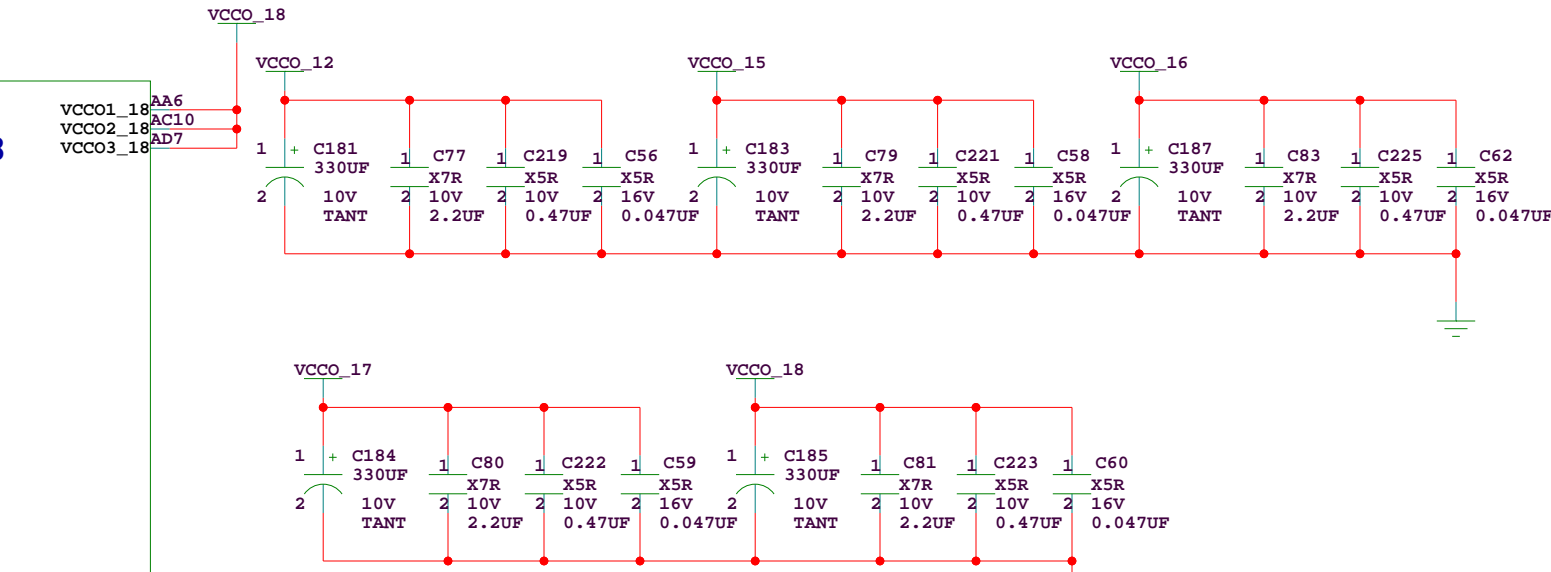
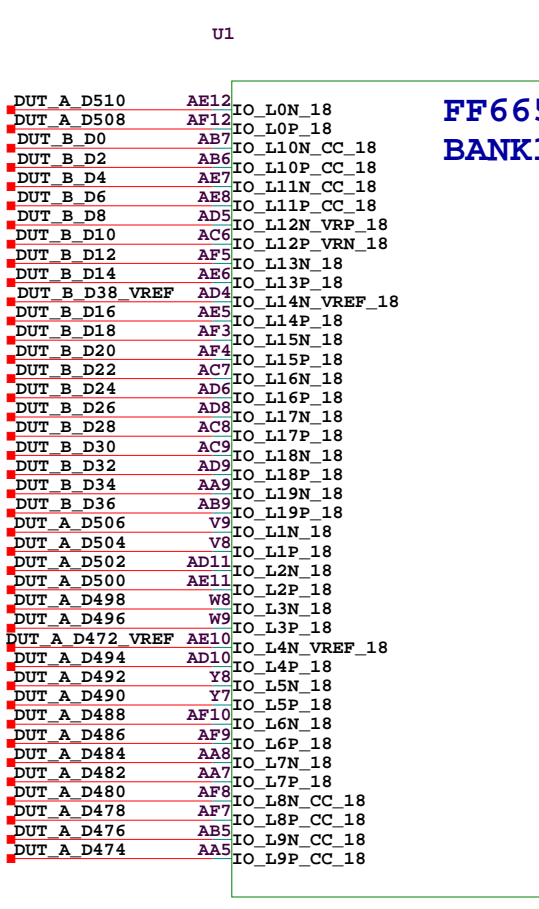
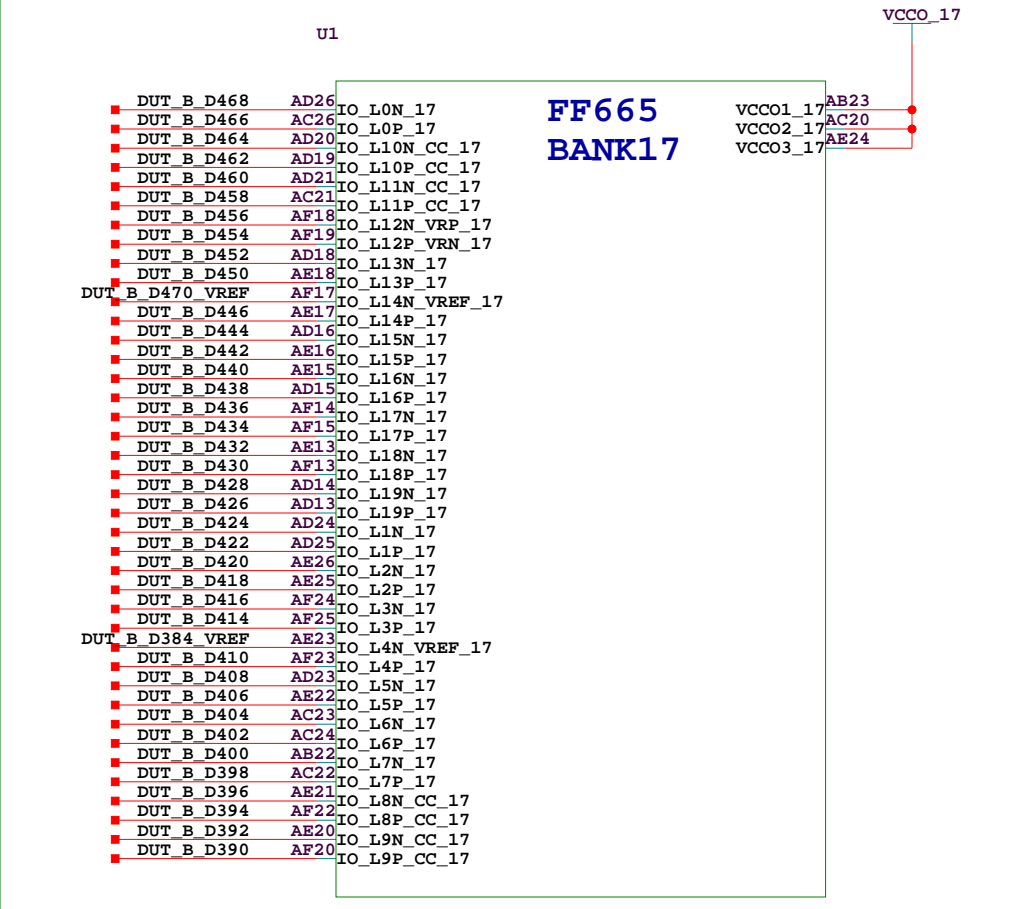
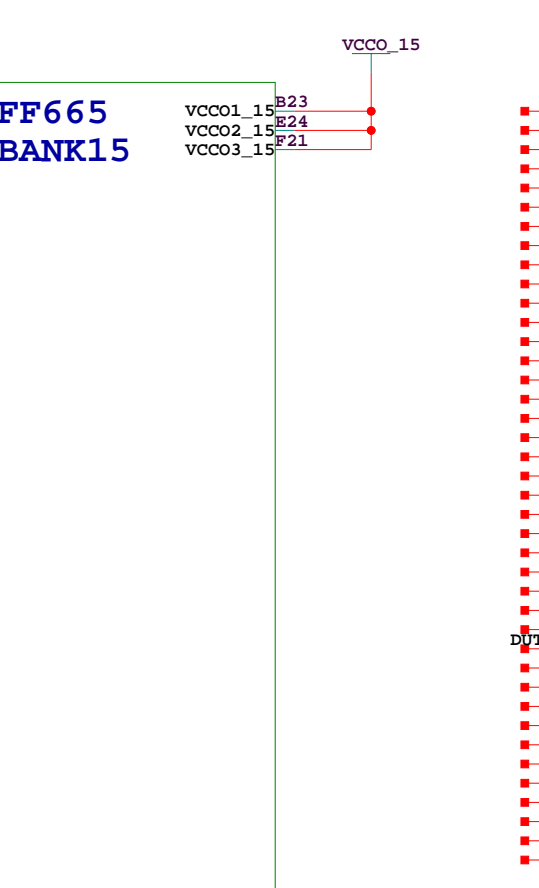
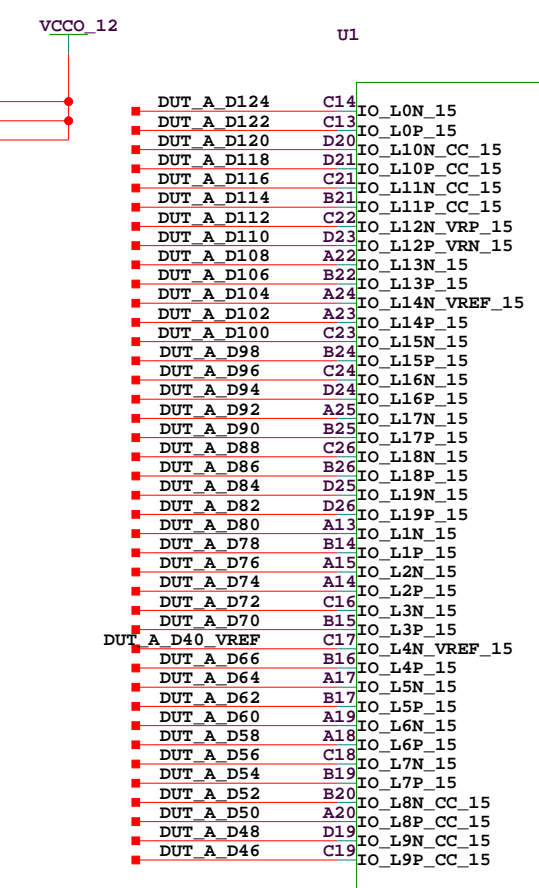
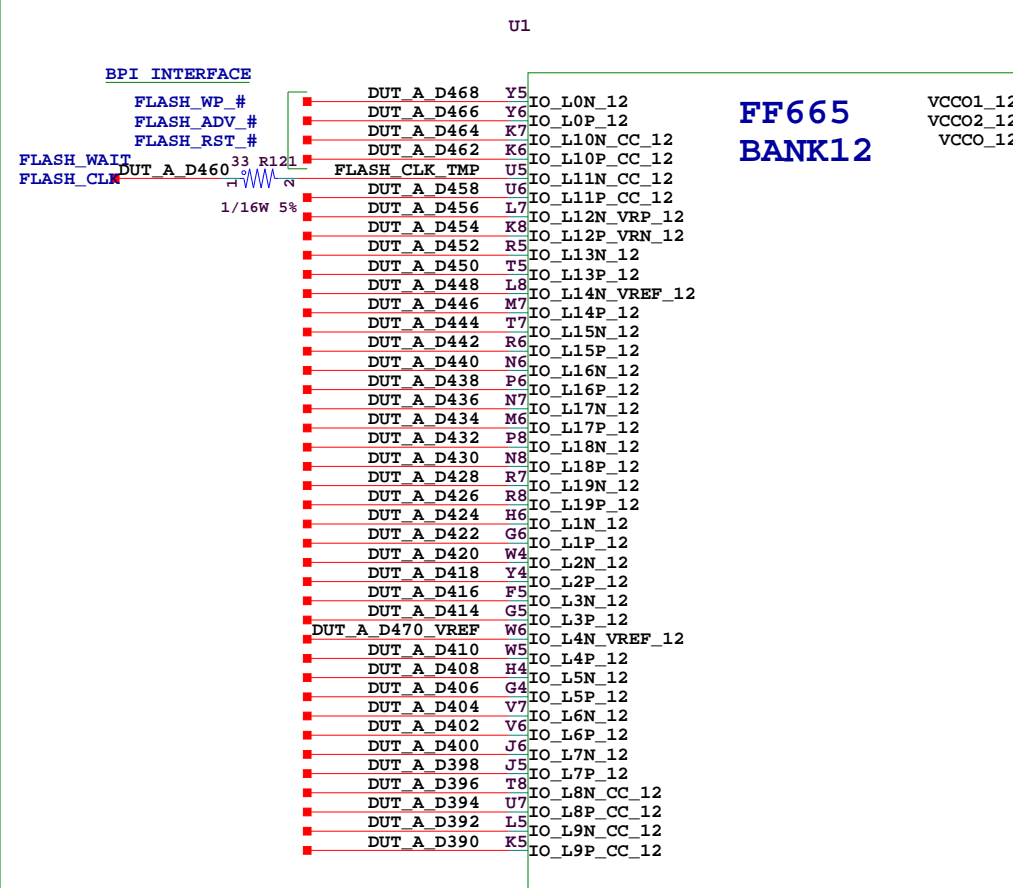
Rev: 02

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Drawn By s.s



		SCH P/N	0381233
		ART P/N	0531592
		FAB P/N	1280404
<b>Title:</b> SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404 <b>MGT LOOPBACK 112,114,116,118</b>			
<b>Date:</b> 2-19-2008_12:14		<b>Ver:</b> C	
<b>Sheet Size:</b> B		<b>Rev:</b> 02	
<b>Sheet</b> 7	<b>of</b> 21	<b>Drawn By</b> s.s.	



**XILINX**

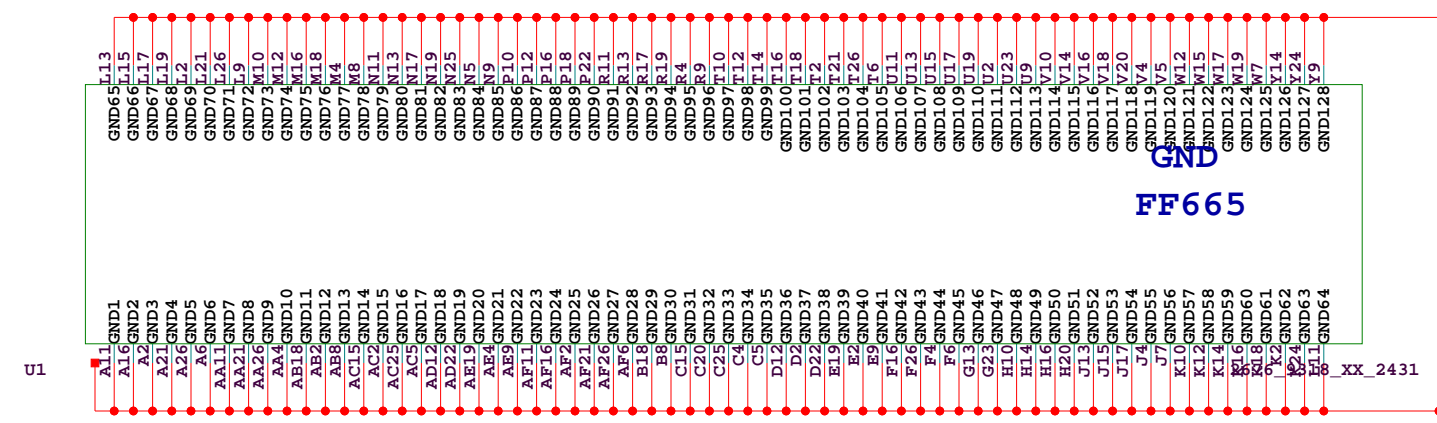
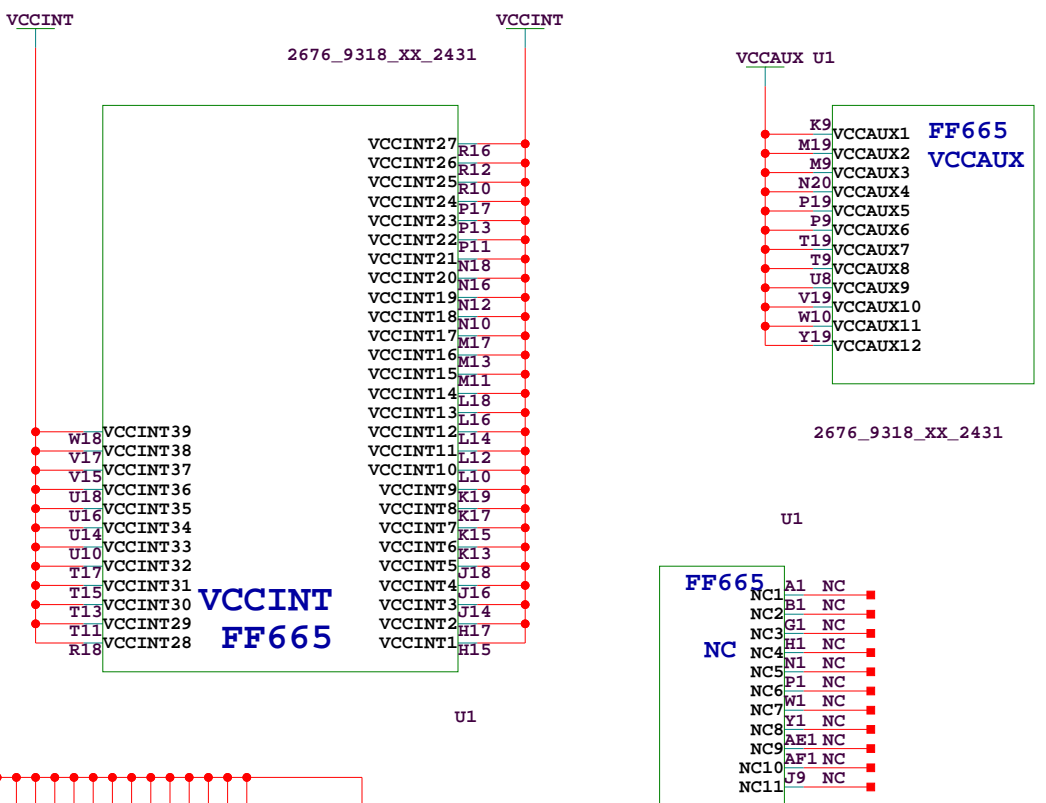
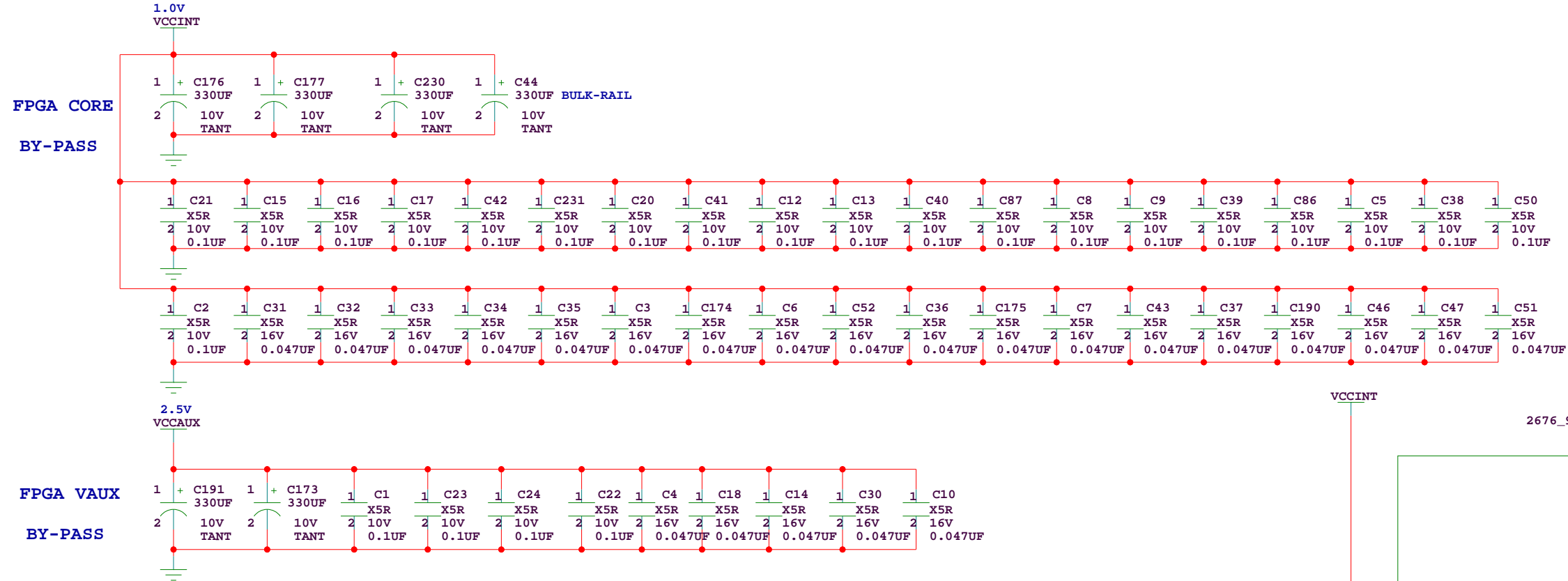
SCH P/N 0381233  
ART P/N 0531592  
FAB P/N 1280404

Title:  
SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404

**DUT INTERFACE**

Date: 2-19-2008\_12:14 Ver: C  
Sheet Size: B Rev: 02  
Sheet 8 of 21 Drawn By s.s.





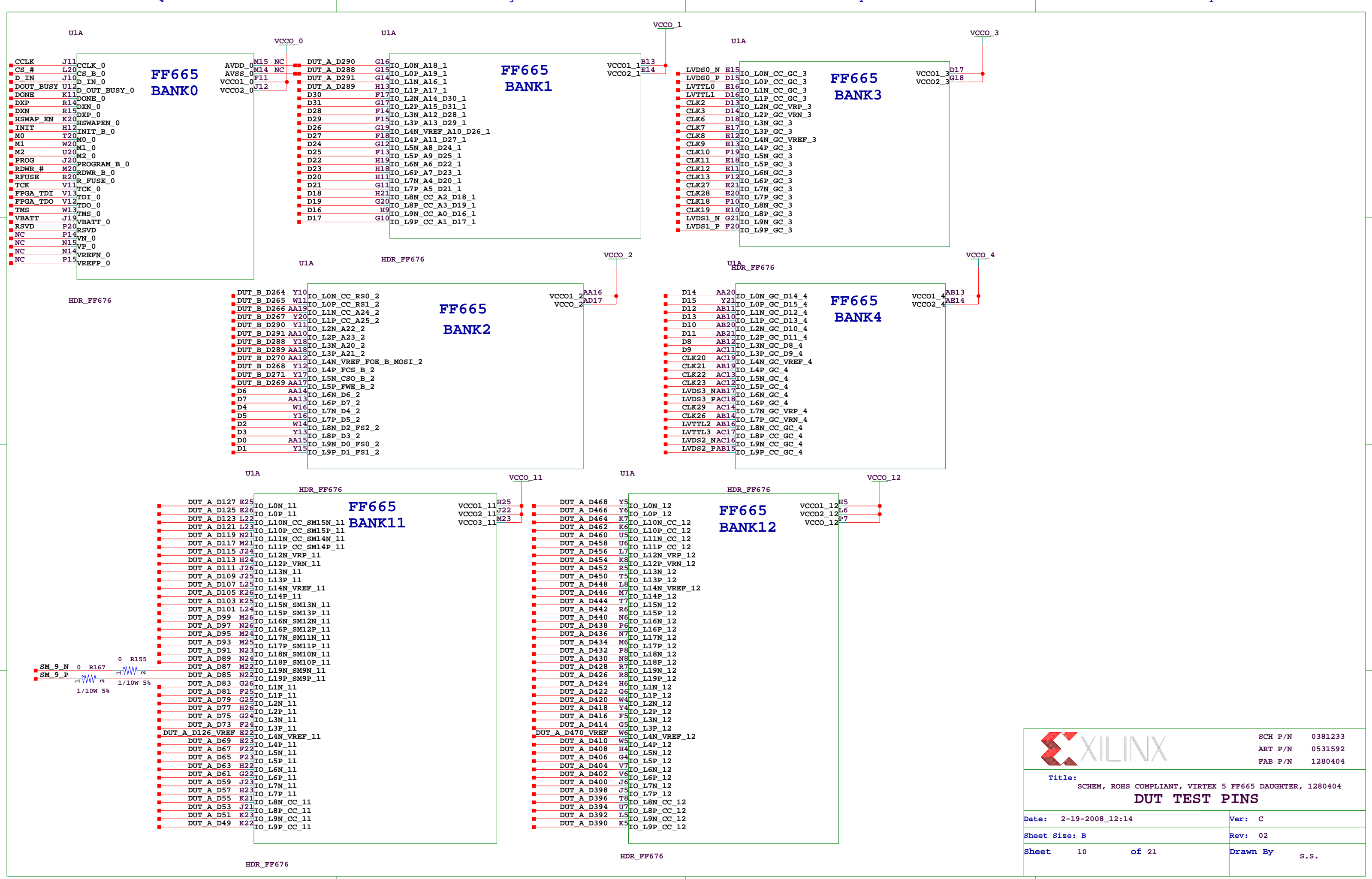
**Title:** SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404  
**FPGA DECOUPLING CAPACITORS**

**Date:** 2-19-2008\_12:14 **Ver:** C

**Sheet Size:** B **Rev:** 02

**Sheet** 9 **of** 21 **Drawn By** s.s.

SCH P/N 0381233  
ART P/N 0531592  
FAB P/N 1280404



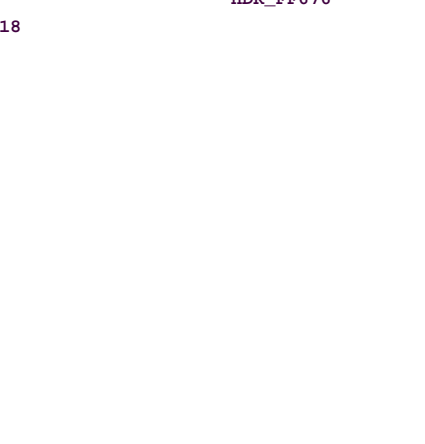
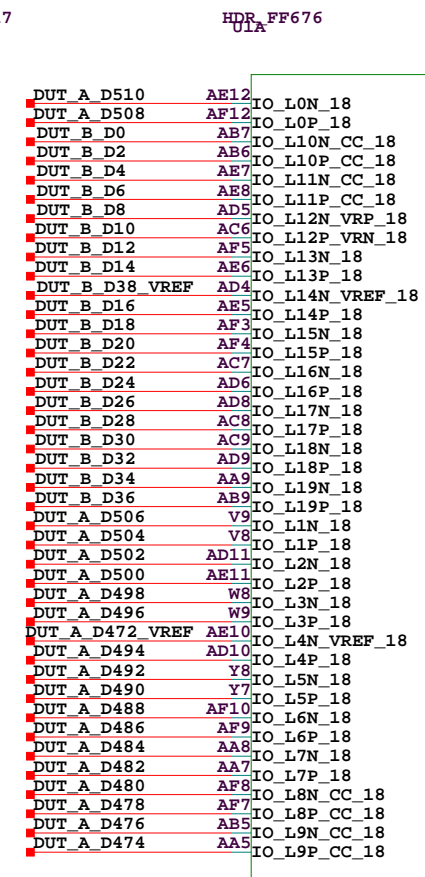
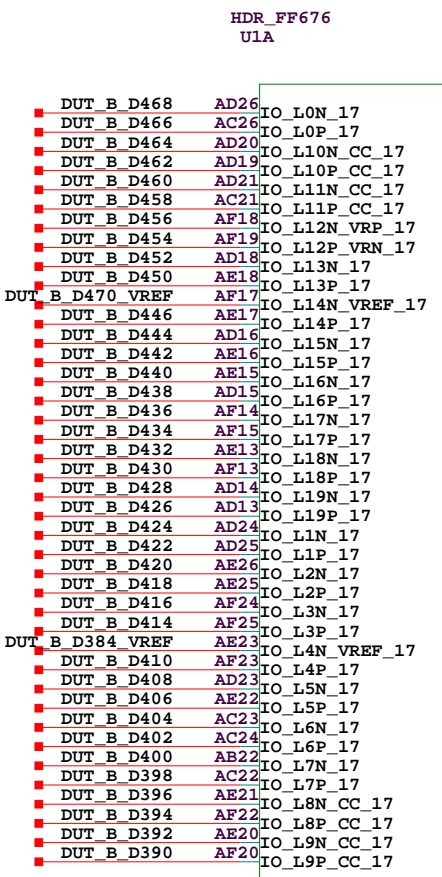
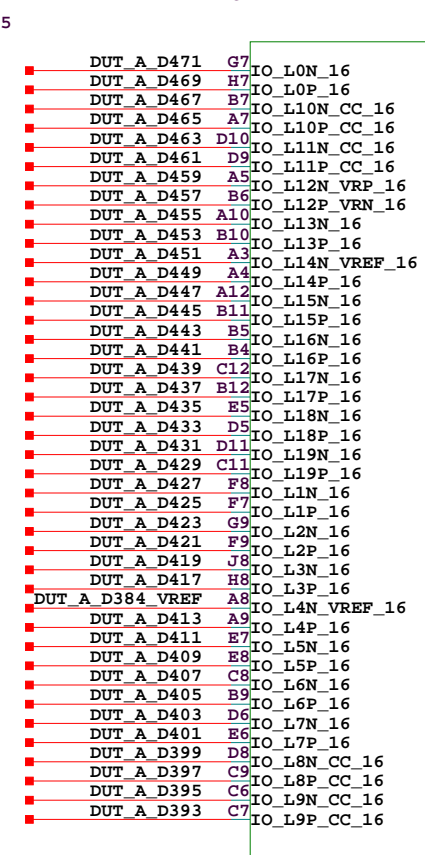
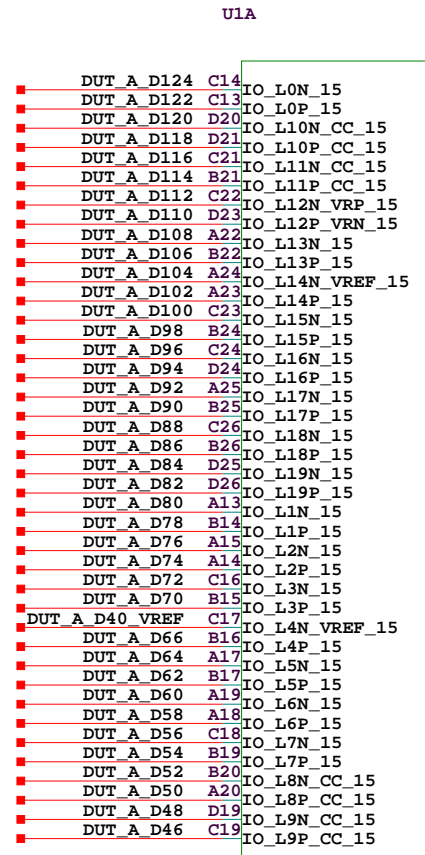
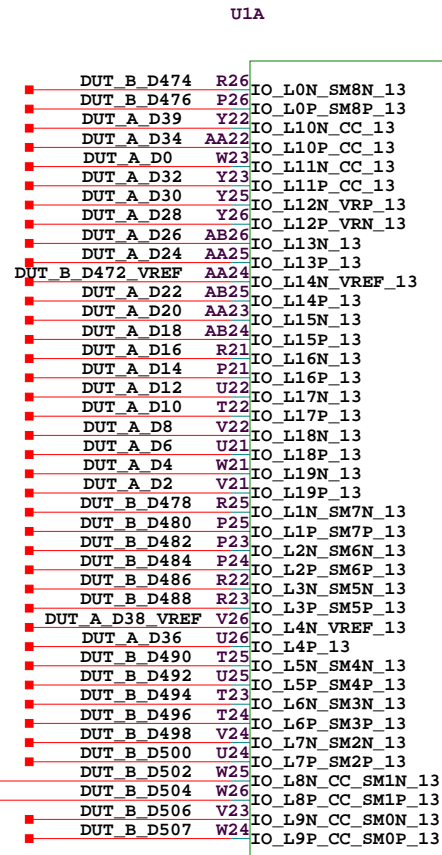
**XILINX**

SCH P/N 0381233  
 ART P/N 0531592  
 FAB P/N 1280404

Title:  
 SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404

**DUT TEST PINS**

Date: 2-19-2008\_12:14 Ver: C  
 Sheet Size: B Rev: 02  
 Sheet 10 of 21 Drawn By s.s.



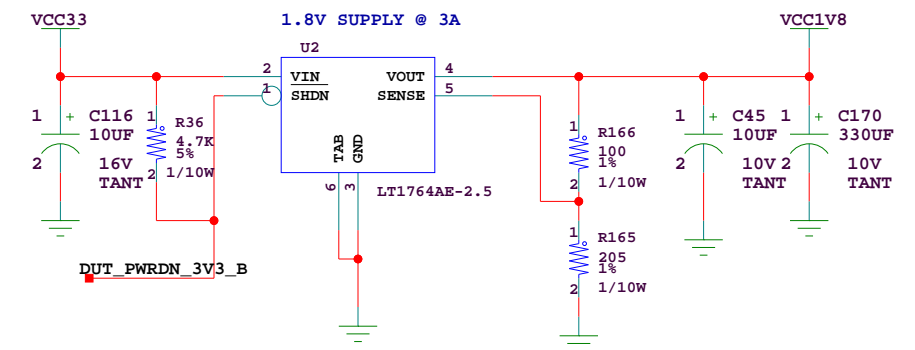
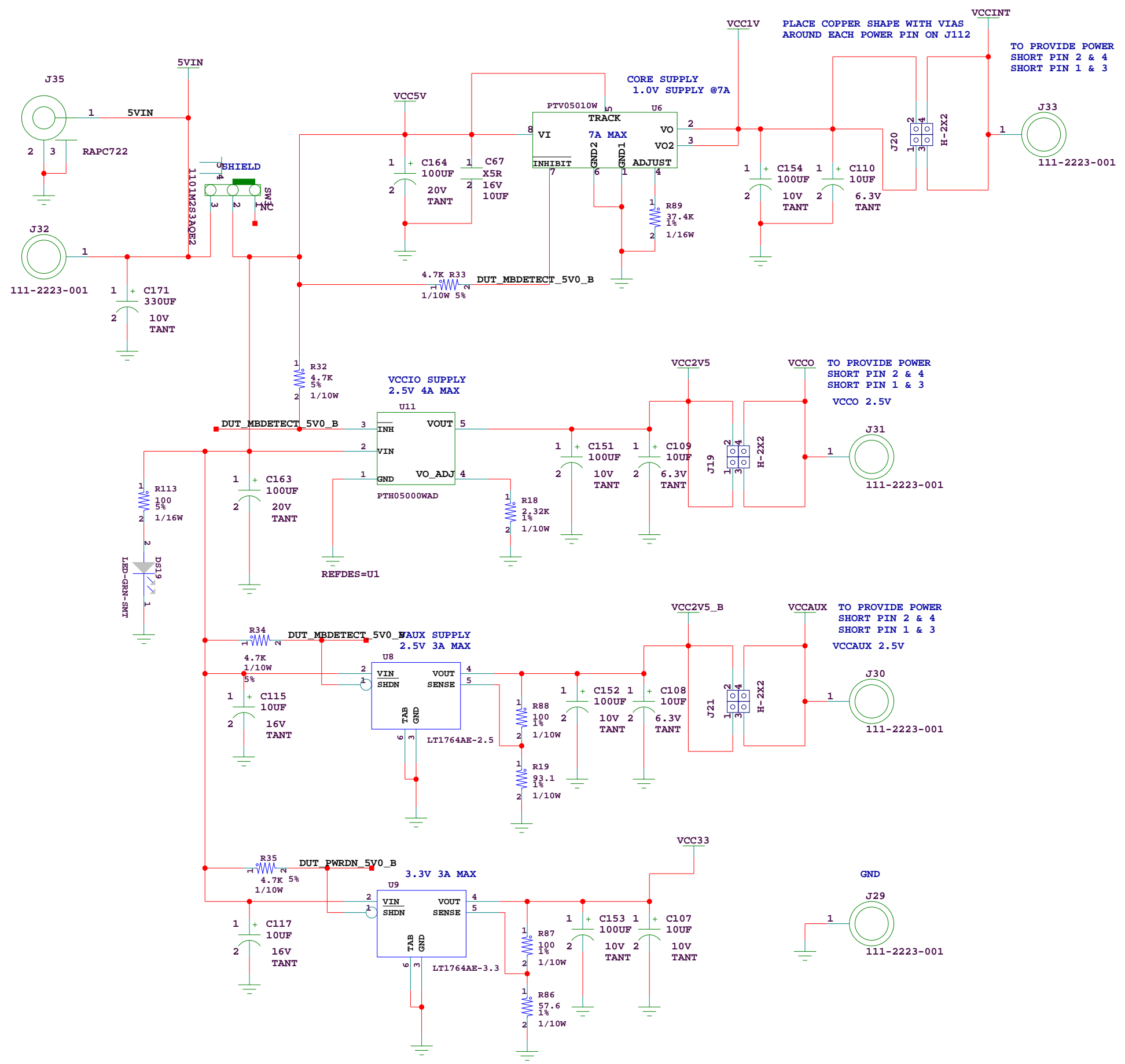
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SCH P/N 0381233  
ART P/N 0531592  
FAB P/N 1280404

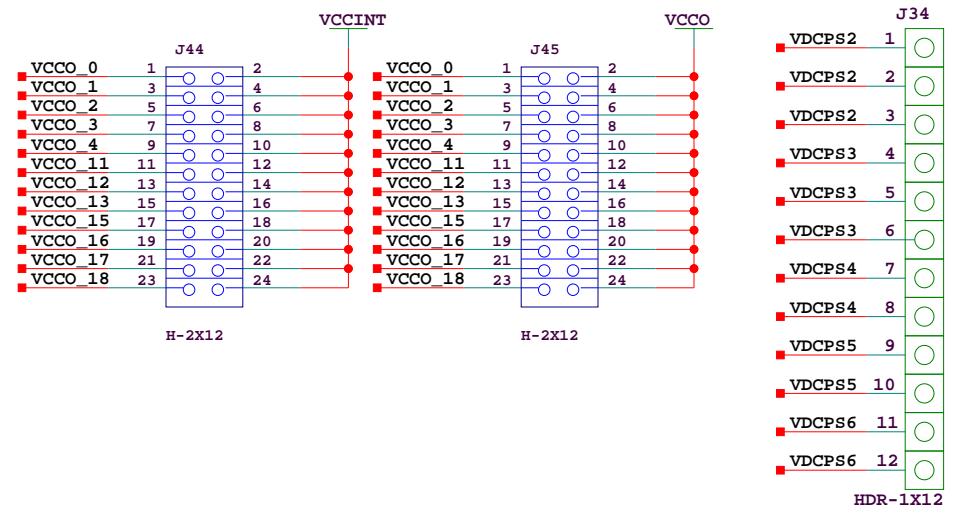
Title:  
SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404

**DUT TEST PINS**

Date: 2-19-2008\_12:14 Ver: C  
Sheet Size: B Rev: 02  
Sheet 11 of 21 Drawn By s.s.



**VCC I/O SELECTION**

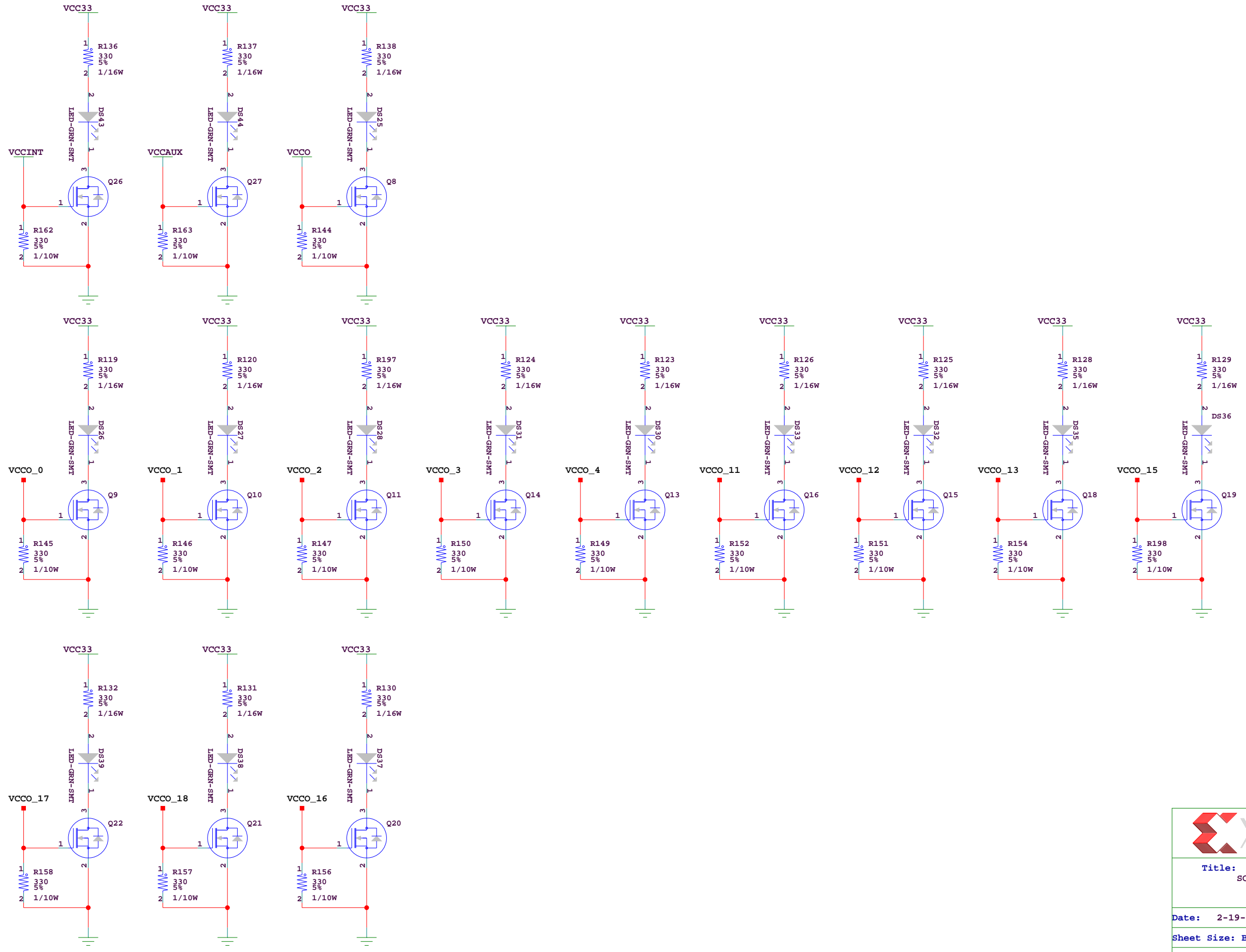



**XILINX**

SCH P/N 0381233  
 ART P/N 0531592  
 FAB P/N 1280404

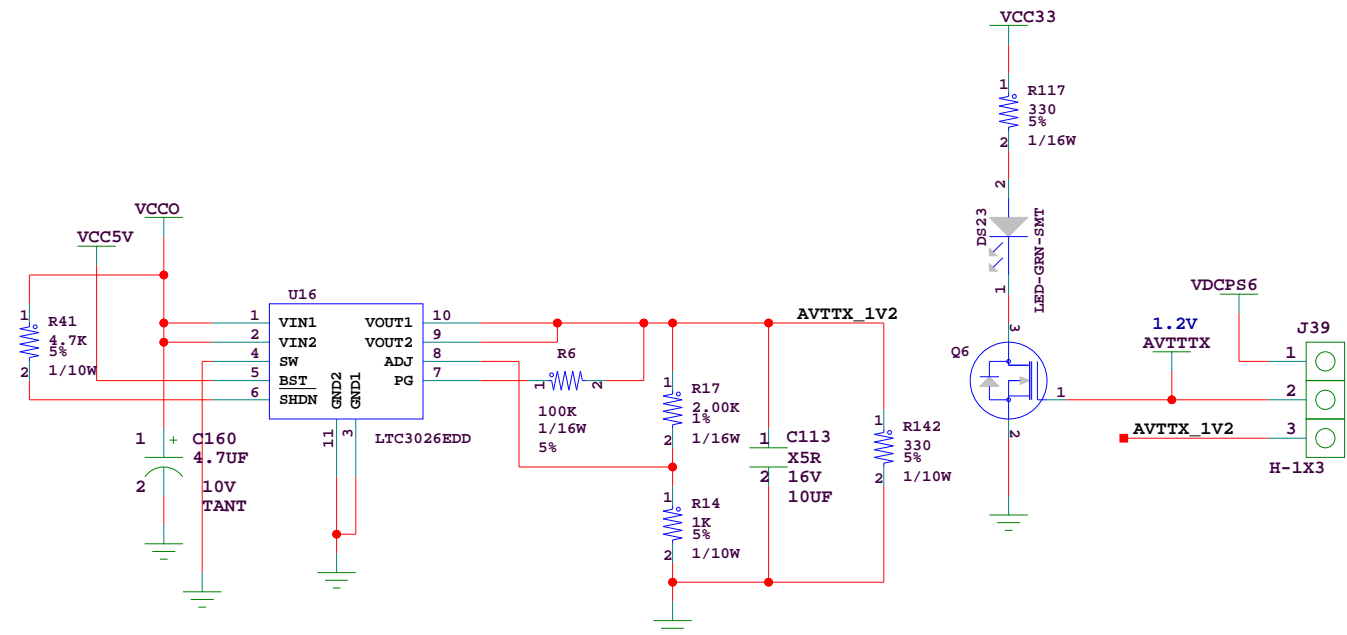
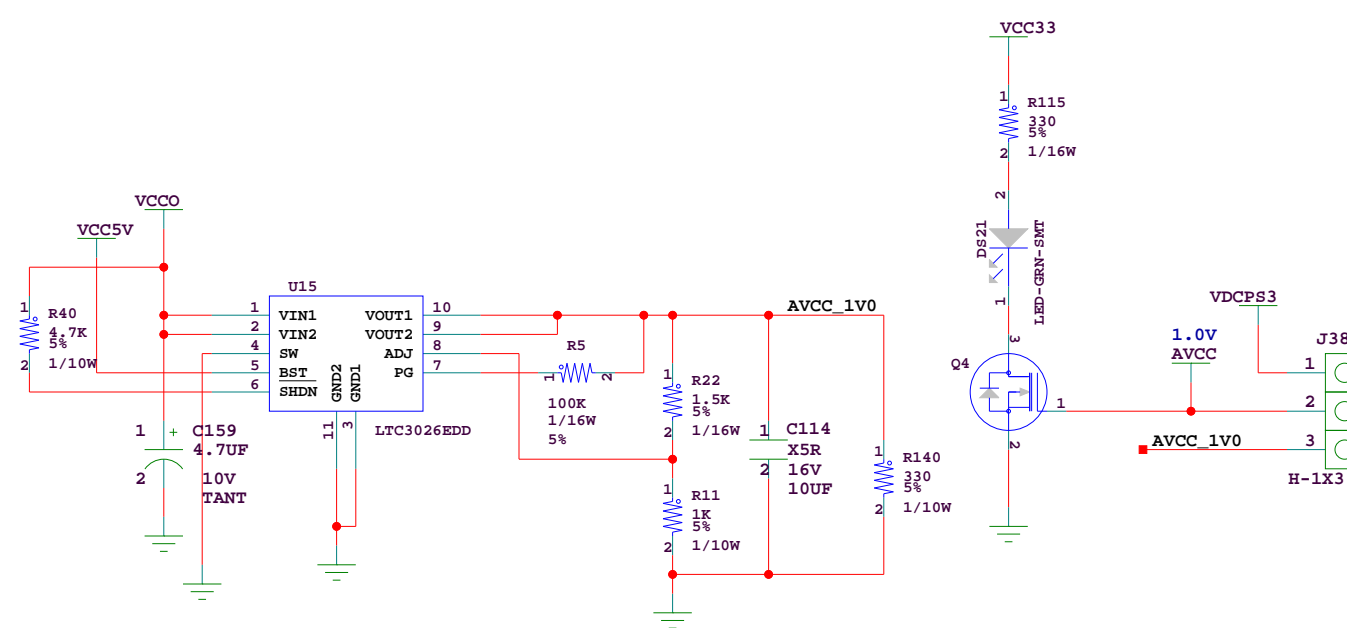
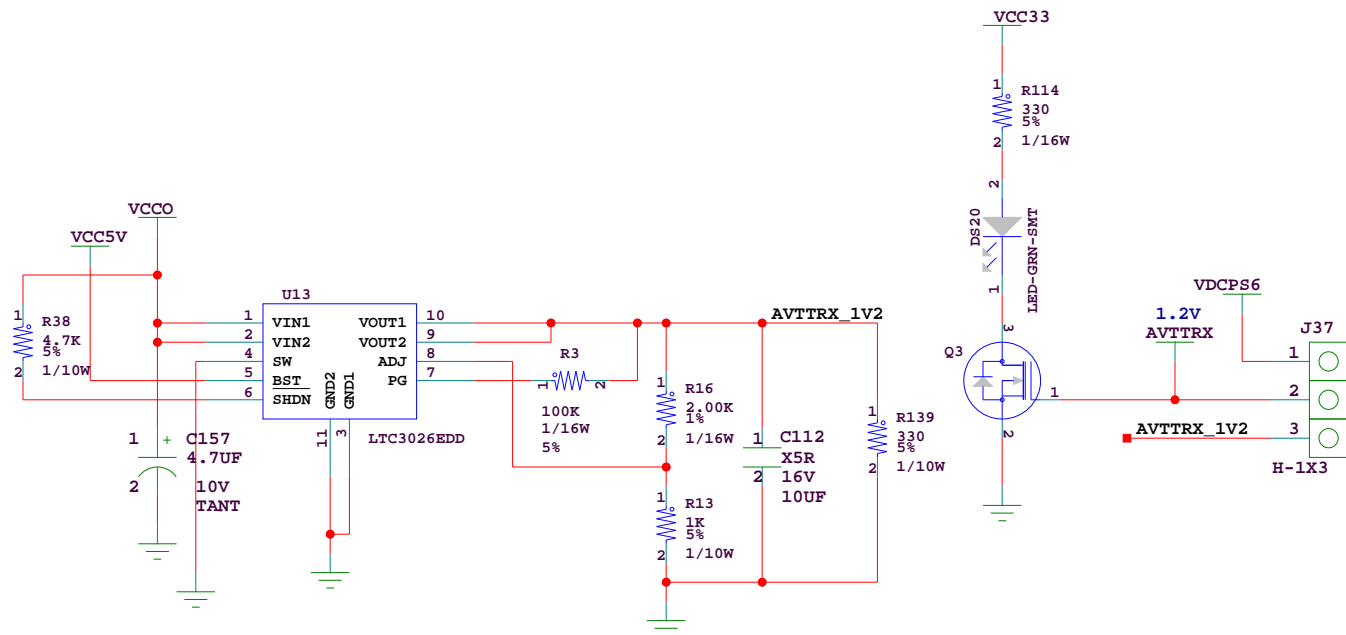
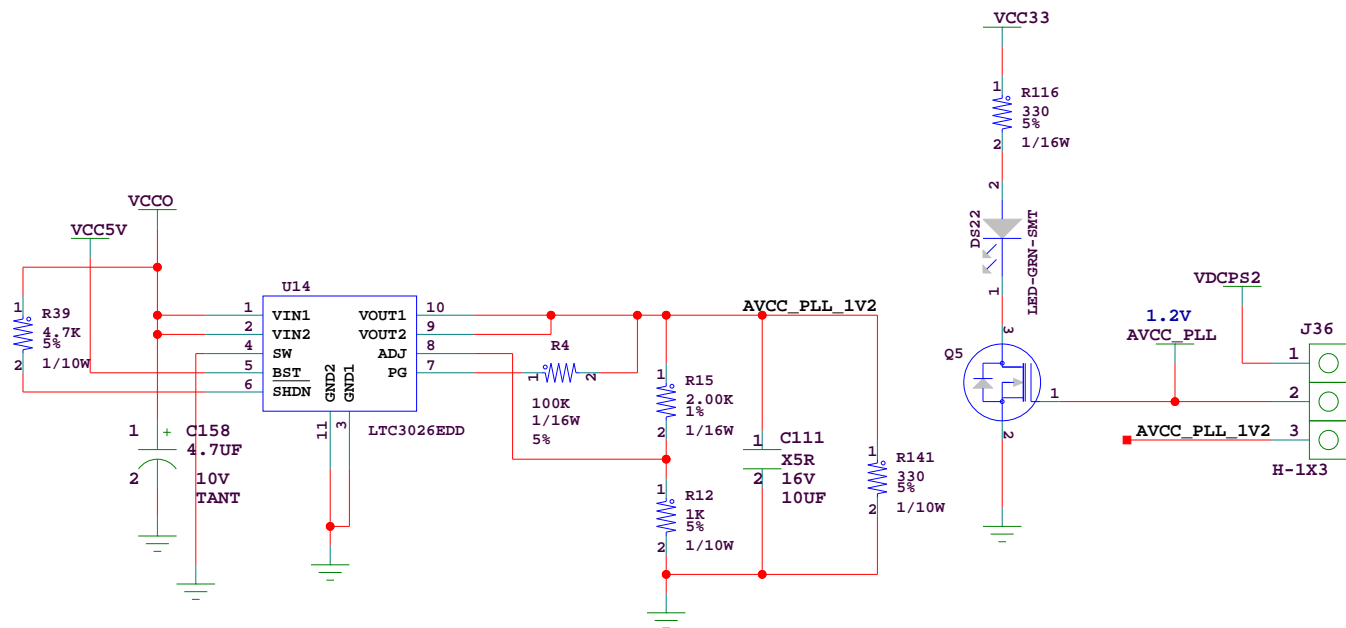
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404  
**FPGA POWER SUPPLY**

Date: 2-19-2008\_12:14 Ver: C  
 Sheet Size: B Rev: 02  
 Sheet 12 of 21 Drawn By s.s.



		SCH P/N	0381233
		ART P/N	0531592
		FAB P/N	1280404
<b>Title:</b> SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404 <b>POWER LED INDICATORS</b>			
<b>Date:</b> 2-19-2008_12:13		<b>Ver:</b> C	
<b>Sheet Size:</b> B		<b>Rev:</b> 02	
<b>Sheet</b> 13 <b>of</b> 21		<b>Drawn By</b> s.s.	



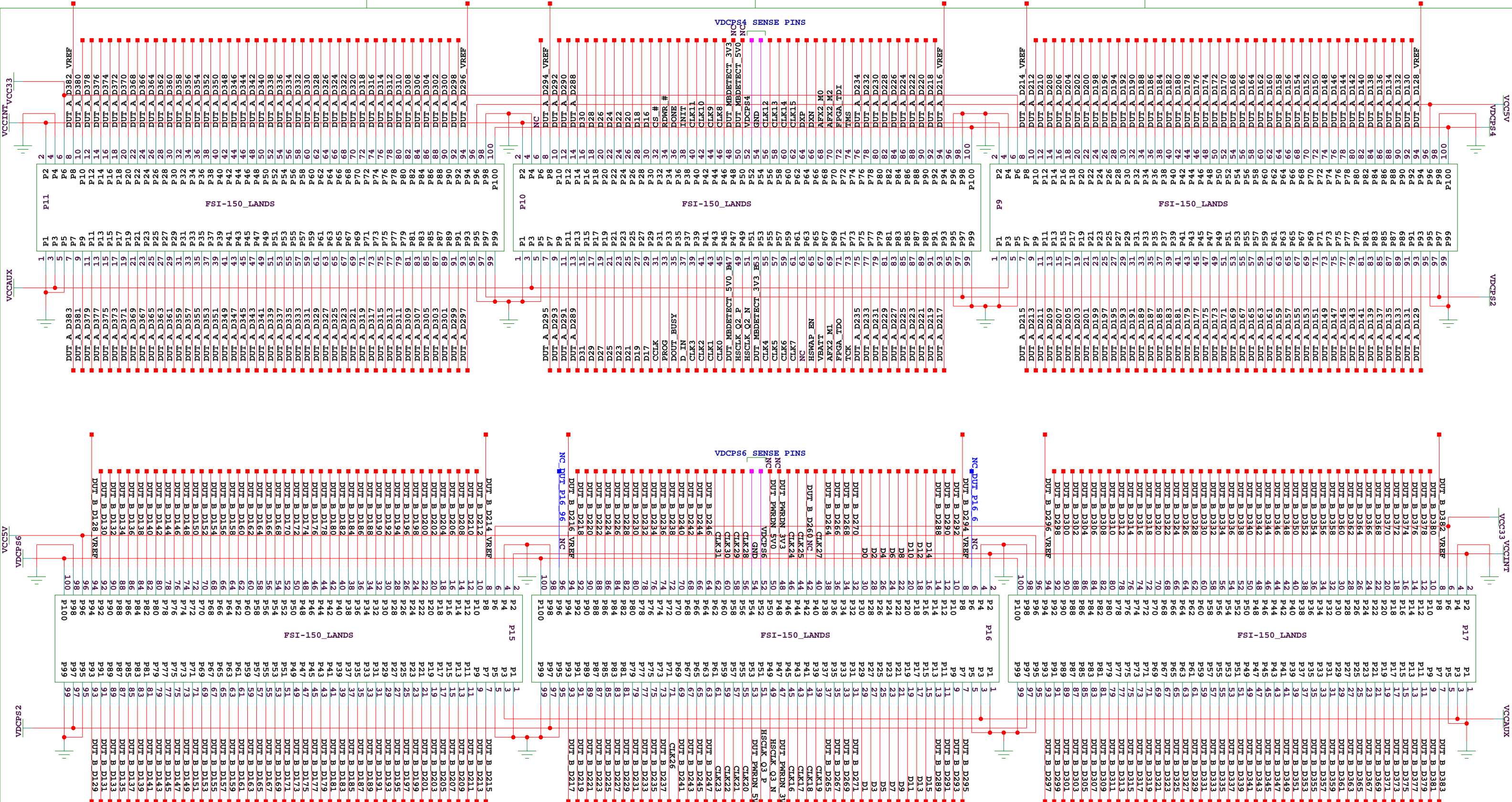


SCH P/N 0381233  
 ART P/N 0531592  
 FAB P/N 1280404

Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404

**MGT POWER SUPPLY**

Date: 2-19-2008_12:13	Ver: C
Sheet Size: B	Rev: 02
Sheet 14 of 21	Drawn By s.s.



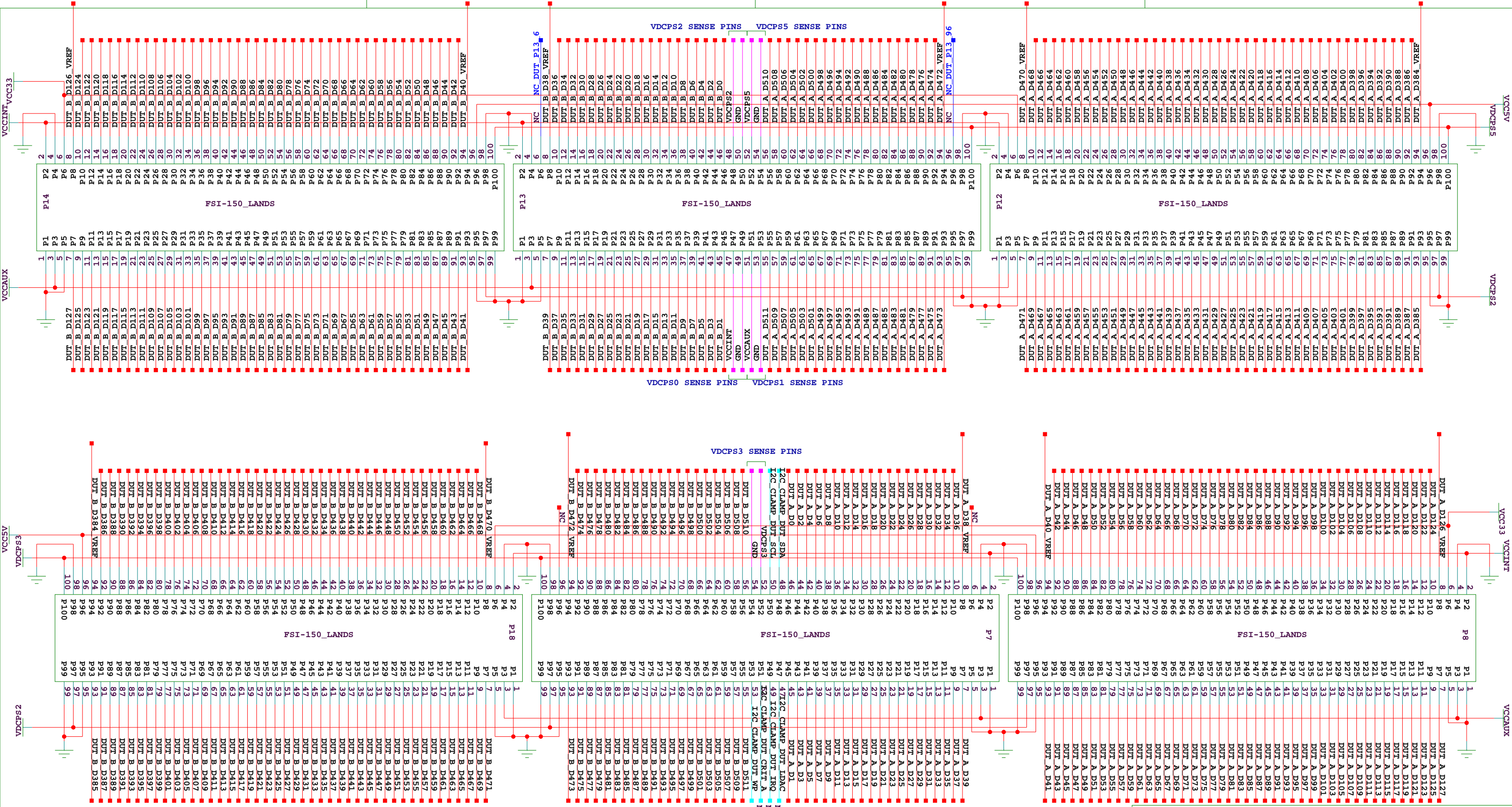
SCH P/N 0381233  
 ART P/N 0531592  
 FAB P/N 1280404


Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404  
**AFX LANDINGS TOP AND BOTTOM**

Date: 2-19-2008\_12:13 Ver: C

Sheet Size: B Rev: 02

Sheet 15 of 21 Drawn By s.s.





SCH P/N 0381233  
ART P/N 0531592  
FAB P/N 1280404

**Title:**  
SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404

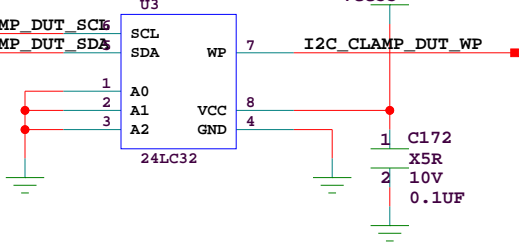
## AFX LANDINGS LEFT AND RIGHT

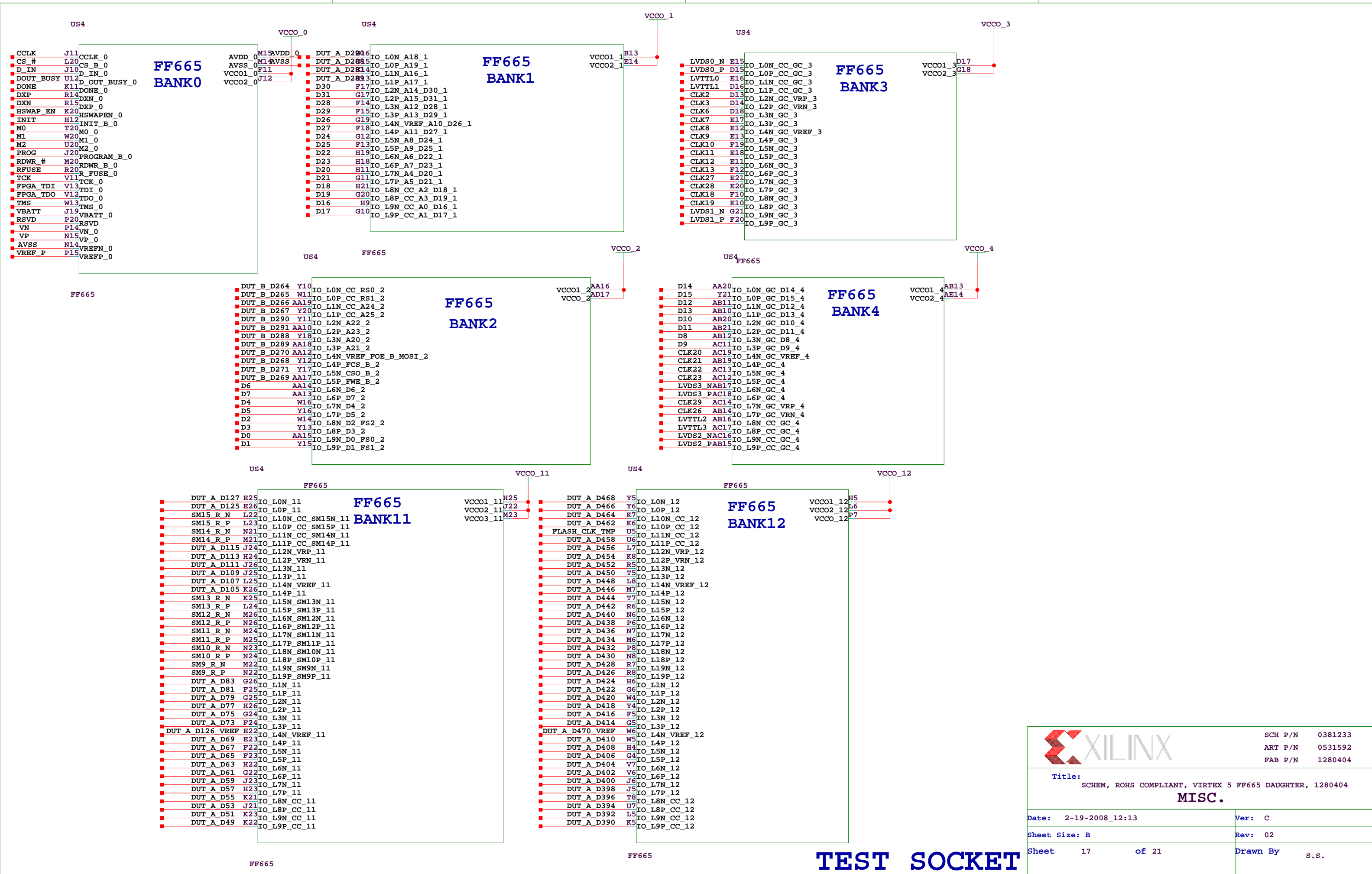
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**Sheet Size:** B      **Rev:** 02

**Sheet** 16 **of** 21      **Drawn By** s.s.

### I2C EEPROM





US4

CCLK	J11	CCLK_0
CS #	L20	CS_B_0
D_IN	J10	D_IN_0
DOUT_BUSY	U12	D_OUT_BUSY_0
DONE	K11	DONE_0
DXP	R14	DXP_0
DXN	R15	DXP_0
HSWAP_EN	K20	HSWAPEN_0
INIT	H12	INIT_B_0
MO	T20	MO_0
M1	W20	M1_0
M2	U20	M2_0
PROG	J20	PROGRAM_B_0
RDWR #	M20	RDWR_B_0
RFUSE	R20	R_FUSE_0
TCK	V11	TCK_0
FPGA_TDI	V13	TDI_0
FPGA_TDO	V12	TDO_0
TMS	W13	TMS_0
VBATT	J19	VBATT_0
RSVD	P20	RSVD
VN	P14	VN_0
VP	N15	VP_0
AVSS	N14	VREFN_0
VREF_P	P15	VREFP_0

**FF665 BANK0**

US4

M1SAVDD	0	DUT A D2806	IO L0N_A18_1
M1AVSS	1	DUT A D2885	IO L0P_A19_1
F11	1	DUT A D2814	IO L1N_A16_1
J12	1	DUT A D2893	IO L1P_A17_1
D30	F17		IO L2N_A14_D30_1
D31	G17		IO L2P_A15_D31_1
D28	F14		IO L3N_A12_D28_1
D29	F15		IO L3P_A13_D29_1
D26	G19		IO L4N_VREF_A10_D26_1
D27	F18		IO L4P_A11_D27_1
D24	G12		IO L5N_A8_D24_1
D25	F13		IO L5P_A9_D25_1
D22	H19		IO L6N_A6_D22_1
D23	H18		IO L6P_A7_D23_1
D20	H11		IO L7N_A4_D20_1
D21	G11		IO L7P_A5_D21_1
D18	H21		IO L8N_CC_A2_D18_1
D19	G20		IO L8P_CC_A3_D19_1
D16	H9		IO L9N_CC_A0_D16_1
D17	G10		IO L9P_CC_A1_D17_1

**FF665 BANK1**

US4

LVDS0_N	E15	IO L0N_CC_GC_3
LVDS0_P	D15	IO L0P_CC_GC_3
LVTTLO	E16	IO L1N_CC_GC_3
LVTTL1	D16	IO L1P_CC_GC_3
CLK2	D13	IO L2N_GC_VRP_3
CLK3	D14	IO L2P_GC_VRN_3
CLK6	D18	IO L3N_GC_3
CLK7	E17	IO L3P_GC_3
CLK8	E12	IO L4N_GC_VREF_3
CLK9	E13	IO L4P_GC_3
CLK10	F19	IO L5N_GC_3
CLK11	E18	IO L5P_GC_3
CLK12	E11	IO L6N_GC_3
CLK13	F12	IO L6P_GC_3
CLK27	E21	IO L7N_GC_3
CLK28	E20	IO L7P_GC_3
CLK18	F10	IO L8N_GC_3
CLK19	E10	IO L8P_GC_3
LVDS1_N	G21	IO L9N_GC_3
LVDS1_P	F20	IO L9P_GC_3

**FF665 BANK3**

FF665

DUT B D264	Y10	IO L0N_CC_RS0_2
DUT B D265	W11	IO L0P_CC_RS1_2
DUT B D266	AA19	IO L1N_CC_A24_2
DUT B D267	Y20	IO L1P_CC_A25_2
DUT B D290	Y11	IO L2N_A22_2
DUT B D291	AA10	IO L2P_A23_2
DUT B D288	Y18	IO L3N_A20_2
DUT B D289	AA18	IO L3P_A21_2
DUT B D270	AA12	IO L4N_VREF_FOE_B_MOSI_2
DUT B D268	Y12	IO L4P_FCS_B_2
DUT B D271	Y17	IO L5N_CSO_B_2
DUT B D269	AA17	IO L5P_FWE_B_2
D6	AA14	IO L6N_D6_2
D7	AA13	IO L6P_D7_2
D4	W16	IO L7N_D4_2
D5	Y16	IO L7P_D5_2
D2	W14	IO L8N_D2_FS2_2
D3	Y13	IO L8P_D3_2
D0	AA15	IO L9N_D0_FS0_2
D1	Y15	IO L9P_D1_FS1_2

**FF665 BANK2**

US4

D14	AA20	IO L0N_GC_D14_4
D15	Y21	IO L0P_GC_D15_4
D12	AB11	IO L1N_GC_D12_4
D13	AB10	IO L1P_GC_D13_4
D10	AB20	IO L2N_GC_D10_4
D11	AB21	IO L2P_GC_D11_4
D8	AB12	IO L3N_GC_D8_4
D9	AC11	IO L3P_GC_D9_4
CLK20	AC19	IO L4N_GC_VREF_4
CLK21	AB19	IO L4P_GC_4
CLK22	AC13	IO L5N_GC_4
CLK23	AC12	IO L5P_GC_4
LVDS3_NAB17		IO L6N_GC_4
LVDS3_PAC18		IO L6P_GC_4
CLK29	AC14	IO L7N_GC_VRP_4
CLK26	AB14	IO L7P_GC_VRN_4
LVTTL2	AB16	IO L8N_CC_GC_4
LVTTL3	AC17	IO L8P_CC_GC_4
LVDS2_NAC16		IO L9N_CC_GC_4
LVDS2_PAB15		IO L9P_CC_GC_4

**FF665 BANK4**

US4

DUT A D127	E25	IO L0N_11
DUT A D125	E26	IO L0P_11
SM15_R_N	L22	IO L10N_CC_SM15N_11
SM15_R_P	L23	IO L10P_CC_SM15P_11
SM14_R_N	N21	IO L11N_CC_SM14N_11
SM14_R_P	M21	IO L11P_CC_SM14P_11
DUT A D115	J24	IO L12N_VRP_11
DUT A D113	H24	IO L12P_VRN_11
DUT A D111	J26	IO L13N_11
DUT A D109	J25	IO L13P_11
DUT A D107	L25	IO L14N_VREF_11
DUT A D105	K26	IO L14P_11
SM13_R_N	K25	IO L15N_SM13N_11
SM13_R_P	L24	IO L15P_SM13P_11
SM12_R_N	M26	IO L16N_SM12N_11
SM12_R_P	N26	IO L16P_SM12P_11
SM11_R_N	M24	IO L17N_SM11N_11
SM11_R_P	M25	IO L17P_SM11P_11
SM10_R_N	N23	IO L18N_SM10N_11
SM10_R_P	N24	IO L18P_SM10P_11
SM9_R_N	M22	IO L19N_SM9N_11
SM9_R_P	N22	IO L19P_SM9P_11
DUT A D83	G26	IO L1N_11
DUT A D81	F25	IO L1P_11
DUT A D79	G25	IO L2N_11
DUT A D77	H26	IO L2P_11
DUT A D75	G24	IO L3N_11
DUT A D73	F24	IO L3P_11
DUT A D126	VREF	IO L4N_VREF_11
DUT A D69	E23	IO L4P_11
DUT A D67	F22	IO L5N_11
DUT A D65	F23	IO L5P_11
DUT A D63	H22	IO L6N_11
DUT A D61	G22	IO L6P_11
DUT A D59	J23	IO L7N_11
DUT A D57	H23	IO L7P_11
DUT A D55	K21	IO L8N_CC_11
DUT A D53	J21	IO L8P_CC_11
DUT A D51	K23	IO L9N_CC_11
DUT A D49	K22	IO L9P_CC_11

**FF665 BANK11**

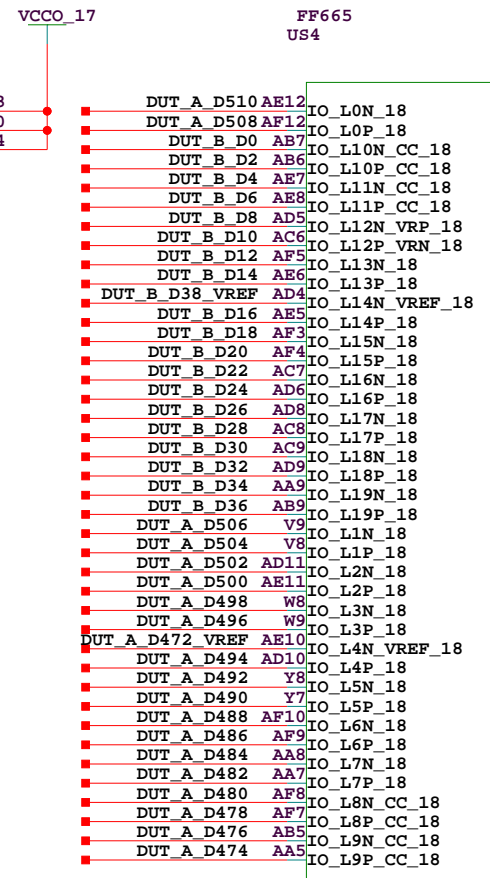
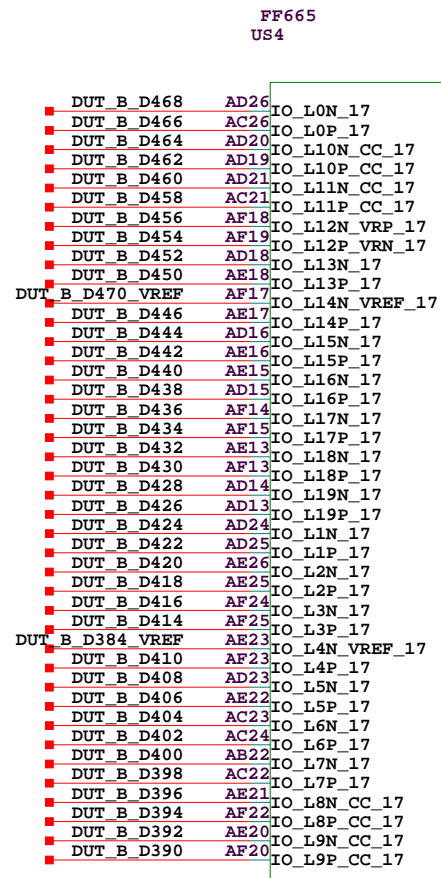
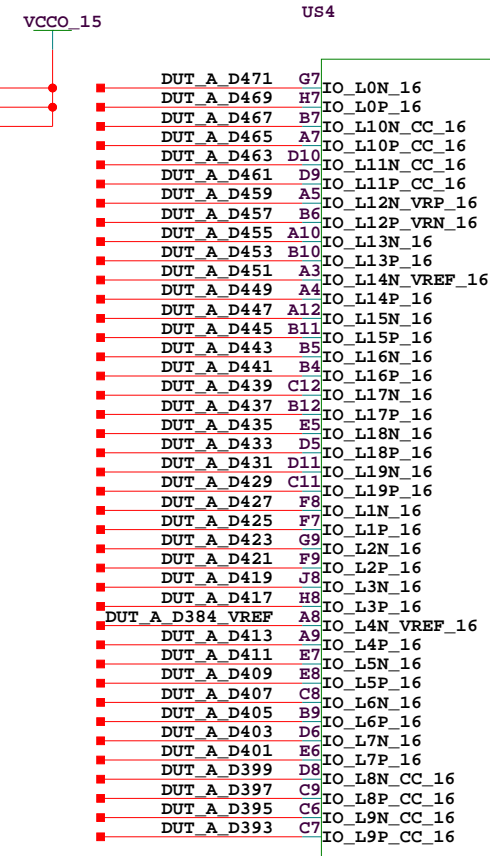
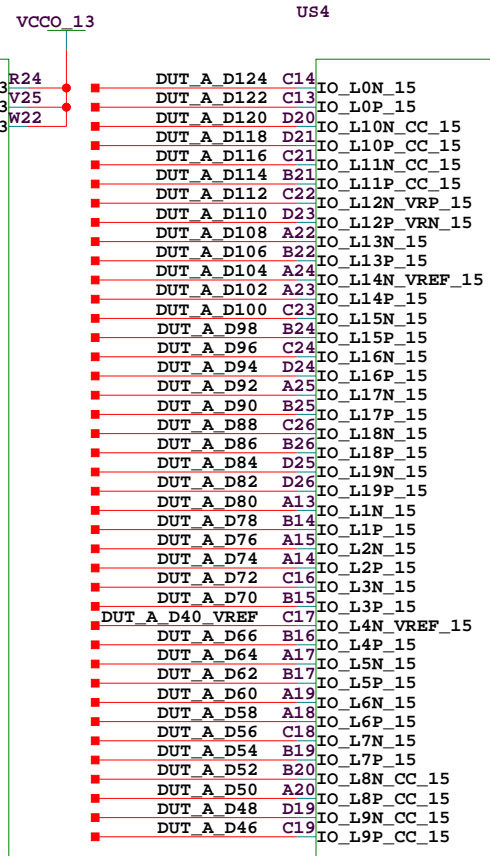
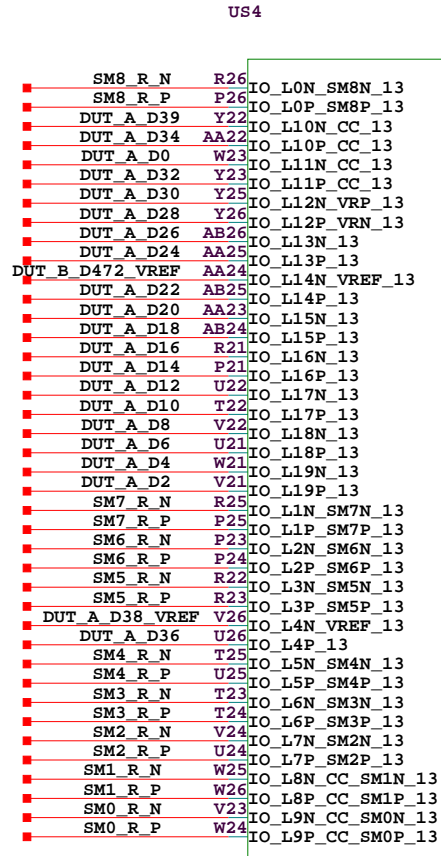
US4


DUT A D468	Y5	IO L0N_12
DUT A D466	Y6	IO L0P_12
DUT A D464	K7	IO L10N_CC_12
DUT A D462	K6	IO L10P_CC_12
FLASH_CLK_TMP	U5	IO L11N_CC_12
DUT A D458	U6	IO L11P_CC_12
DUT A D456	L7	IO L12N_VRP_12
DUT A D454	K8	IO L12P_VRN_12
DUT A D452	R5	IO L13N_12
DUT A D450	T5	IO L13P_12
DUT A D448	L8	IO L14N_VREF_12
DUT A D446	M7	IO L14P_12
DUT A D444	T7	IO L15N_12
DUT A D442	R6	IO L15P_12
DUT A D440	N6	IO L16N_12
DUT A D438	P6	IO L16P_12
DUT A D436	N7	IO L17N_12
DUT A D434	M6	IO L17P_12
DUT A D432	P8	IO L18N_12
DUT A D430	N8	IO L18P_12
DUT A D428	R7	IO L19N_12
DUT A D426	R8	IO L19P_12
DUT A D424	H6	IO L1N_12
DUT A D422	G6	IO L1P_12
DUT A D420	W4	IO L2N_12
DUT A D418	Y4	IO L2P_12
DUT A D416	F5	IO L3N_12
DUT A D414	G5	IO L3P_12
DUT A D470	VREF	IO L4N_VREF_12
DUT A D410	W5	IO L4P_12
DUT A D408	H4	IO L5N_12
DUT A D406	G4	IO L5P_12
DUT A D404	V7	IO L6N_12
DUT A D402	V6	IO L6P_12
DUT A D400	J6	IO L7N_12
DUT A D398	J5	IO L7P_12
DUT A D396	T8	IO L8N_CC_12
DUT A D394	U7	IO L8P_CC_12
DUT A D392	L5	IO L9N_CC_12
DUT A D390	K5	IO L9P_CC_12

**FF665 BANK12**

**TEST SOCKET**

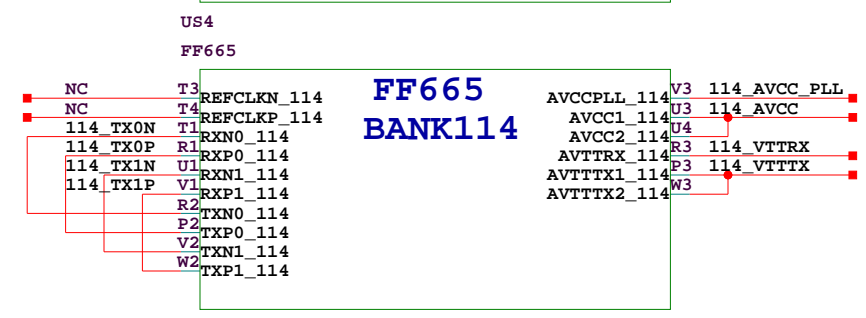
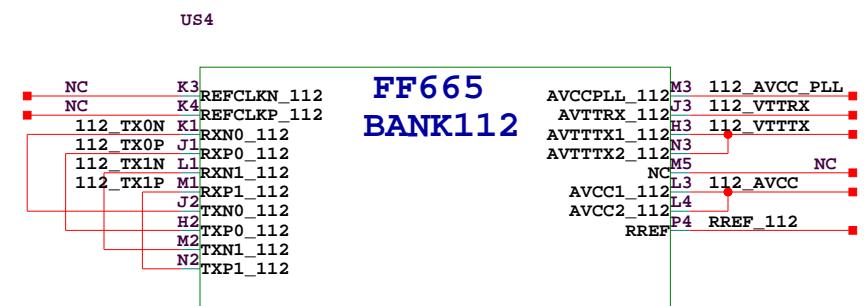
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		ART P/N	0531592
		FAB P/N	1280404
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Date:	2-19-2008_12:13	Ver:	C
Sheet Size:	B	Rev:	02
Sheet	17 of 21	Drawn By	s.s.



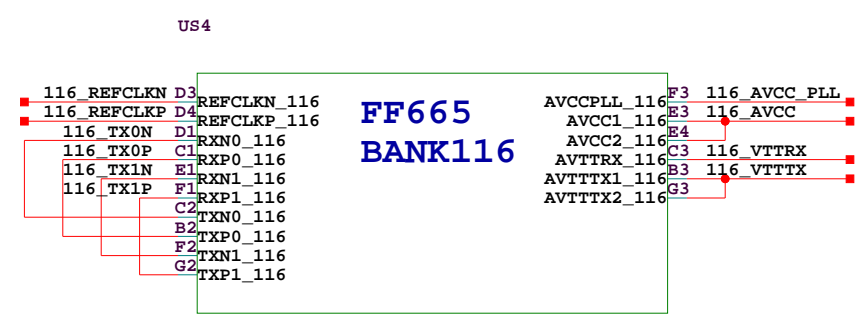
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<b>Date:</b> 2-19-2008_12:13		<b>Ver:</b> C	
<b>Sheet Size:</b> B		<b>Rev:</b> 02	
<b>Sheet</b> 18	<b>of</b> 21	<b>Drawn By</b>	s.s.

**TEST SOCKET**

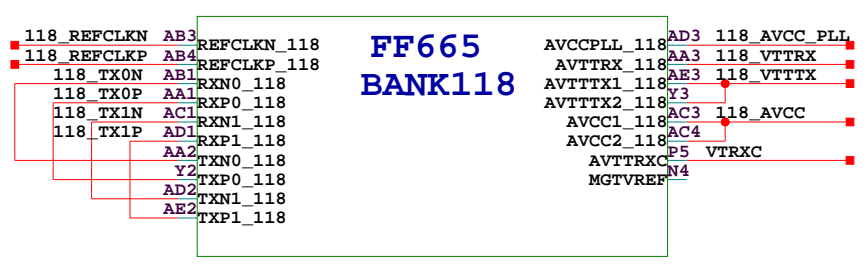




FF665



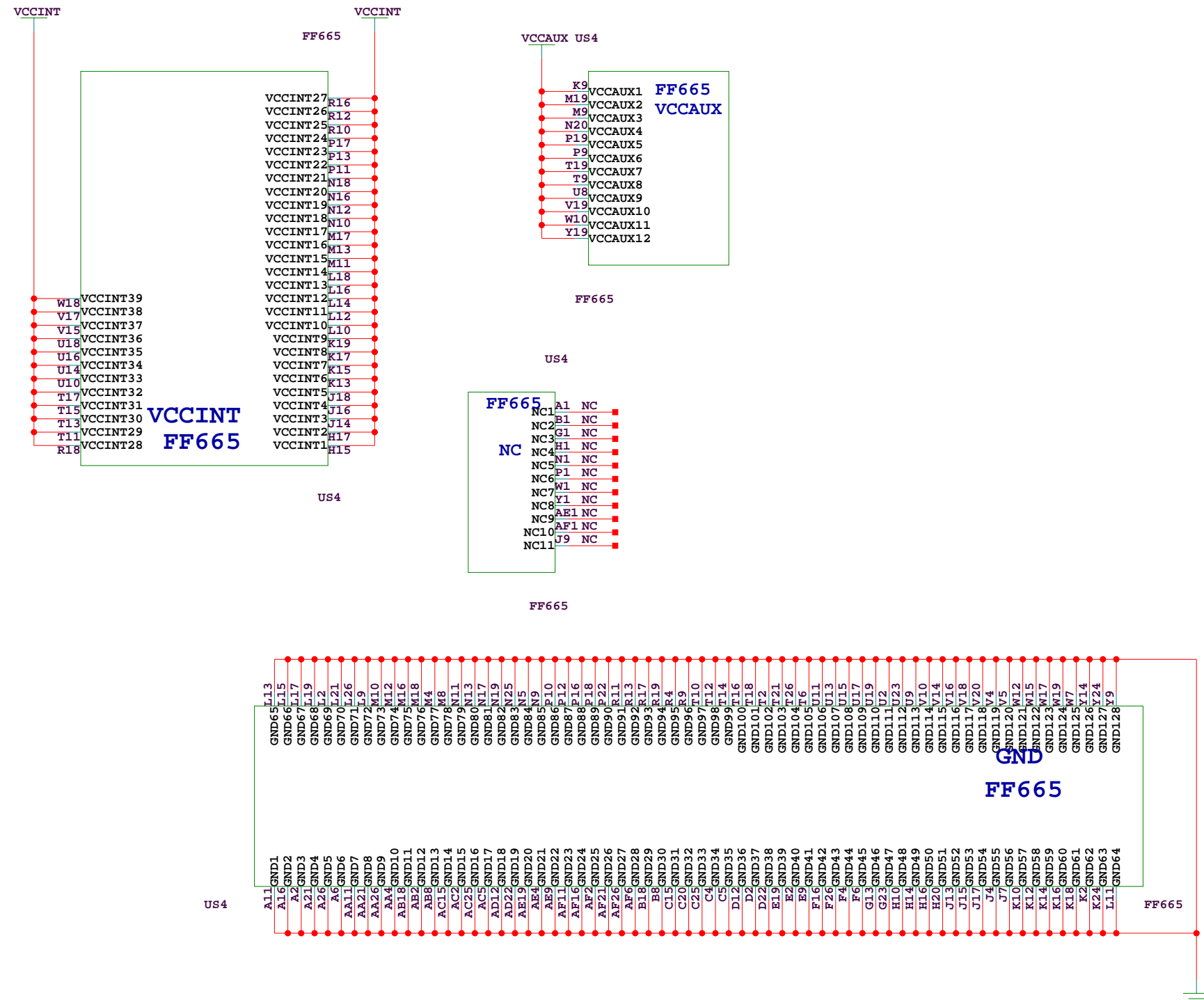
FF665  
US4




FF665

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		ART P/N	0531592
		FAB P/N	1280404
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Date:	2-19-2008_12:13	Ver:	C
Sheet Size:	B	Rev:	02
Sheet	19 of 21	Drawn By	s.s.

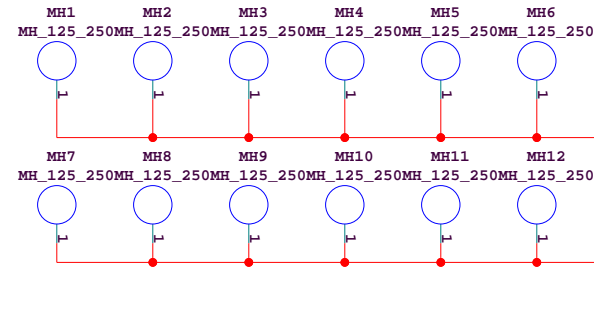
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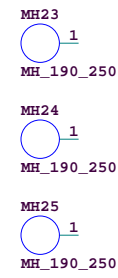
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Date: 2-19-2008_12:13		Ver: C	
Sheet Size: B		Rev: 02	
Sheet 20	of 21	Drawn By	s.s.

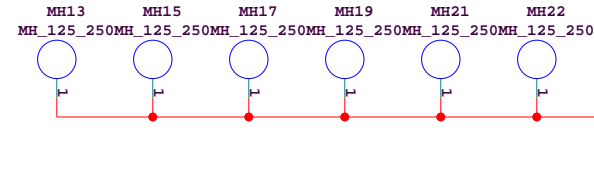
**AFXII MOUNTING HOLES**



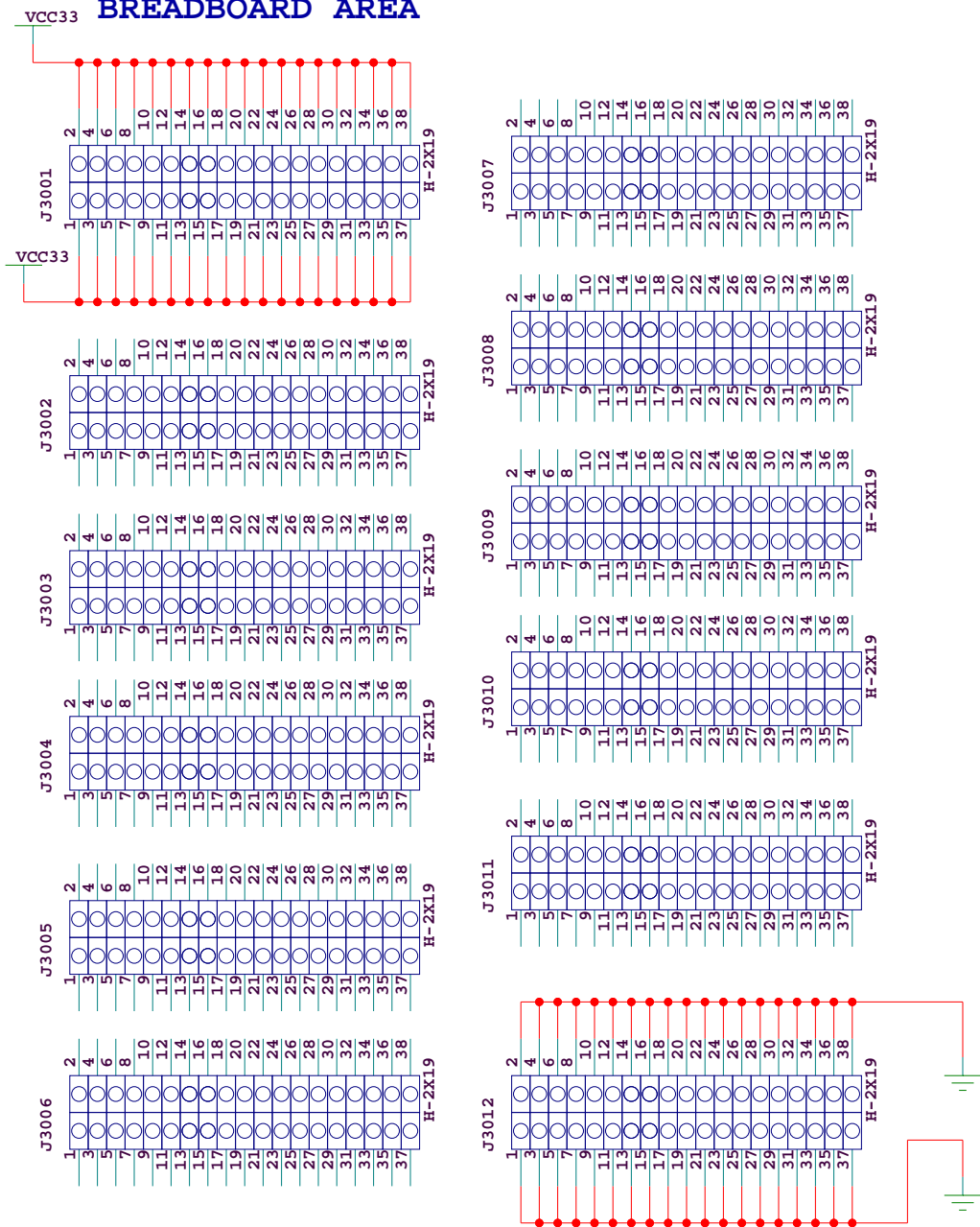
**AFXII GUIDE HOLES**



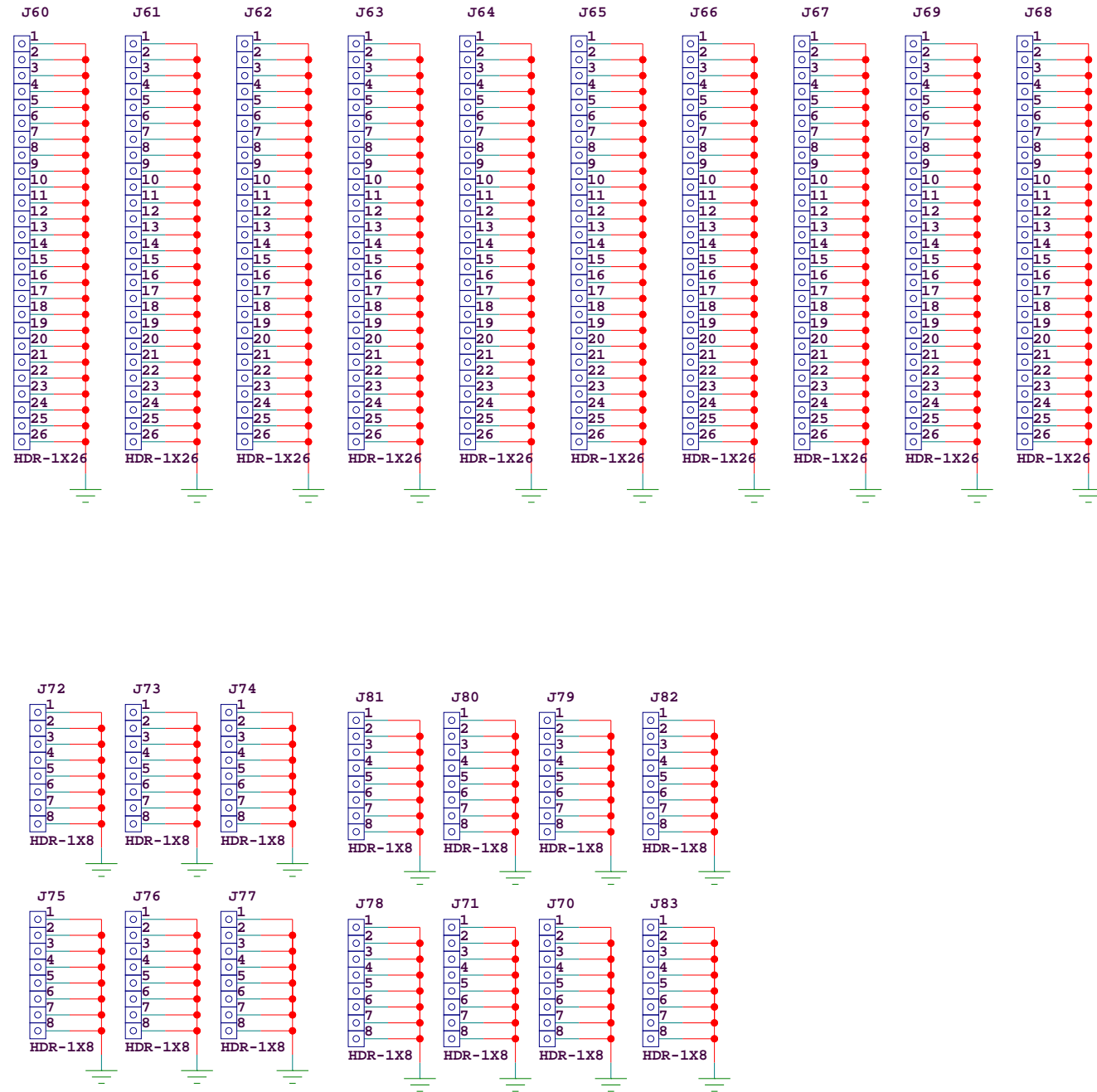
**MOUNTING HOLES**



**BREADBOARD AREA**



**DUT INTERLEAVE GND'S**



SCH P/N 0381233  
 ART P/N 0531592  
 FAB P/N 1280404

Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF665 DAUGHTER, 1280404  
**HARDWARE AND BREADBOARD AREA**

Date: 2-19-2008_12:13	Ver: C
Sheet Size: B	Rev: 02
Sheet 21 of 21	Drawn By s.s.