Alveo U200 and U250 Data Center Accelerator Cards

User Guide

UG1289 (v1.0) February 15, 2019

XILINX

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
02/15/2019 Version 1.0	
Initial release.	N/A

XILINX®

Table of Contents

Appendix C: Additional Resources and Legal Notices

Introduction

Overview

IMPORTANT: *Except where noted, this user guide applies to both the U200 and U250 cards.*

The Xilinx® Alveo™ U200 and U250 Data Center accelerator cards are peripheral component interconnect express (PCIe®) Gen3 x16 compliant cards featuring the Xilinx Virtex® UltraScale+™ technology. These cards accelerate compute-intensive applications such as machine learning, data analytics, video processing, and more. The Alveo U200 and U250 Data Center accelerator cards are available in passive and active cooling configurations. Figure 1-1 shows a passively cooled Alveo U200 accelerator card.

Figure 1-1: **Alveo U200 Data Center Accelerator Card (Passive Cooling)**

CAUTION! *The Alveo U200 and U250 accelerator cards with passive cooling are designed to be installed into a data center server, where controlled air flow provides direct cooling. Due to the card enclosure, switches are not accessible and LEDs are not visible (except for the triple-LED module DS3 that protrudes through the left front end PCIe bracket). The card details in this user guide are provided to aid understanding of the card features. If the cooling enclosure is removed from the card and the card is powered-up, external fan cooling airflow MUST be applied to prevent over-temperature shut-down and possible damage to the card electronics. Removing the cooling enclosure voids the board warranty.*

See Appendix C, Additional Resources and Legal Notices for references to documents, files, and resources relevant to the Alveo U200 and U250 accelerator cards.

Block Diagram

The block diagram of the Alveo U200 and U250 accelerator cards is shown in Figure 1-2.

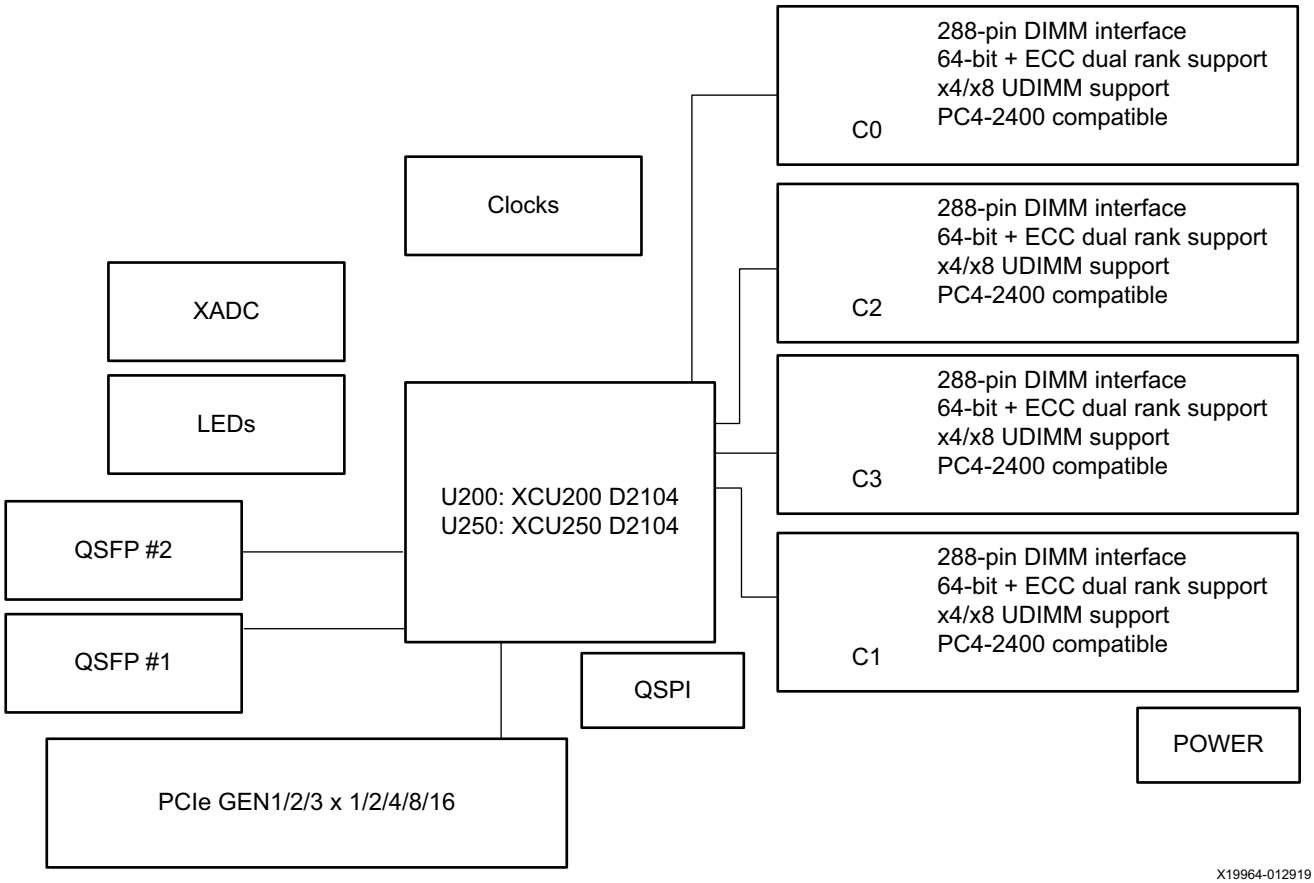


Figure 1-2: **Card Block Diagram**

Card Features

The Alveo U200 and U250 accelerator card features are listed in this section. Detailed information for each feature is provided in Feature Descriptions in Chapter 3.

- Alveo U200 accelerator card:
  - Virtex UltraScale+ XCU200-2FSGD2104E FPGA
- Alveo U250 accelerator card:
  - Virtex UltraScale+ XCU250-2LFIGD2104E FPGA
- Memory (four independent dual-rank DDR4 interfaces)
  - 64 gigabyte (GB) DDR4 memory
  - 4x DDR4 16 GB, 2400 mega-transfers per second (MT/s), 64-bit with error correcting code (ECC) DIMM
  - x4/x8 unregistered dual inline memory module (UDIMM) support
- Configuration options
  - 1 gigabit (Gb) Quad Serial Peripheral Interface (SPI) flash memory
  - Micro-AB universal serial bus (USB) JTAG configuration port
- 16-lane PCI Express
- Two QSFP28 connectors 100G interfaces
- USB-to-UART FT4232HQ bridge with Micro-AB USB connector
- PCIe integrated Endpoint block connectivity
  - Gen1, 2 or 3 x1/x2/x4/x8/x16
- I2C bus
- Status LEDs
- Power management with system management bus (SMBus) voltage, current, and temperature monitoring
- Dynamic power sourcing based on external power supplied
- 75W PCIe slot functional with 35 A max V_{CCINT} current PCIe slot power only
- 150 W PCIe slot functional with 110 A max V_{CCINT} current PCIe slot power and 6-pin PCIe Aux power cable connected
- 225 W PCIe slot functional with 160 A max V_{CCINT} current PCIe slot power and 8-pin PCIe Aux power cable connected
- Onboard reprogrammable flash configuration memory

- Front panel JTAG and universal asynchronous receiver-transmitter (UART) access through the USB port
- FPGA configurable over USB/JTAG and Quad SPI configuration flash memory

Card Specifications

Dimensions

Height: 4.376 inch (11.115 cm)

PCB thickness (±5%): 0.062 inch (0.157 cm)

Card length, passive heat sink: 9.2 inch (23.4 cm)

Card thickness with heat sink enclosure installed:

Passive: 1.44 inch (3.66 cm)

Note: A 3D model of this card is not available.

Environmental

Temperature

Operating: 0°C to +45°C

Storage: –25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

PCIe slot +12 V_{DC}, +3.3 V_{DC}, +3.3 V_{AUXDC}, External +12 V_{DC}

Design Flows

The preferred optimal design flow for targeting the Alveo Data Center accelerator card uses SDAccel. However, long-time FPGA designers might want to use traditional design flows, such as RTL or HLx. While these are not optimized design flows for the Alveo accelerator card, Xilinx offers limited support for using the Vivado® tools with RTL or HLx. Figure 1-3 shows a summary of the design flows.

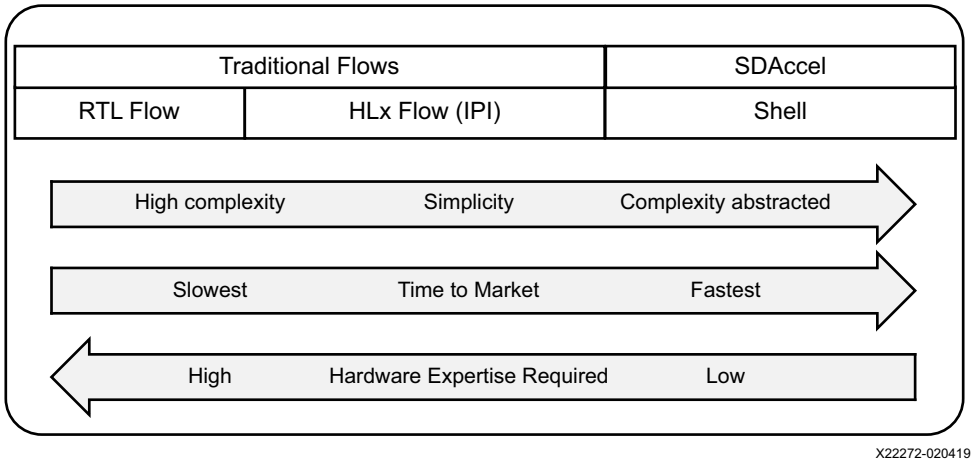


Figure 1-3: **Alveo Data Center Accelerator Card Design Flows**

Each design flow has different requirements as listed in Table 1-1.

Table 1-1: **Requirements to Get Started with Alveo Data Center Accelerator Card Design Flows**

	RTL Flow	HLx Flow	SDAccel
Flow documentation	UG949(1)	UG895(2)	UG1301(3)
Hardware documentation	UG1289	UG1289	N/A
Vivado tools support	Board support XDC	Board support XDC	N/A

Notes:

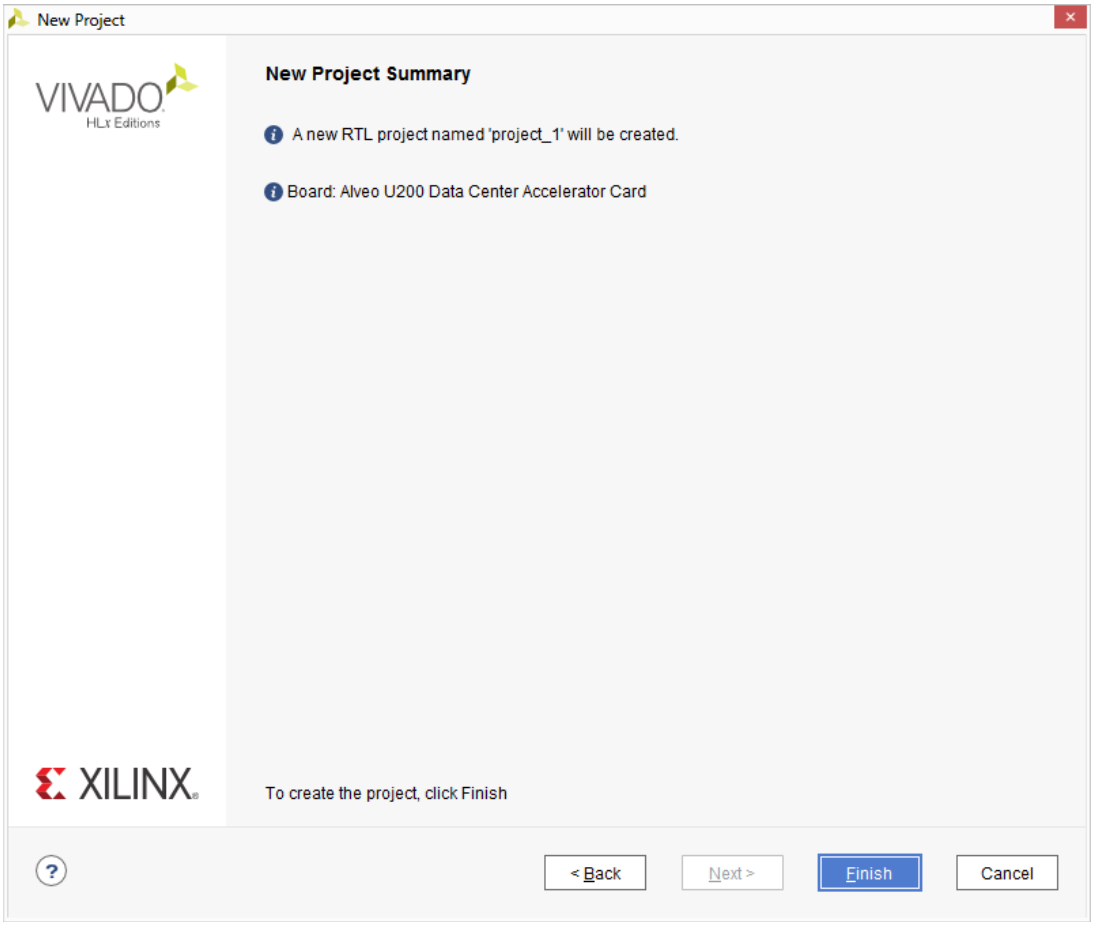
1. *UltraFast Design Methodology Guide for the Vivado Design Suite* (UG949) [Ref 1].
2. *Vivado Design Suite User Guide: System-Level Design Entry* (UG895) [Ref 2]. See "Using the Vivado Design Suite Platform Board Flow" in Chapter 2 and Appendix A.
3. *Getting Started with Alveo Data Center Accelerator Cards* (UG1301) [Ref 3].

This user guide provides a starting point for expert HDL developers using the RTL flows or for developers who want to customize in HLx beyond the standard support in the Vivado tools. For either the RTL or HLx flow, designers can start by targeting the Alveo Data Center accelerator card in the Vivado tools. In the Vivado Design Suite, select **Create New Project** > **RTL Project**, and then select the Alveo Data Center accelerator U200 card as shown in Figure 1-4.

X22260-012919

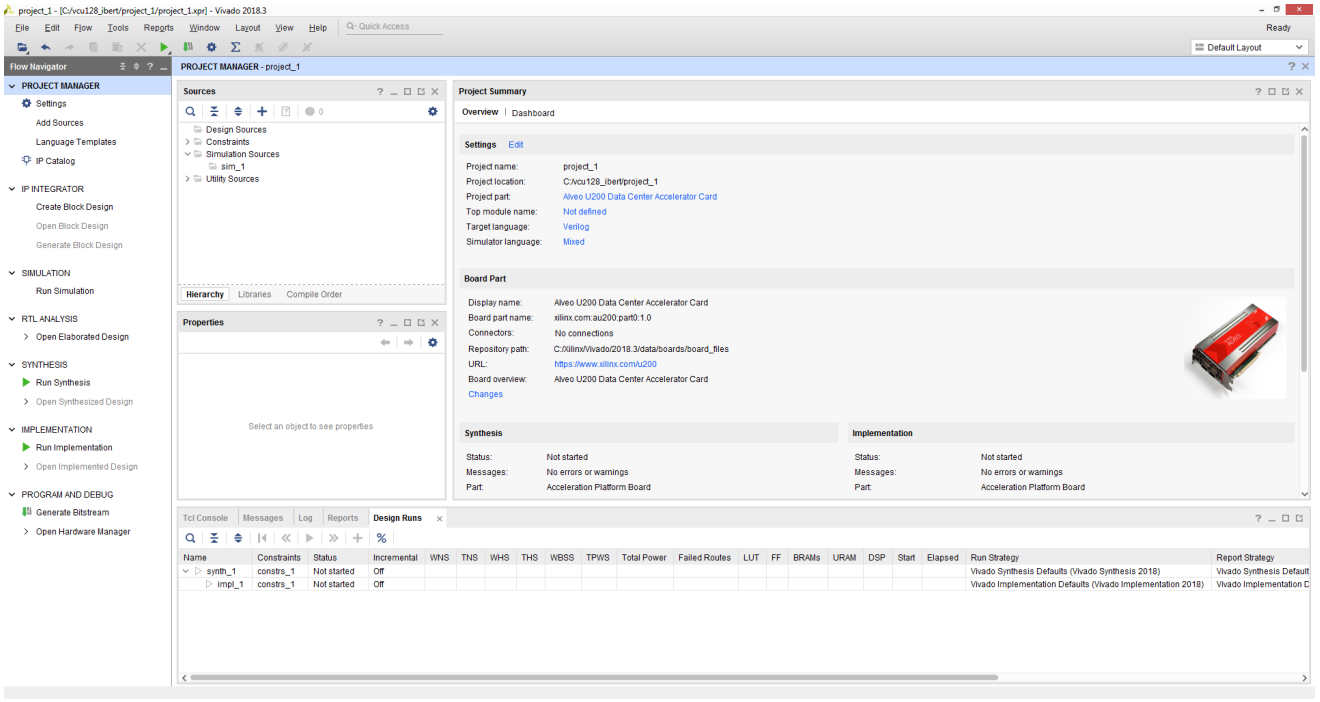
Figure 1-4: **Selecting Alveo Data Center Accelerator U200 Card in Vivado Design Suite**

When using the RTL flow, after you have selected the Alveo Data Center accelerator card from the Boards tab, Figure 1-5 appears followed by Figure 1-6. The RTL-based project can now be created.



X22261-012519

Figure 1-5: **Alveo Data Center Accelerator U200 Card New Project Summary**



X22262-012519

Figure 1-6: **Alveo Data Center Accelerator U200 Card New Project Summary**

Creating an MCS file (PROM Image)

This section outlines the Alveo Data Center accelerator card custom flow, including:

- Bitstream constraints and generating a PROM file
- Flash programming through the USB-JTAG (Micro USB) interface

To create an MCS file (PROM image) for the Alveo accelerator card, a bitstream (.bit) file must first be created with the proper settings. For reference, the bitstream configuration constraints are listed at the end of this section.

The Alveo accelerator card contains a Quad SPI configuration flash memory part that can be configured over USB-JTAG. This part contains a protected region, with the factory base image at the 0x00000000 address space. This base image points to the customer programmable region at a 0x01002000 address space offset.

To ensure that the customer image is successfully loaded onto the Alveo accelerator card at run time, these settings must be used to create the MCS file:

- Memory part: mt25qu01g-spi-x1_x2_x4
- Start address: 0x01002000

```
# Bitstream Configuration
# ------------------------------------------------------------------------
set_property CONFIG_VOLTAGE 1.8                          [current_design]
set_property BITSTREAM.CONFIG.CONFIGFALLBACK Enable      [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE             [current_design]
set_property CONFIG_MODE SPIx4                           [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4             [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 85.0            [current_design]
set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN disable [current_design]
set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES          [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN Pullup           [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR Yes         [current_design]
# ------------------------------------------------------------------------
```

After the MCS file is created, see the procedure in the "Programming the FPGA Device" chapter in the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 5] to connect to the Alveo Data Center accelerator card using the hardware manager.

1. Select Add Configuration Device and select the mt25qu01g-spi-x1_x2_x4 part.
2. Select Program the Configuration Memory Device on the target.
   a. Select the MCS file target.
   b. Select the Address Range of Configuration File Only.
   c. Select OK.
3. After this operation has completed, disconnect the card in the hardware manager, and disconnect the USB cable from the Alveo accelerator card.
4. Perform a cold reboot on the host machine.

Card Setup and Configuration

Electrostatic Discharge Caution

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.
- If you are returning the adapter to Xilinx® Product Support, place it back in its antistatic bag immediately.

Installing Alveo Data Center Accelerator Cards in Server Chassis

Because each server or PC vendors hardware is different, for physical board installation guidance, see the manufacturer's PCIe® board installation instructions.

For programming and start-up details, see *Getting Started with Alveo Data Center Accelerator Cards* (UG1301) [Ref 3].

FPGA Configuration

The Alveo™ U200 and U250 accelerator cards support two UltraScale+™ FPGA configuration modes:

- Quad SPI flash memory
- JTAG using USB JTAG configuration port (USB J13/FT4232H U27)

The FPGA bank 0 mode pins are hardwired to M[2:0] = **001** master SPI mode with pull-up/down resistors.

At power up, the FPGA is configured by the Quad SPI NOR flash device (Micron MT25QU01GBBA8E12-0SIT) with the FPGA_CCLK operating at clock rate of 105 MHz (EMCCLK) using the master serial configuration mode. The Quad SPI flash memory NOR device has a capacity of 1 Gb.

While the FPGA default mode selects Quad SPI configuration, JTAG mode overrides it if invoked. JTAG mode is always available independent of the mode pin settings.

For complete details on configuring the FPGA, see the *UltraScale Architecture Configuration User Guide* (UG570) [Ref 4].

Table 2-1: **Configuration Modes**

Configuration Mode	M[2:0]	Bus Width	CCLKL Direction
Master SPI	001	x1, x2, x4	FPGA output
JTAG	Not applicable – JTAG overrides	x1	Not applicable

Card Component Descriptions

Overview

This chapter provides a functional description of the Alveo™ U200 and U250 Data Center accelerator card features.

Feature Descriptions

Virtex UltraScale+ FPGA

The Alveo U200 accelerator card is populated with the Virtex® UltraScale+™ XCU200-L2FSGD2104E FPGA. The Alveo U250 accelerator card is populated with the Virtex UltraScale+ XCU250-L2FIGD2104E FPGA. For more information on Virtex UltraScale+ FPGAs, see *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923) [Ref 6].

DDR4 DIMM Memory

Four independent dual-rank DDR4 interfaces are available. The card is populated with four socketed single-rank Micron MTA18ASF2G72PZ-2G3B1IG 16GB DDR4 RDIMMs. Each DDR4 DIMM is 72-bits wide (64-bits plus support for ECC).

The detailed FPGA connections for the feature described in this section are documented in the Alveo U200 or U250 accelerator card XDC file, referenced in Appendix A, Xilinx Constraints File.

For more details about the Micron DDR4 DIMM, see the Micron MTA18ASF2G72PZ-2G3B1IG data sheet at the Micron website [Ref 11].

Quad SPI Flash Memory

The Quad SPI device provides 1 Gb of nonvolatile storage.

- Part number: MT25QU01GBB8E12-0SIT (Micron)
- Supply voltage: 1.8V
- Datapath width: four bits
- Data rate: variable

For more flash memory details, see the Micron MT25QU01GBB8E12-0SIT data sheet at the Micron website [Ref 11].

For configuration details, see the *UltraScale Architecture Configuration User Guide* (UG570) [Ref 4]. The detailed FPGA connections for the feature described in this section are documented in the Alveo U200 or U250 accelerator card XDC file, referenced in Appendix A, Xilinx Constraints File.

USB JTAG Interface

The Alveo U200 and U250 accelerator cards provide access to the FPGA device via the JTAG interface.

FPGA device configuration is available through the Vivado® hardware manager, which accesses the onboard USB-to-JTAG FT4232HQ bridge device. The micro-AB USB connector on the Alveo U200 accelerator card PCIe® panel/bracket provides external device programming access.

Note: JTAG configuration is allowed at any time regardless of the FPGA mode pin settings consistent with the *UltraScale Architecture Configuration User Guide* (UG570) [Ref 4].

For more details about the FT4232HQ device, see the FTDI website [Ref 12].

FT4232HQ USB-UART Interface

The FT4232HQ Quad USB-UART provides a UART connection through the micro-AB USB connector. The FPGA UART TX/RX (two-wire) connection is made through the FT4232HQ BD port. Channel BD implements a 2-wire level-shifted TX/RX UART connection to the FPGA. The FTDI FT4232HQ data sheet is available on the FTDI website [Ref 12].

PCI Express Endpoint

The Alveo U200 and U250 accelerator cards implement a 16-lane PCI Express® edge connector that performs data transfers at the rate of 2.5 giga-transfers per second (GT/s) for Gen1, 5.0 GT/s for Gen2, and 8.0 GT/s for Gen3 applications. The -2 speed grade FPGA included with the cards supports up to Gen3 x16.

The detailed FPGA connections for the feature described in this section are documented in the Alveo U200 or U250 accelerator card XDC file, referenced in Appendix A, Xilinx Constraints File.

QSFP28 Module Connectors

The Alveo accelerator cards host two 4-lane small form-factor pluggable (QSFP) connectors that accept an array of optical modules. Each connector is housed within a single QSFP cage assembly.

The QSFP+ connectors are accessible via the I2C interface on the Alveo U200 and U250 accelerator cards. The QSFP connector's sideband signals are accessible directly from the FPGA. The MODSELL, RESETL, MODPRSL, INTL, and LPMODE sideband signals are defined in the small form factor (SFF) specifications listed below. The components visible through the card PCIe panel/bracket top to bottom are:

- Triple status LEDs
- QSFP0
- QSFP1
- USB

For additional information about the quad SFF pluggable (28 Gb/s QSFP+) module, see the SFF-8663 and SFF-8679 specifications for the 28 Gb/s QSFP+ at the SNIA Technology Affiliates website [Ref 13].

Each QSFP connector has its own clock generator.

- QSFP0 clock
  - Clock generator: Silicon Labs SI5335A-B06201-GM
  - Output CLK1A/1B: the QSFP0_CLOCK_P/N clock is an AC-coupled LVDS 156.25 MHz clock wired to the QSFP0 GTY interface
- QSFP1 clock
  - Clock generator: Silicon Labs SI5335A-B06201-GM
  - Output CLK1A/1B: the QSFP1_CLOCK_P/N clock is an AC-coupled LVDS 156.25 MHz clock wired to the QSFP1 GTY interface

The detailed FPGA connections for the feature described in this section are documented in the Alveo U200 or U250 accelerator card XDC file, referenced in Appendix A, Xilinx Constraints File.

I2C Bus

The Alveo U200 and U250 accelerator cards implement an I2C bus network (the device tree details are available in the board support package).

Status LEDs

The card is designed to operate with the passive heat sink enclosure cover installed so the DS1 and DS2 LEDs are not visible. Status light emitting diodes (LED) DS3, DS4, and DS5 are visible through a cut out in the PCIe end bracket. Table 3-1 defines the card status LEDs.

Table 3-1: **Card Status LEDs**

Reference Designator	Description
DS1	RED: POWER_GOOD
DS2	BLUE: DONE_0
DS3	ORANGE: STATUS_LED0
DS4	YELLOW: STATUS_LED1
DS5	GREEN: STATUS_LED2

Card Power System

Limited power system telemetry is available via the I2C IP that is instantiated during the FPGA design process that starts after the Alveo Data Center accelerator card is selected from the Vivado Design Suite Boards tab as described in Design Flows.

Appendix A

Xilinx Constraints File

Overview

RTL users can reference the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 8] for more information. The Alveo™ U200 and U250 accelerator card XDC files are available for download from their respective websites along with this user guide.

XILINX

Appendix B

Regulatory and Compliance Information

Overview

This product is designed and tested to conform to the European Union directives and standards described in this section.

Alveo™ Data Center Accelerator Card — Master Answer Record 71752

For Technical Support, open a Support Service Request.

CE Directives

2014/35/EC, *Low Voltage Directive (LVD)*

2014/30/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN:55032:2015, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN:55024:2015, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

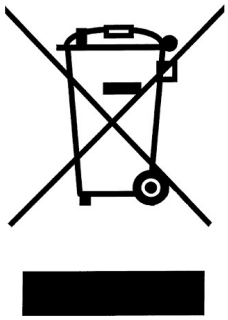
This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

IEC 60950-1, 2nd Edition, 2014, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1, 2nd Edition, 2014, *Information technology equipment – Safety, Part 1: General requirements*

Markings



In August of 2005, the European Union (EU) implemented the EU Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU. These directives require Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Appendix C

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter **`docnav`**.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

The most up to date information related to the U200 and U250 cards and documentation is available on the following websites.

Alveo U200 Data Center Accelerator Card

Alveo U250 Data Center Accelerator Card

Master Answer Record 71752

These Xilinx documents provide supplemental material useful with this guide:

1. *UltraFast Design Methodology Guide for the Vivado Design Suite* (UG949)
2. *Vivado Design Suite User Guide: System-Level Design Entry* (UG895)
3. *Getting Started with Alveo Data Center Accelerator Cards* (UG1301)
4. *UltraScale Architecture Configuration User Guide* (UG570)
5. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
6. *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923)
7. *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide* (PG150)
8. *Vivado Design Suite User Guide: Using Constraints* (UG903)
9. *UltraScale Architecture PCB Design User Guide* (UG583)

For additional documents associated with Xilinx devices, design tools, intellectual property, cards, and kits see the Xilinx documentation website.

The following websites provide supplemental material useful with this guide:

10. Xilinx, Inc: www.xilinx.com
    (XCU200-L2FSGD2104E)
11. Micron Technology: www.micron.com
    (MTA18ASF2G72PZ-2G3B1IG, MT25QU01GBB8E12-0SIT)
12. Future Technology Devices International Ltd.: www.ftdichip.com
    (FT4232HQ)
13. SFF-8663, SFF-8679 specification: SNIA Technology Affiliates

Please Read: Important Legal Notices

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at https://www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at https://www.xilinx.com/legal.htm#tos.

AUTOMOTIVE APPLICATIONS DISCLAIMER

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.