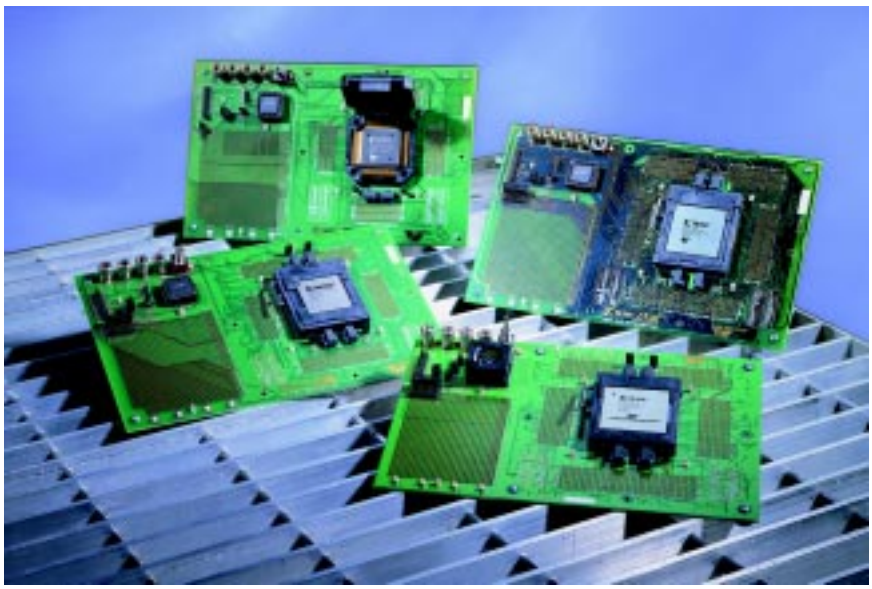
Xilinx Prototype Platforms User Guide for Virtex and Virtex-E Series FPGAs

DS020 (v1.1) December 9, 1999



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CDROM Contents

The CDROM contains documentation for all Xilinx Prototype boards including the following:

- The User Guide in .pdf format.
- An example design "demo" that flashes the on-board LED. This design includes the Verilog source, demo.v, synthesized using FPGA Express.
- A .bit file and a .mcs file for each part type supported by the board.
- Full schematics of the board in both .pdf format and in ViewDraw schematic capture format.
- The PC board layout in Pads PCB format.
- The gerber files for the PC board (*.pho). There are many free or shareware gerber file viewers available on the web for viewing and printing these files.

Introduction

The traditional approach to experimenting with new devices involving wiring together some ICs on a breadboard is fast becoming impractical and ineffective. Instead, designers using new high-density devices need custom PC boards representing a substantial investment of time and money.

Prototype boards from device manufacturers can meet this demand for experimentation while eliminating the expense and time involved with custom PC boards. Additionally, such prototype boards facilitate the understanding and advantages of new device features.

The Xilinx Prototype board allows experimentation with Virtex™ devices prior to committing to using them for specific applications. It allows designers to try Virtex features such as block RAM, DLLs, and the SelectI/O™ resource, with an off-the-shelf resource. The Xilinx Prototype board also facilitates learning the entire design flow from schematic capture or HDL to programming and verification of designs.

The Xilinx Prototype board has the following features.

- Independently switched V_{CCINT} and V_{CCO} power supply jacks.
- Selectable V_{CCO} for each SelectI/O™ bank.
- Virtex configuration port for use with MultiLinx™ or Xchecker cable.
- Selectable mode pins.
- Every GCLK (Global CLocK) input has an available oscillator socket with enable pin.
- Power indicator LED.
- 44-pin, PLCC PROM socket for master serial configuration.
- JTAG port for reprogramming the XC1800 series re-configurable PROMs.

The kit contains headers that may be soldered on to the breakout area if desired.

The headers are useful with certain types of oscilloscope probes, connecting function generators, or when wiring pins to the prototype area.

Block Diagram

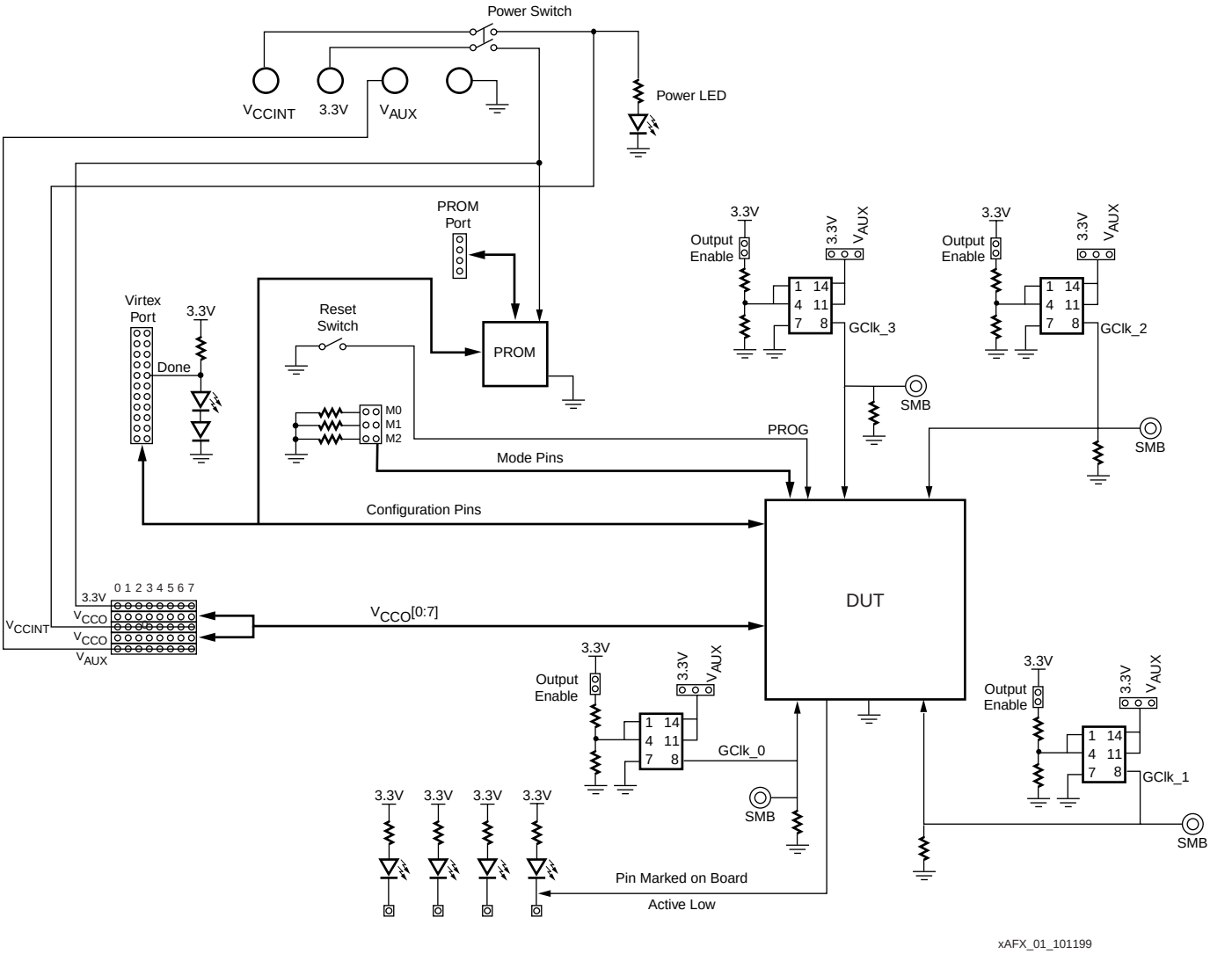

Figure 1: Block Diagram of Xilinx Prototype Board

Detailed Description

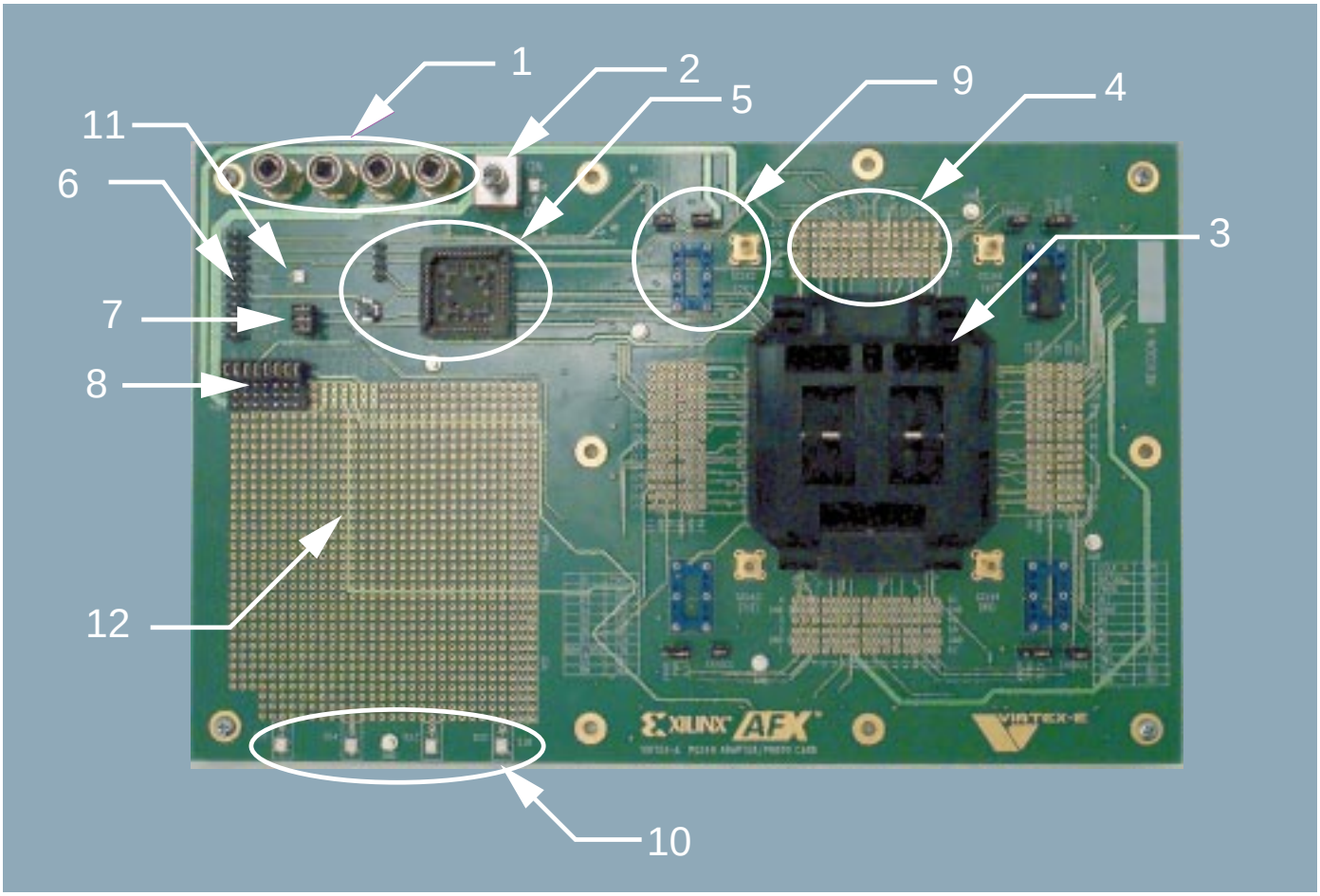

Figure 2: Detailed Description of Xilinx Prototype Board Components

1. Power Supply Jacks

The board has four power supply jacks labeled V_{CCINT}, 3.3V, V_{AUX}, and GND. The V_{CCINT} jack supplies the Virtex device core. Consult the Xilinx data book for maximum V_{CCINT} voltage for the device you are using. The 3.3V supply supplies power to the on-board configuration PROM, the four oscillators, and to all pins marked 3.3V including the Virtex Port, the prototyping area, and the V_{CCO} Supply Jumpers.

2. Power Switch

A power switch connects the V_{CCINT} and 3.3V supply jacks to the board. It does not switch V_{AUX} or GND. A green LED indicates power to the device core when V_{CCINT} is 2.0V or higher.

3. DUT Socket

Failure to properly orient the device using the Pin 1 indicator on the board when inserting may damage the device. To avoid pin damage, always use the vacuum tool provided when inserting or removing the Virtex device.

WARNING: WITH BGA PACKAGES, DO NOT APPLY PRESSURE TO THE DEVICE WHILE ACTIVATING THE VACUUM TOOL LEVER! Doing so may damage the socket and/or the device.

4. Pin Breakout

The pin breakout area is used to monitor or apply signals to each of the device pins. Each pin has an adjacent ground pin for ease of use.

5. PROM socket, PROM port, and Reset Switch

The SPROM socket may be used to configure the Virtex device in master serial mode. The socket accepts XC1700 and XC1800 series configuration PROMs in PC44 packages. The PROM port may be used to reprogram an XC1800 series PROM via JTAG. Depressing the reset switch causes the PROGRAM pin on the FPGA to short to ground reconfiguring the FPGA. The reset polarity low option must be selected when programming the configuration PROM.

6. Virtex Port

The Virtex Port is used to connect a MultiLinx or download cable to the board. This port supports all Virtex device configuration modes.

7. Mode Pin Jumpers

The M0, M1, and M2 jumpers short the mode pins to ground to select the configuration mode desired. The FPGA provides a weak pull-up on each mode pin that pulls the pin High when the jumper is removed.

8. V_{CCO} Supply Jumpers

Virtex series devices have eight SelectI/O banks, each with a V_{CCO} supply (only one for the PQ package). V_{CCO} supply jumpers connect each bank to one of the three on-board supplies: V_{CCINT}, 3.3V, or V_{AUX}. These jumpers must be installed for the Virtex device to function normally. Each bank, labeled 0 through 7 above the headers, can be connected to the 3.3V, V_{CCINT} or V_{AUX} supply.

9. GCLK Oscillators and Jumpers

The board has four crystal oscillator sockets, one for each GCLK. Some Xilinx Prototype boards accommodate both half-size and full-size oscillators; earlier versions only accommodate half-size oscillators. There are jumper sockets next to each oscillator marked "enable" to control the output enable pin on the oscillator. When the jumper is installed, the enable pin is pulled High. If not installed, the enable pin is Low.

Some prototype boards have jumper sockets to select oscillator supply, allowing the oscillator connection to be 3.3V or V_{AUX}. A jumper must be installed for the oscillator to function. Without this feature, the oscillator power is 3.3V.

Some boards have an SMB-type connector for each GCLK pin. With such boards, the kit contains a BNC to SMB 50 Ω cable. When the SMB connector is used, there is space for

user-installed termination resistors near the GCLK pins. For details about the termination resistors, please reference the schematics included on the accompanying CD.

10. User LEDs

There are four-user defined LEDs on the board. The LED in the bottom right portion of the prototyping area is a dedicated LED connected to a Virtex device pin. The pin number appears next to the LED. There is a test point associated with each LED. When this point is pulled Low, the LED turns on.

11. DONE LED

The LED located next to the Virtex port indicates the status of the DONE pin. This LED turns on when DONE is High and turns off when DONE is Low. If power is applied to the board without a part in the socket, the LED also turns on.

12. Prototyping Area

The prototyping area accommodates 0.10" spaced ICs. V_{CCINT}, 3.3V, and V_{AUX} power supplies are accessed through the centered headers available in the prototyping area.

Example Design

The CD-ROM includes an example design that can be downloaded to a Virtex device on the prototype board. This design causes the LED in the lower-right prototype area to flash.

Follow this procedure to download the demo design:

1. Place the power switch on the Xilinx Prototype board in the off position.

2. Connect one power supply to the V_{CCINT} jack and another power supply to the 3.3V jack. Set the V_{CCINT} supply to the recommended V_{CCINT} voltage for the Virtex part you are using. Set the 3.3V supply to 3.3V.

3. Connect a MultiLinx or X-Checker cable to the Virtex port on the Xilinx Prototype board. See Appendix A to determine the correct wire connections.

4. Insert the included oscillator in the GCLK0 oscillator socket, being careful to observe the pin 1 indicator on the oscillator and on the Xilinx Prototype board.

5. Insert a jumper on the Enable pin for GCLK0.

6. Using the supplied jumpers, connect each V_{CCO} bank to the 3.3V supply.

7. Install or remove the mode pin jumpers to select the proper configuration mode. See Appendix A for mode pins settings.

8. Turn on the board and download the bit stream. The bit stream is located on the CD in the file *board_part_num**designs**demo**vitex_part_num**demo_par.bit*.

Replace *board_part_num* with the board part number and *virtex_part_num* with the Virtex part number. The board part number is on the back of the board.

Download example: \hw-afx-pq240-100\designs\demo\xcv300\demo_par.bit

When the bit stream is downloaded correctly, the DONE indicator LED turns on and the LED in the prototype area flashes.

APPENDIX A MultiLinx™ Connections

The following tables show the cable connections between the MultiLinx cable and the Xilinx Prototype Board for each of the supported configuration modes. Also shown are the mode pin settings for the mode pins on the board. The mode pins are shown in the order of M2, M1, and M0. A '1' indicates the jumper is removed, a '0' indicates the jumper is installed.

Table 1: Slave Serial Mode; Mode Pins: 111 or 011

MultiLinx Cable	Prototype Board
PWR	3.3V
GND	GND
CCLK	CCLK
DONE	DONE
DIN	D0
PROG	PROG
INIT	INIT

Table 2: Select Map Mode; Mode Pins: 110 or 010

MultiLinx Cable	Prototype Board
PWR	3.3V
GND	GND
CCLK	CCLK
DONE	DONE
PROG	PROG
INIT	INIT
CS	CS
RS(RDWR)	RW
RDY/BUSY	DOUT/BUSY
DO	DO
D1	D1
D2	D2
D3	D3
D4	D4
D5	D5
D6	D6
D7	D7

Table 3: Boundary-scan Mode; Mode Pins: 101 or 001

MultiLinx Cable	Prototype Board
PWR	3.3V
GND	GND
CCLK	CCLK
DONE	DONE
DIN	D0
PROG	PROG
INIT	INIT

Master-serial Mode; Mode Pins: 000 or 100

The MultiLinx cable does not support master-serial mode. To configure in master-serial mode, install a pre-programmed Xilinx serial configuration PROM (XC1700 series) in the PC44 socket on the board.

Manufacturing Part Number:
0401852

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