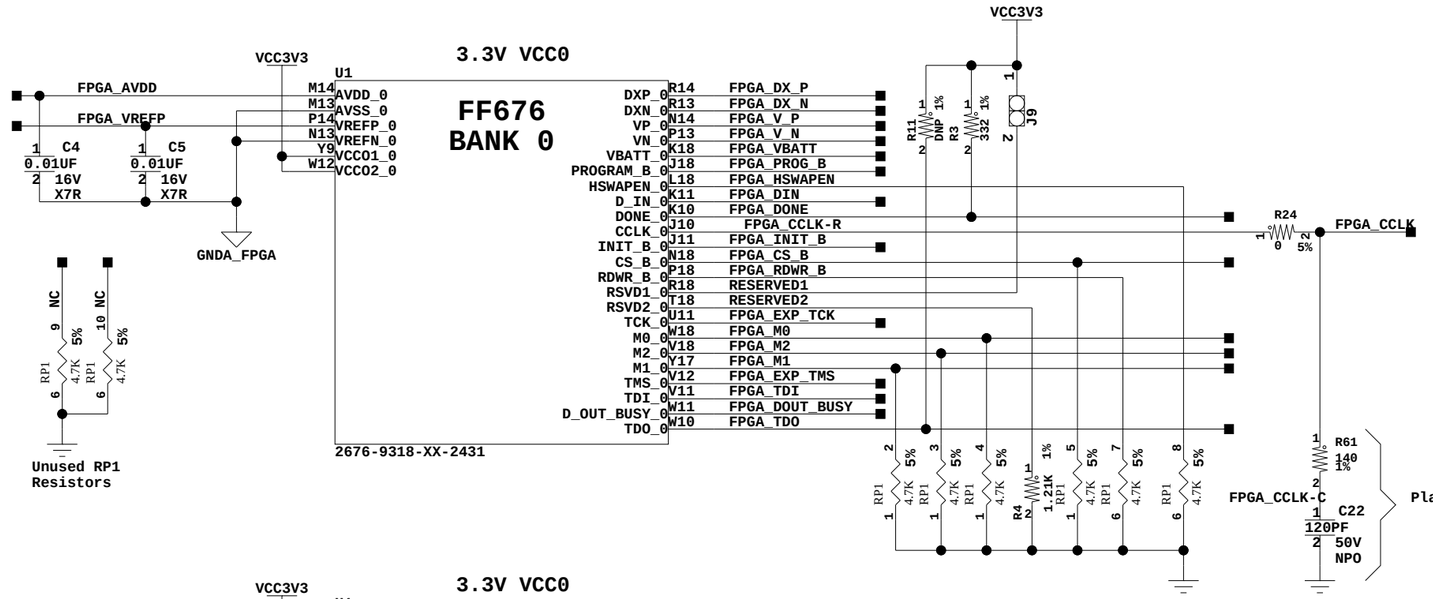
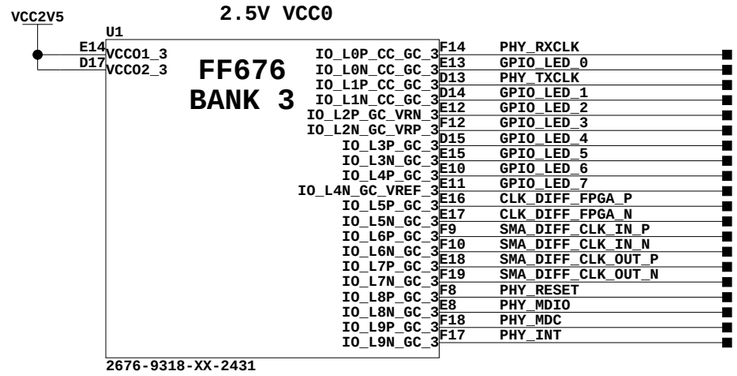
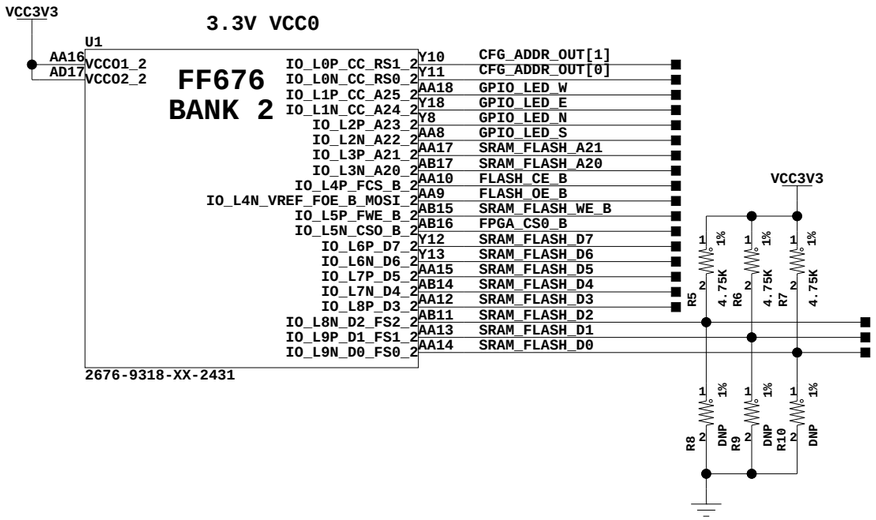
XILINX

Title:
SCHEM, ROHS COMPLIANT, ML501 VIRTEX-5 LX EVALUATION PLATFORM, 1280412
0381239

Date: 8-30-2006_16:33	Ver: 01
Sheet Size: B	Rev: B
Sheet 1 of 22	Drawn By BP







Banks 0,1,2,3,4 Config, FLASH, SRAM, GPIO, CLKs

XILINX

Title:	SCHEM, ML501 EVAL PLATFORM FPGA Banks 0,1,2,3,4 Config, FLASH, SRAM, GPIO, CLKs		
0381239			
Date:	10-10-2006_13:25	Ver:	01
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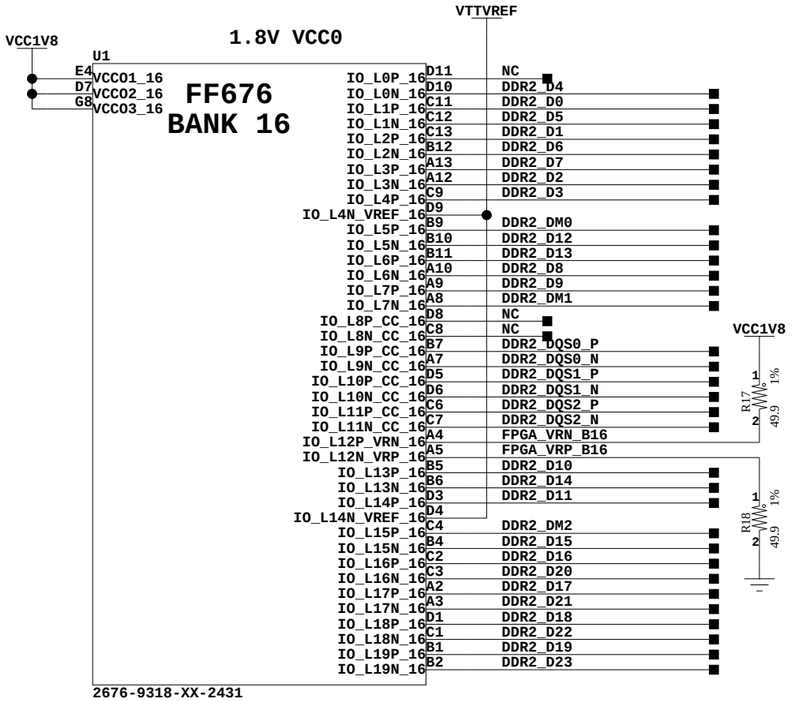

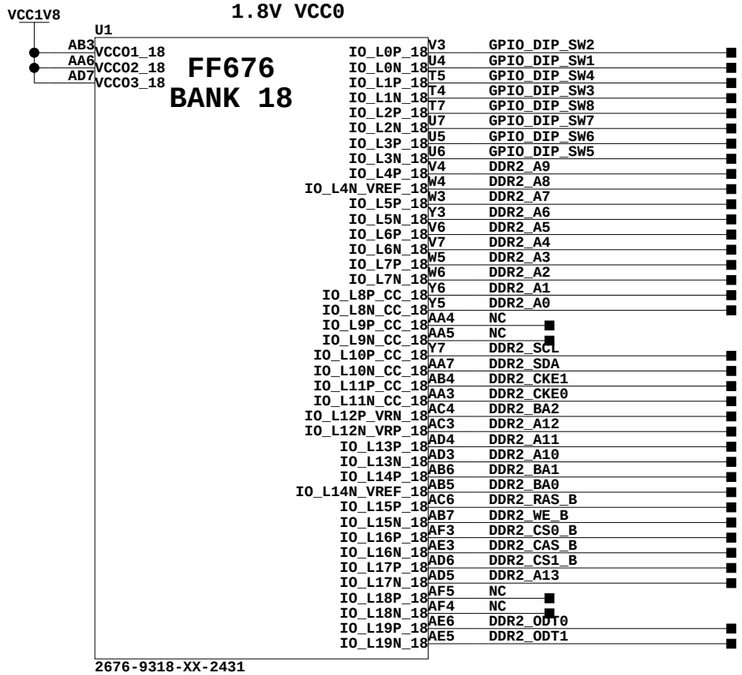

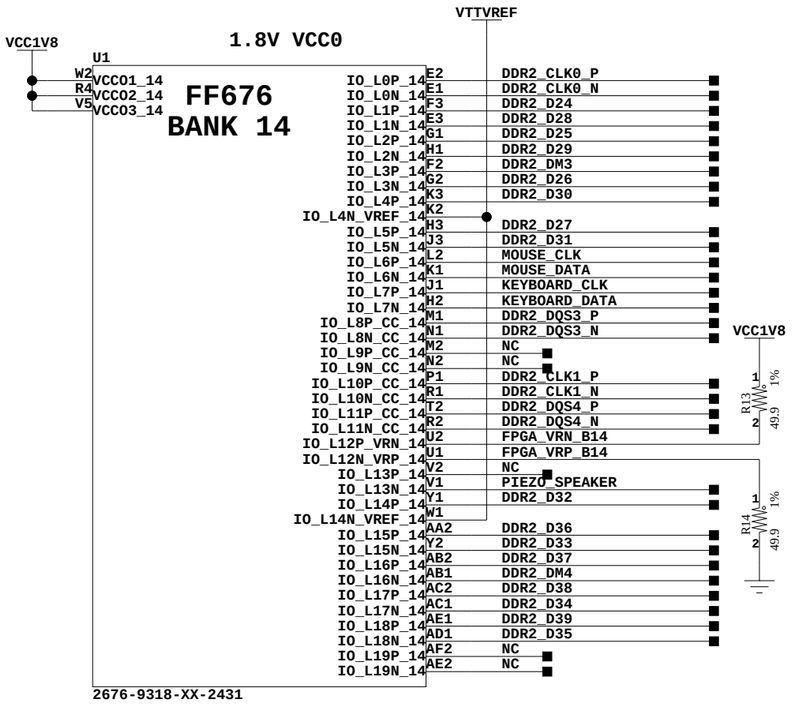

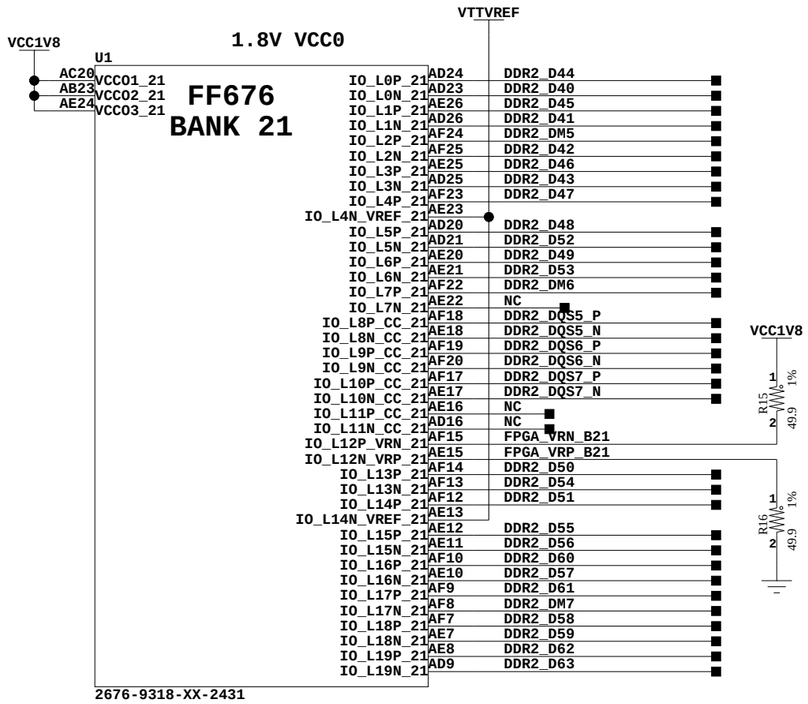

Banks 14,16,18,21
DDR2, PS2, GPIO

XILINX

Title: 0381239	SCHEM, ML501 EVAL PLATFORM FPGA Bank 14, 16, 18, 21 DDR2, PS2, GPIO		
Date:	8-30-2006_16:33	Ver:	01
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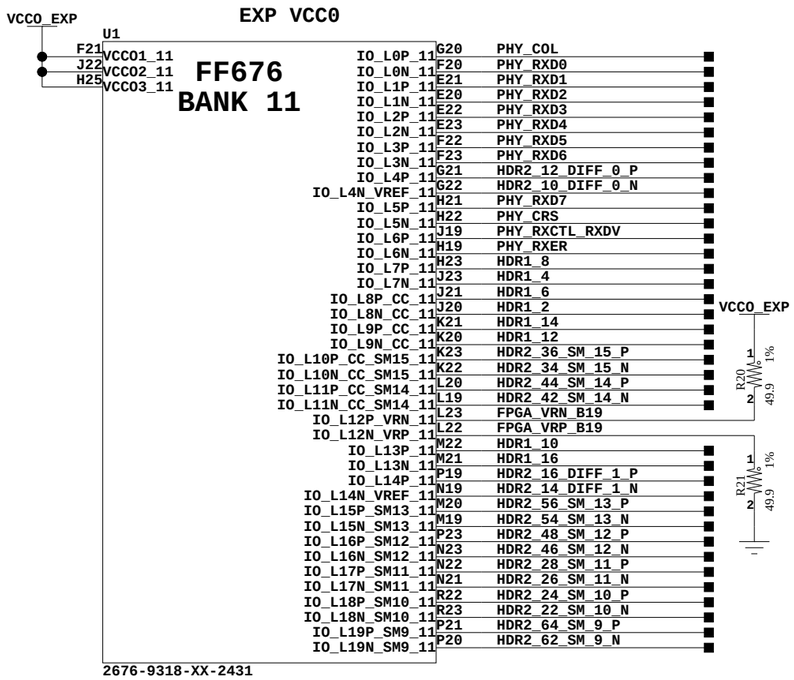
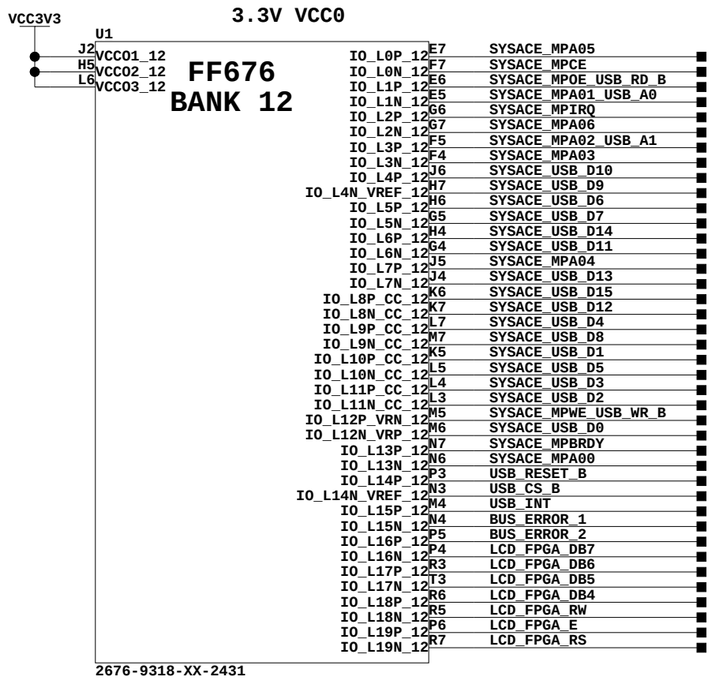
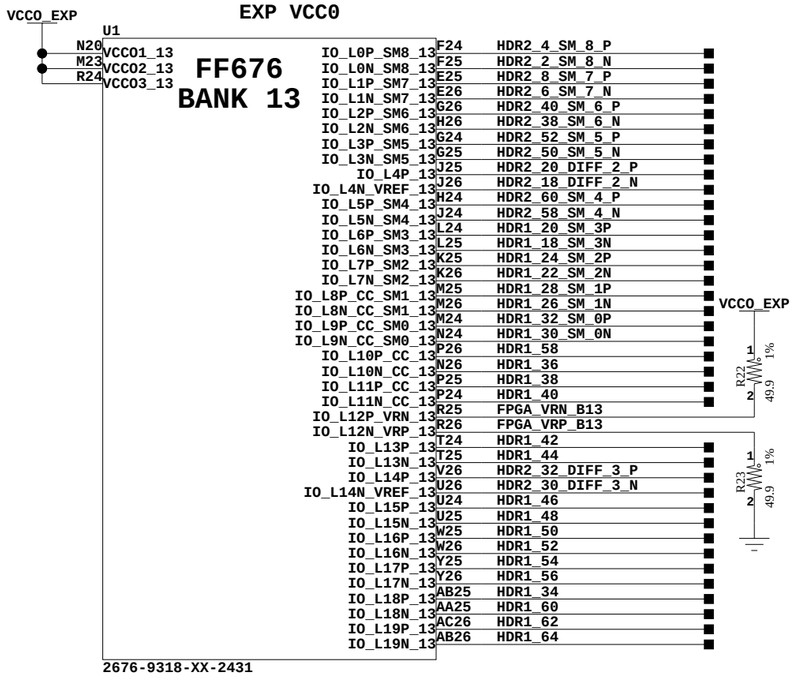
Sheet	3 of 22	Drawn By	BP







Banks 11,12,13
Sys ACE, XGI, PHY, LCD

XILINX

Title: 0381239	SCHEM, ML501 EVAL PLATFORM Banks 11,12,13 Sys ACE, XGI, PHY, LCD		
Date:	8-30-2006_16:33	Ver:	01
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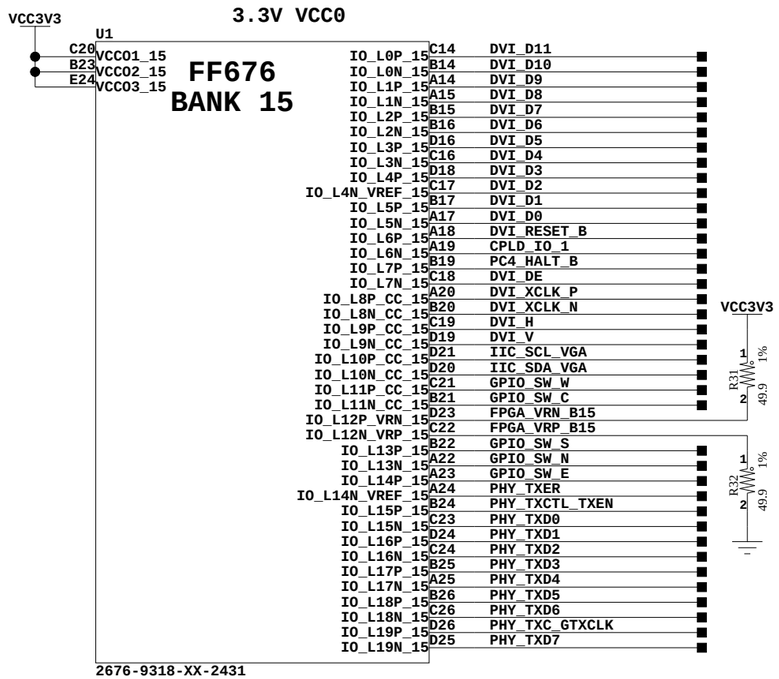

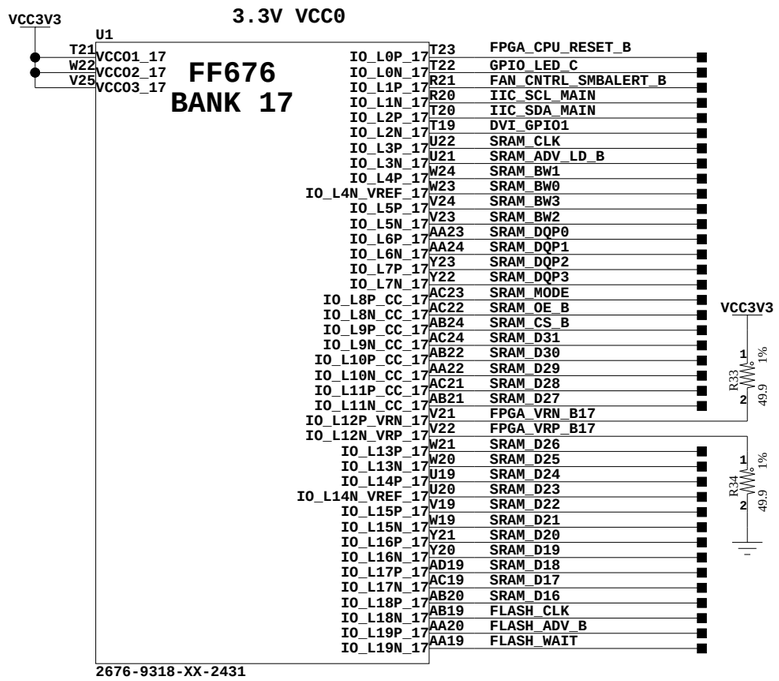

Banks 15, 17
DVI, IIC, PHY
SRAM, FLASH, GPIO

XILINX

Title: 0381239	SCHEM, ML501 EVAL PLATFORM Banks 11,12,13 DVI, IIC, PHY, SRAM, GPIO		
Date:	8-30-2006_16:33	Ver:	01
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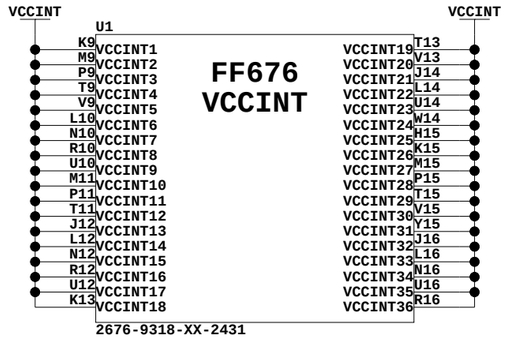
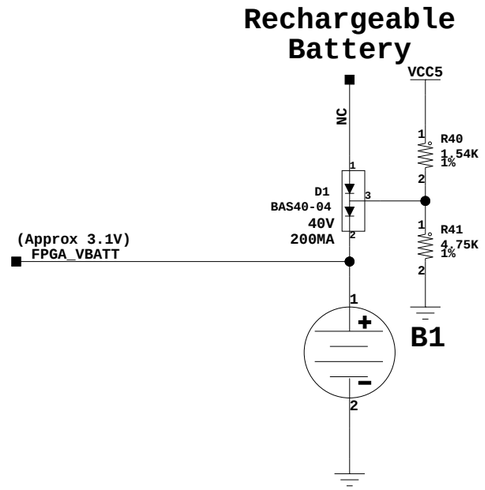
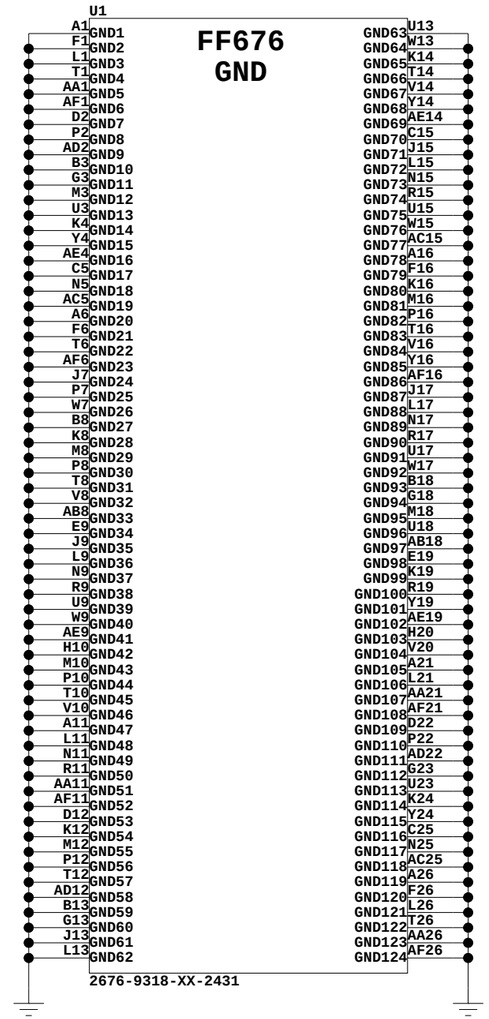
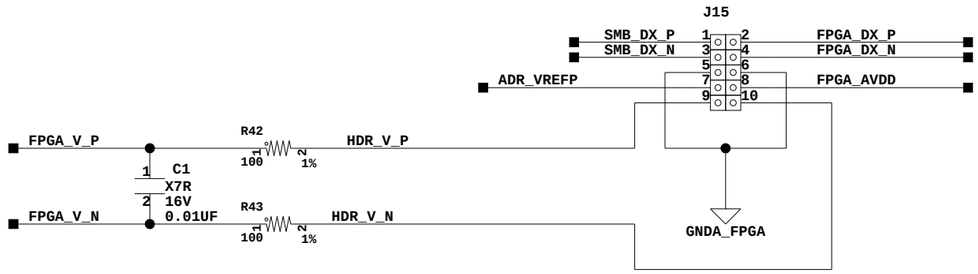


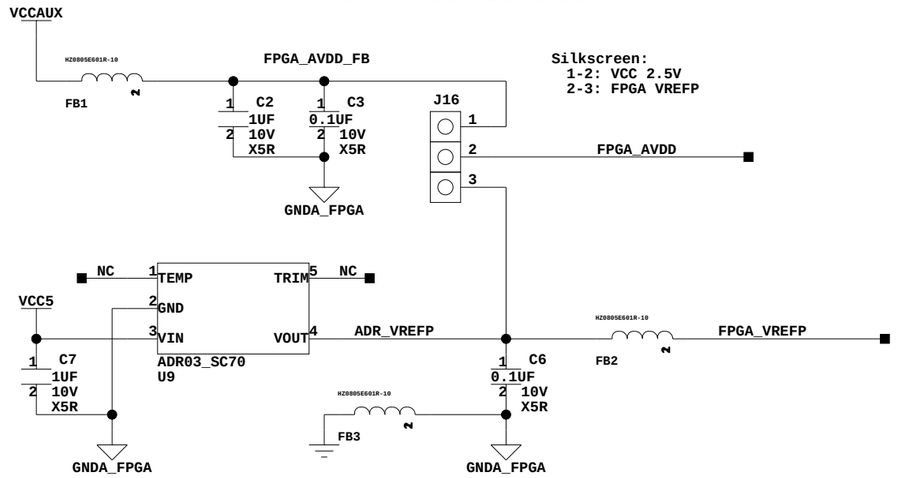




System Monitor Header



FPGA AVDD Select



Misc Banks
VCCINT, VCCAUX, GND
System Moniter

XILINX

Title: 0381239	SCHEM, ML501 EVAL PLATFORM FPGA Misc VCCINT, VCCAUX, GND, Sys Mon		
Date:	8-30-2006_16:33	Ver:	01
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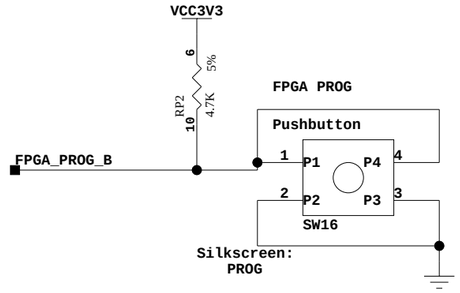

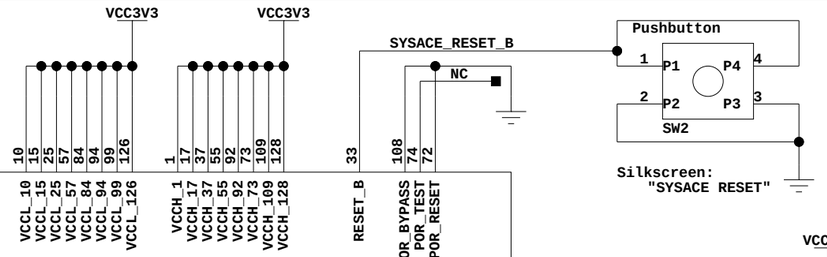

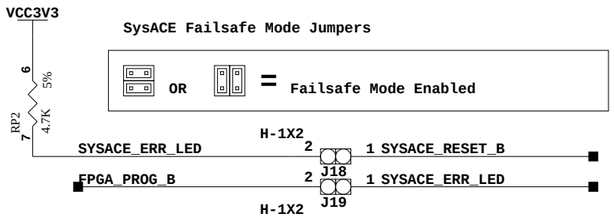

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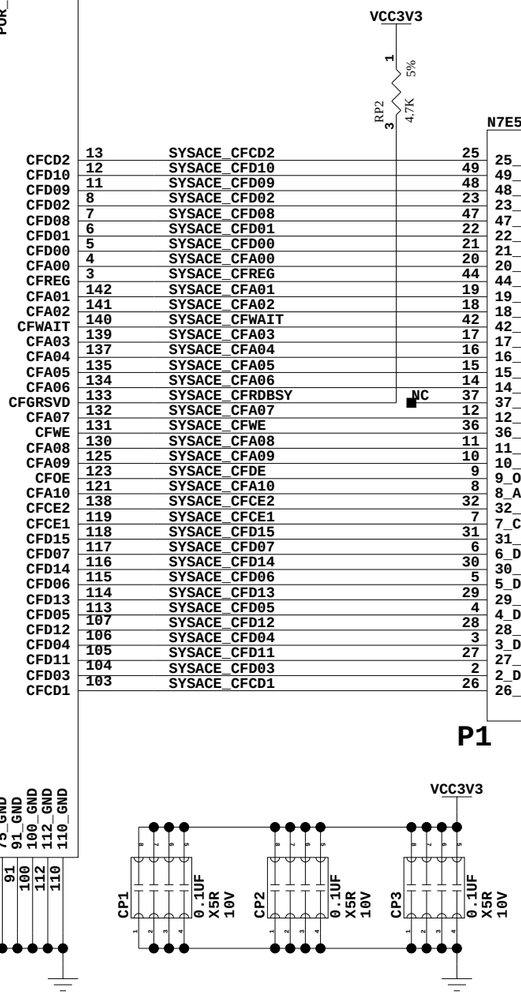
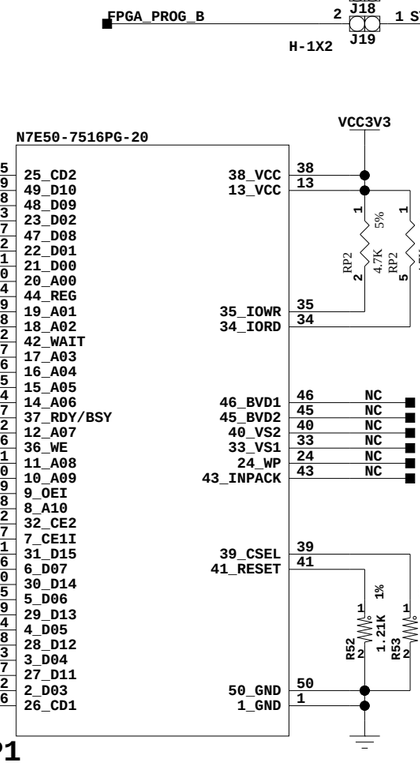
SYSACE_MPIRQ	41	MPIRQ
SYSACE_MPCE	42	MPCE
SYSACE_MPA06	43	MPA06
SYSACE_MPA05	44	MPA05
SYSACE_MPA04	45	MPA04
SYSACE_USB_D15	47	MPD15
SYSACE_USB_D14	48	MPD14
SYSACE_USB_D13	49	MPD13
SYSACE_USB_D12	50	MPD12
SYSACE_USB_D11	51	MPD11
SYSACE_USB_D10	52	MPD10
SYSACE_USB_D9	53	MPD09
SYSACE_USB_D8	56	MPD08
SYSACE_USB_D7	58	MPD07
SYSACE_USB_D6	59	MPD06
SYSACE_USB_D5	60	MPD05
SYSACE_USB_D4	61	MPD04
SYSACE_USB_D3	62	MPD03
SYSACE_USB_D2	63	MPD02
SYSACE_USB_D1	65	MPD01
SYSACE_USB_D0	66	MPD00
SYSACE_MPA03	67	MPA03
SYSACE_MPA02_USB_A1	68	MPA02
SYSACE_MPA01_USB_A0	69	MPA01
SYSACE_MPA00	70	MPA00
SYSACE_MPWE_USB_WR_B	76	MPWE
SYSACE_MPOE_USB_RD_B	77	MPOE

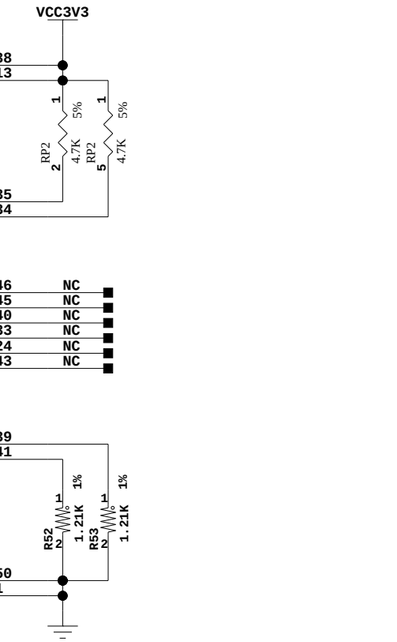
SYSTEMACE TQFP144 (DIE DOWN)

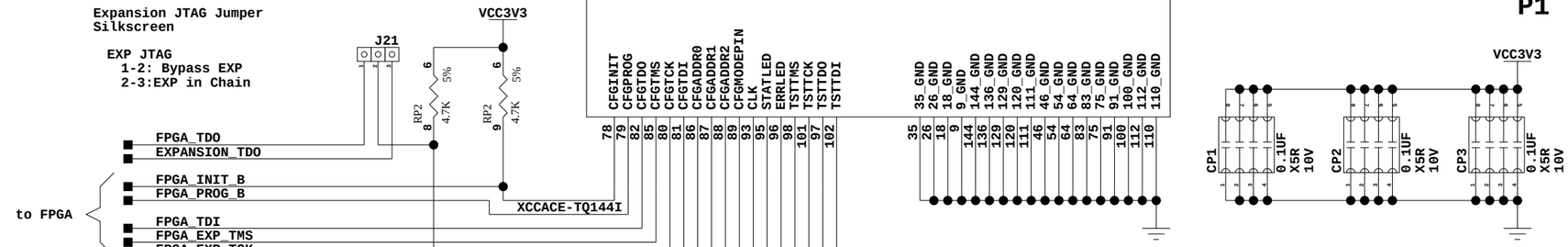
PARTS=1
LEVEL=STD

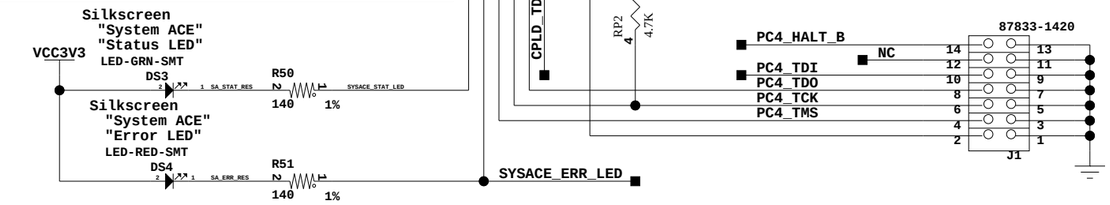
U2











Combined
FPGA & CPU
PC4 Connector

System ACE

Title: 0381239	SCHEM, ML501 EVAL PLATFORM System ACE		
Date:	8-30-2006_16:33	Ver:	01
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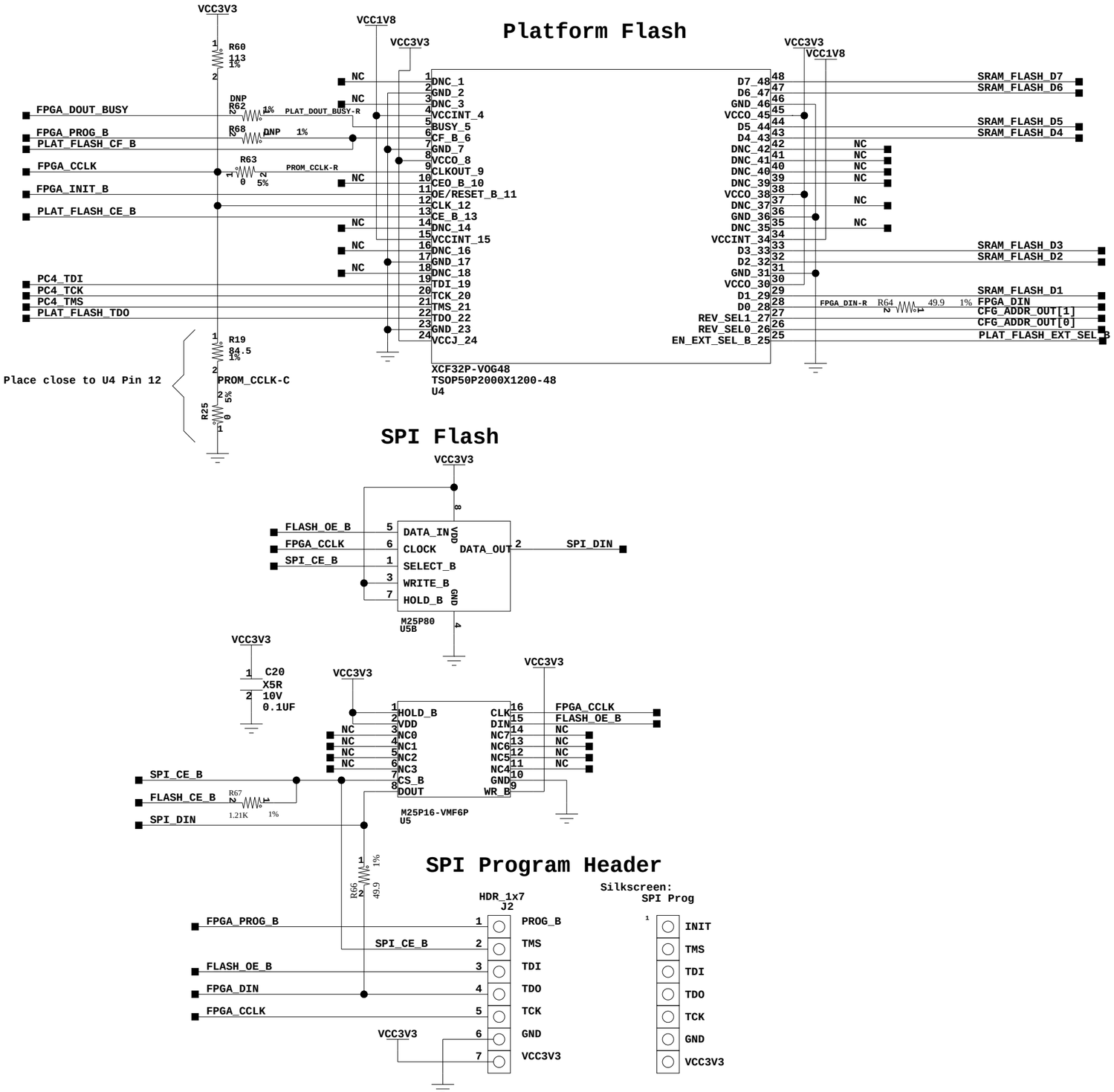

Misc Config
Platform Flash, SPI Flash

XILINX

Title: 0381239	SCHEM, ML501 EVAL PLATFORM Misc Config Platform Flash, SPI Flash		
Date:	8-30-2006_16:33	Ver:	01
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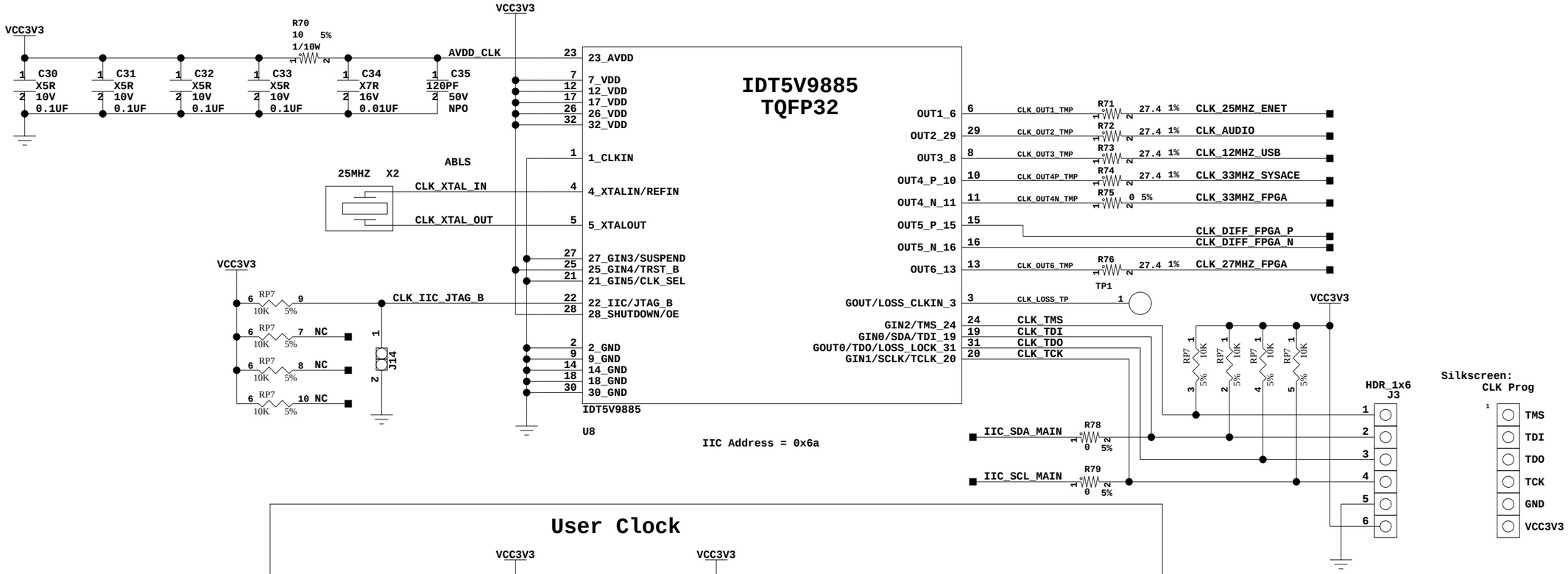
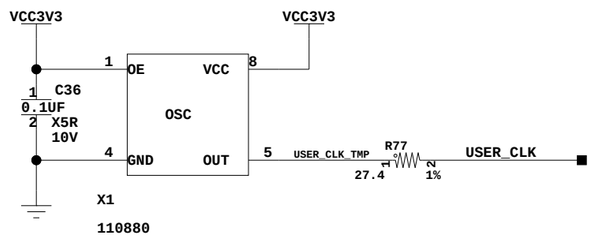
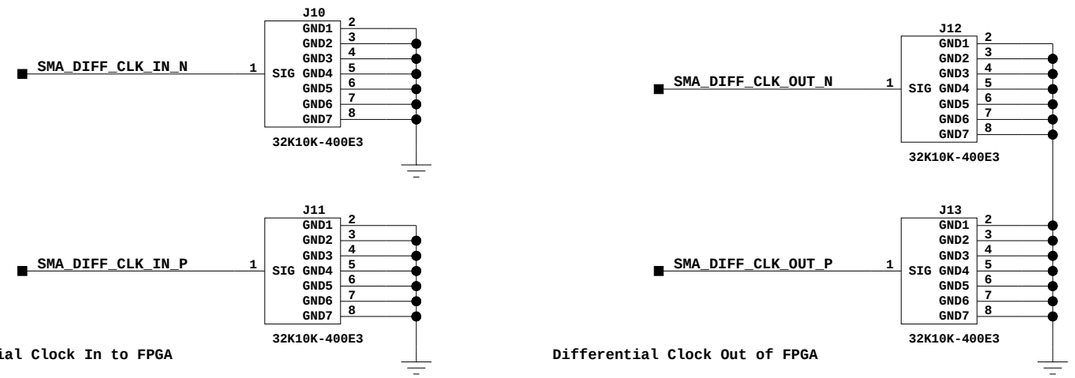
Clock Generation



User Clock



SMA Differential Clocks



Clocking - User Clk, Clk Generator SMA CLK Connectors

XILINX

Title: 0381239	SCHEM, ML501 EVAL PLATFORM Clock Generator, User Clock, SMA CLK Connectors		
Date:	8-30-2006_16:33	Ver:	01
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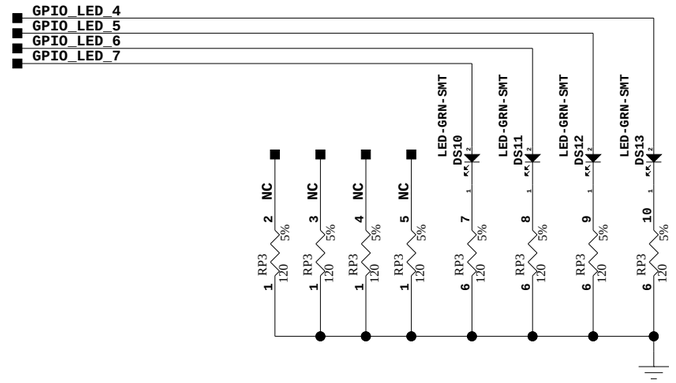

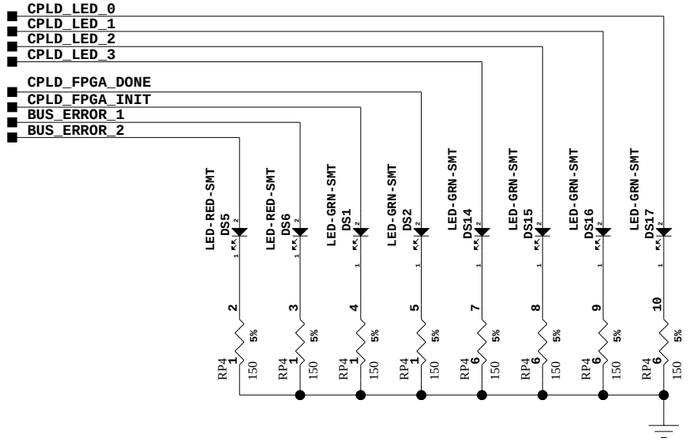

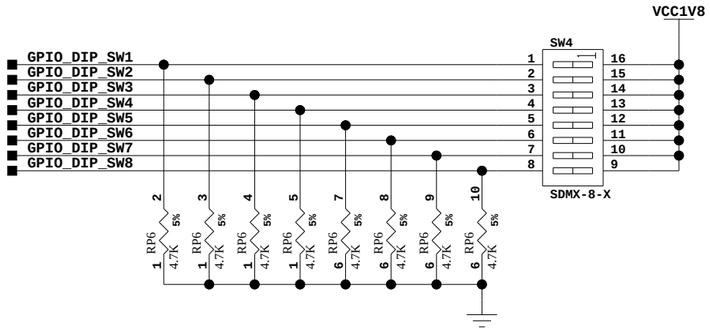

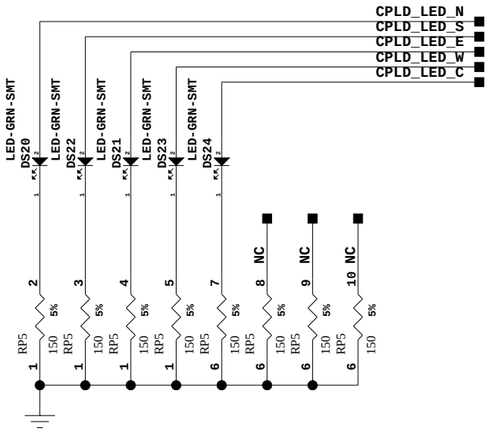

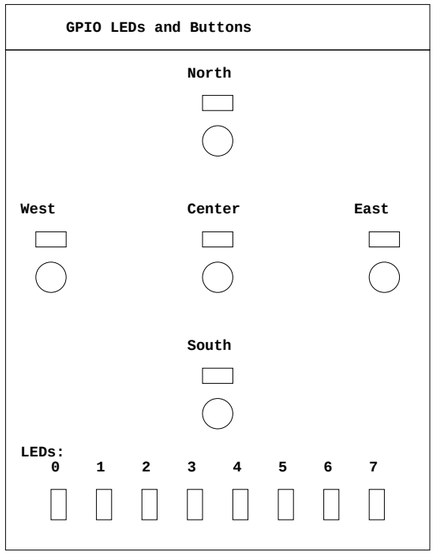

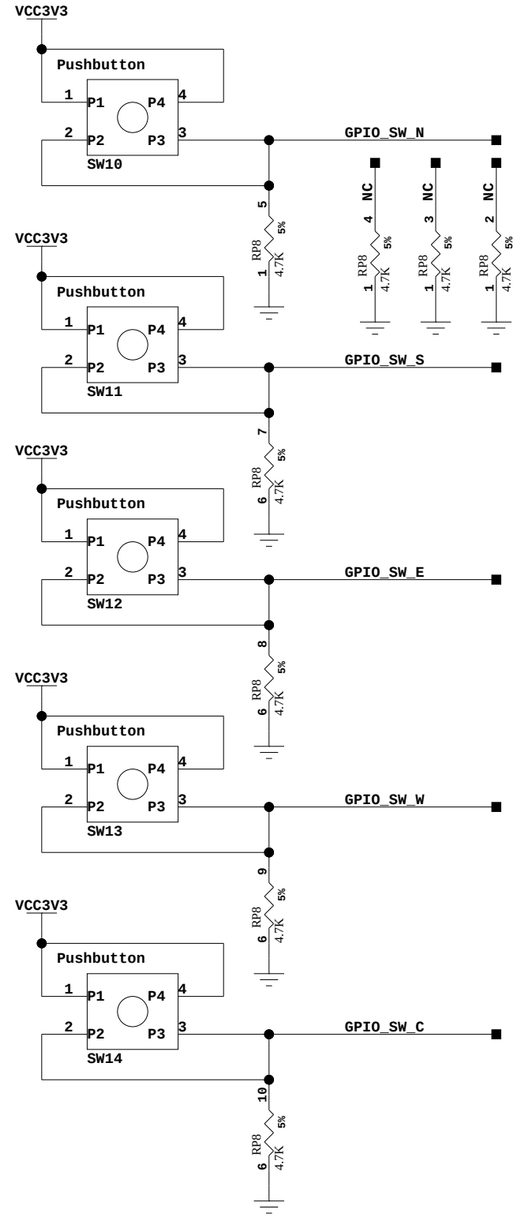

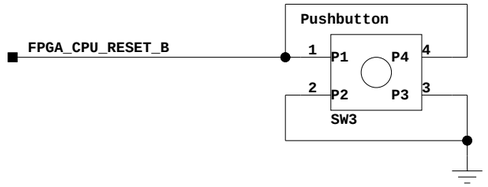

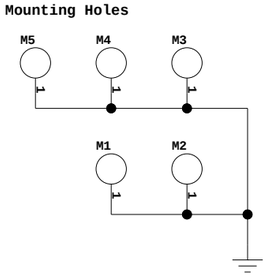

GPIO - Buttons, LEDs, Switches

Title: 0381239	SCHEM, ML501 EVAL PLATFORM GPIO Buttons, LEDs, Switches GPIO		
Date:	8-30-2006_16:33	Ver:	01
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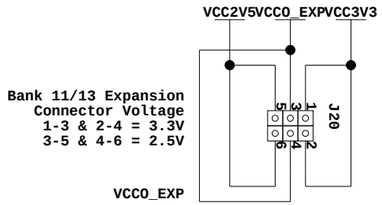
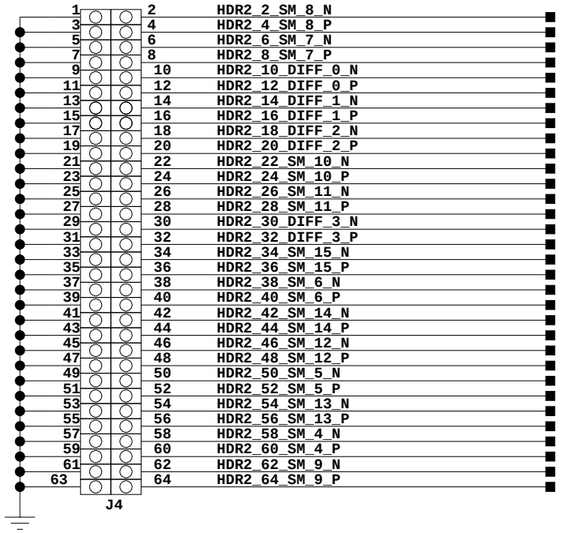
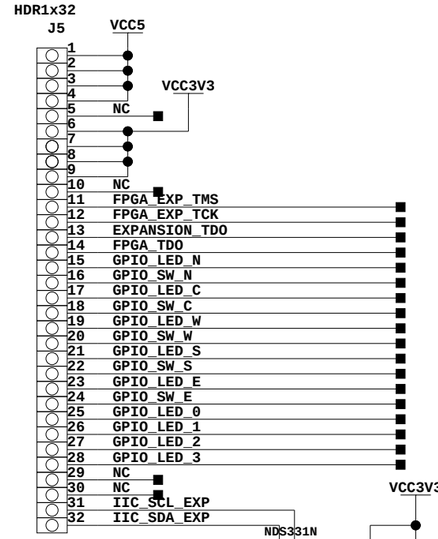
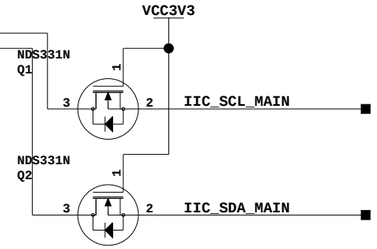
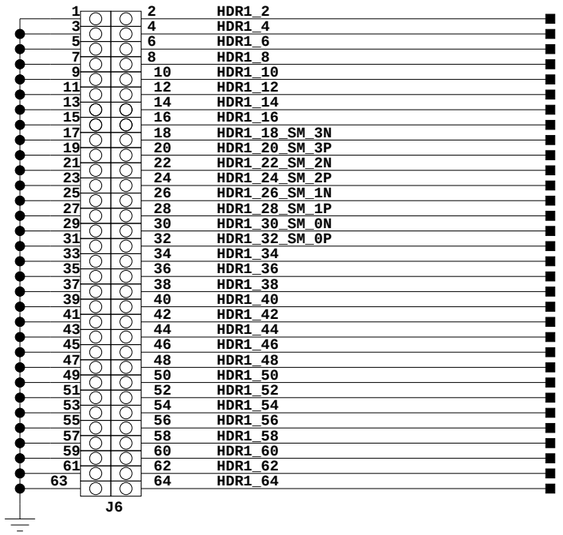




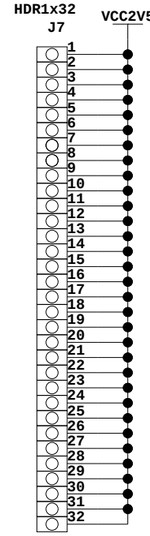
Matched Length Traces
Differential Pairs







Matched Length Traces
Independent signals



XGI - Expansion Connector

Title:	SCHEM, ML501 EVAL PLATFORM XGI - Expansion Headers		
0381239			
Date:	8-30-2006_16:33	Ver:	01
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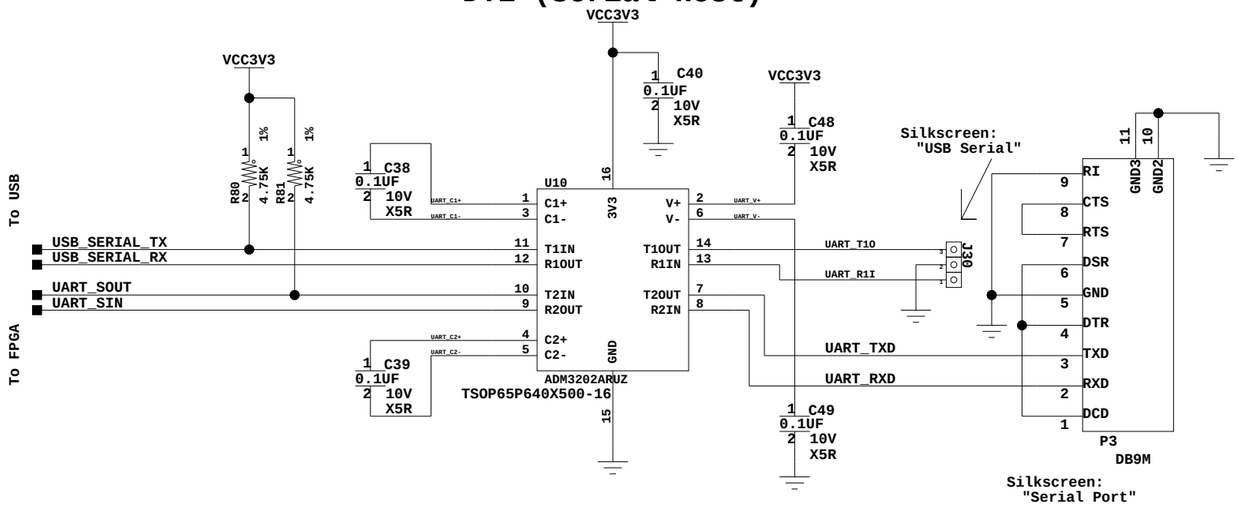
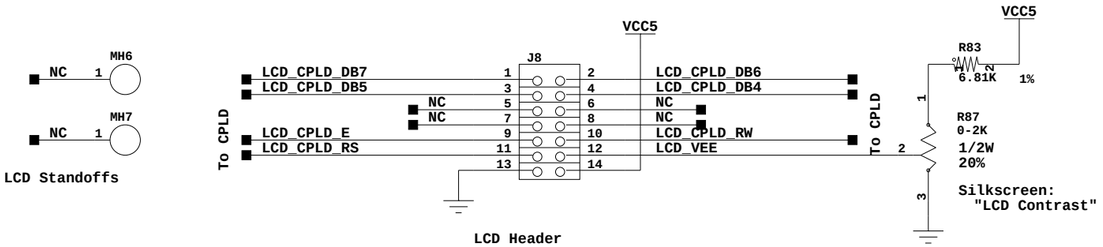
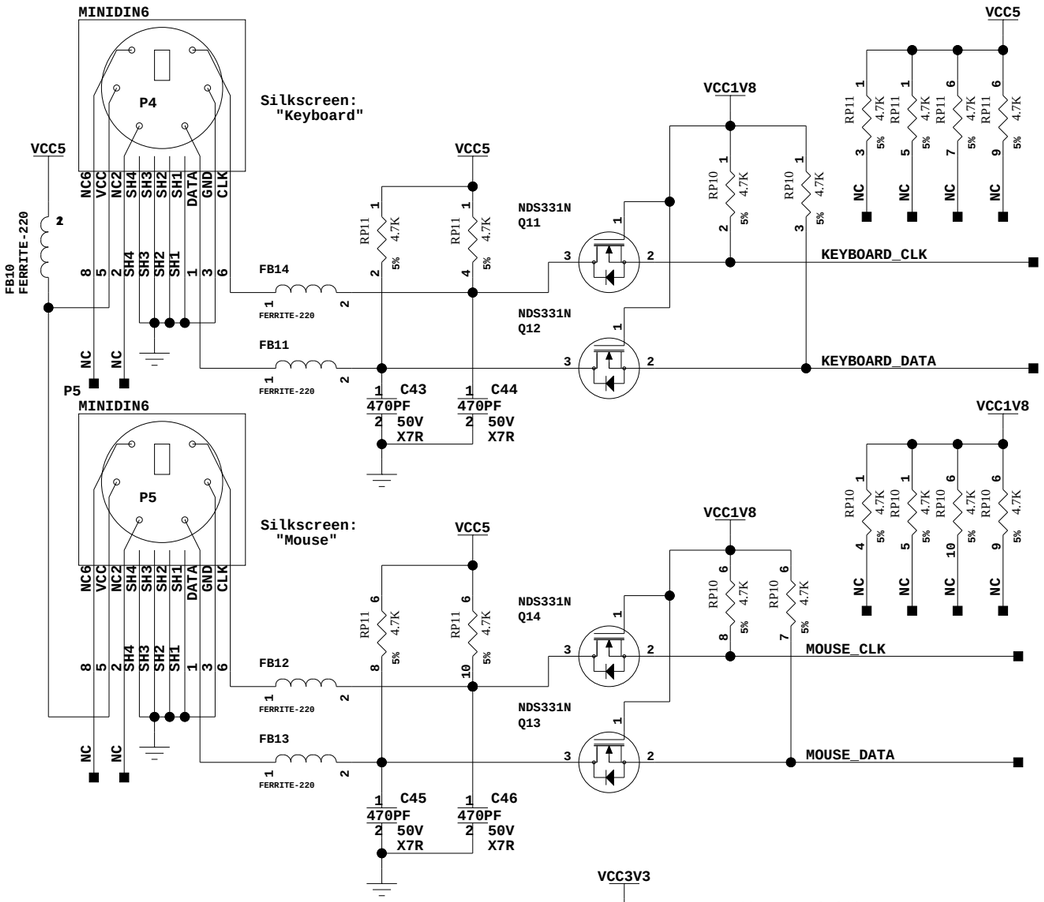
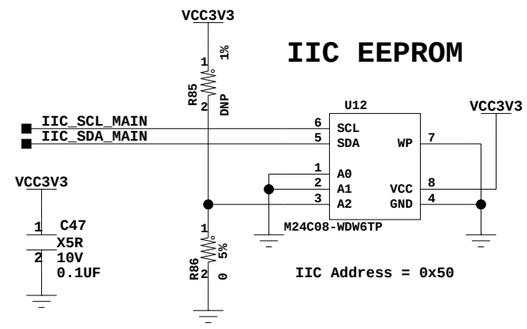
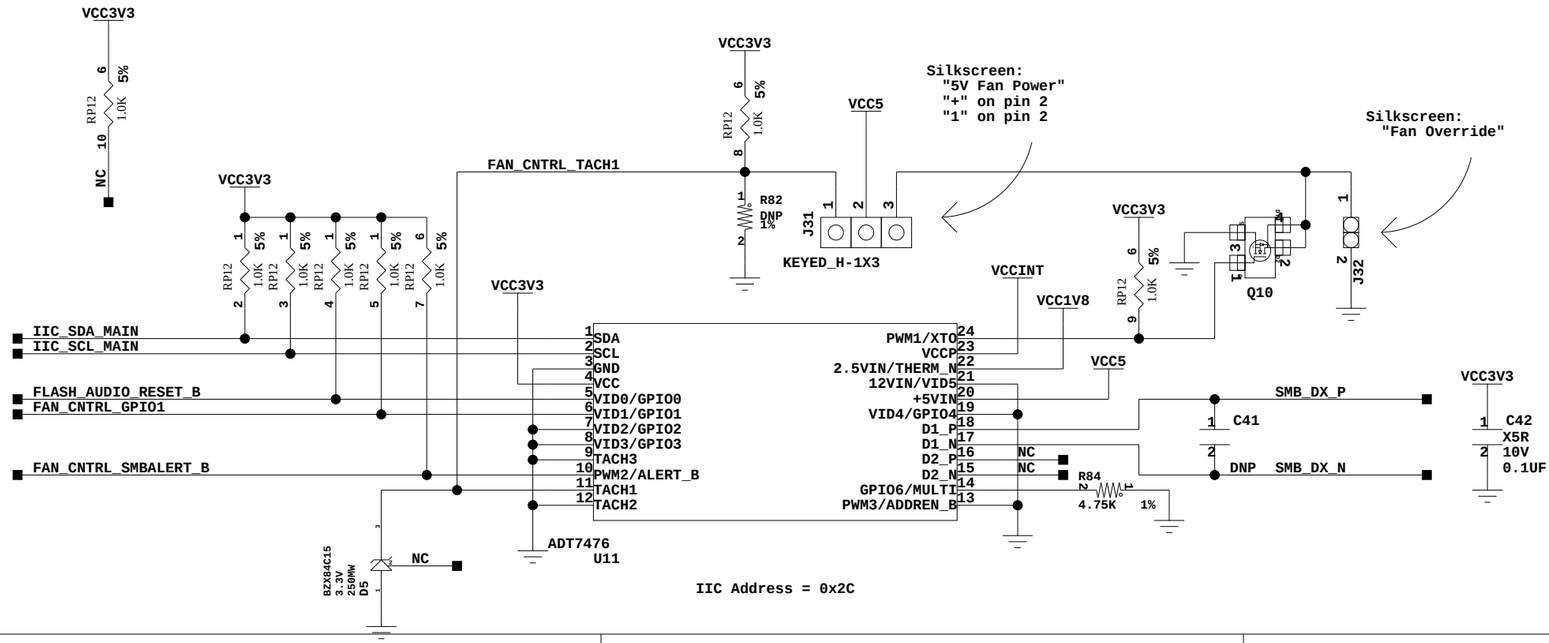
DTE (Serial Host)











Misc - LCD, PS2, UART, IIC EEPROM, Fan Cntlr

Title: 0381239	SCHEM, ML501 EVAL PLATFORM LCD, PS2, UART, IIC EEPROM IIC Fan Controller	
Date: 9-6-2006_14:46		Ver: 01
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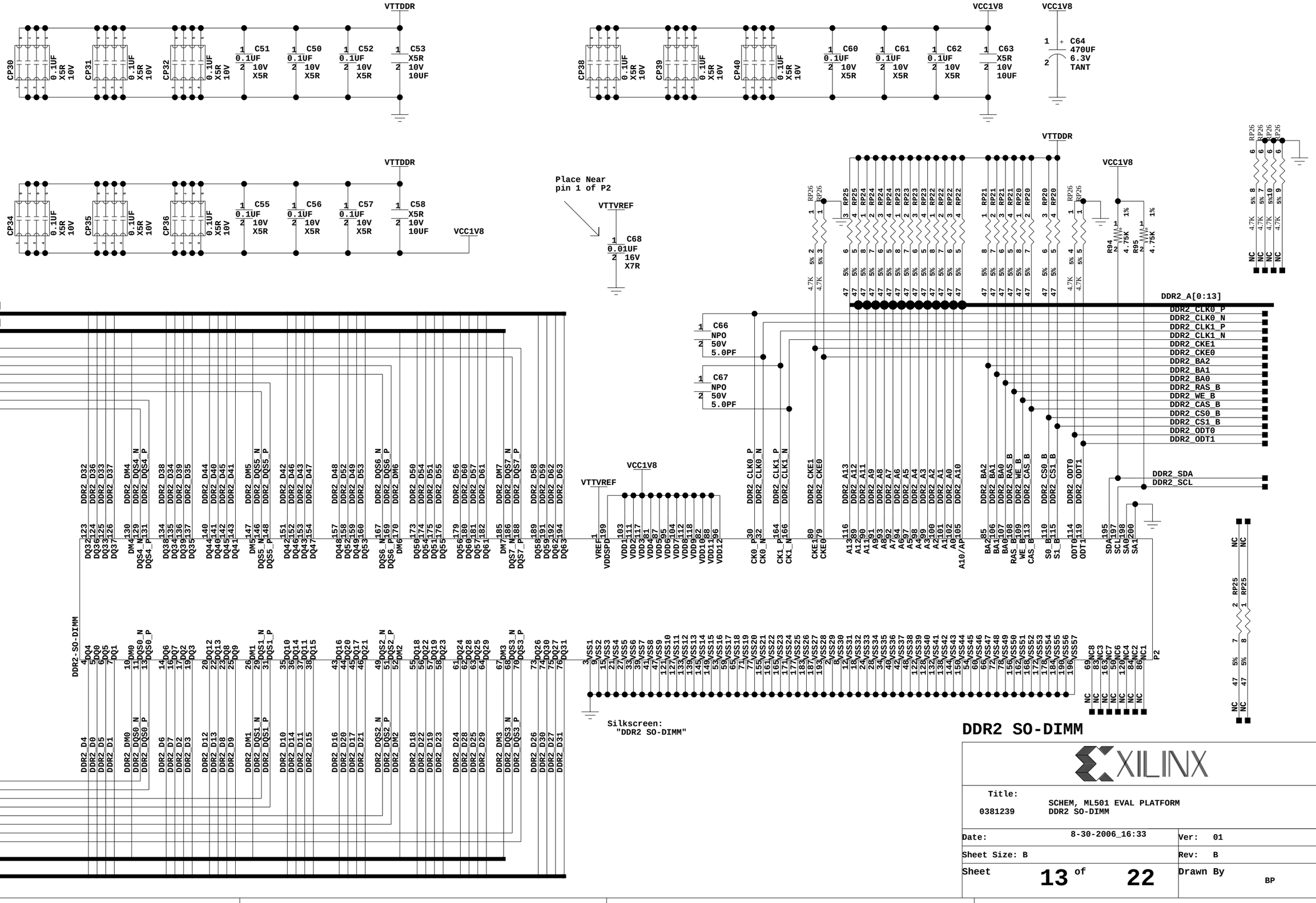

DDR2 SO-DIMM

XILINX

Title:	SCHEM, ML501 EVAL PLATFORM DDR2 SO-DIMM		
0381239			
Date:	8-30-2006_16:33	Ver:	01
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The PHY MDIP Pins below are
Media Dependent Interface Pins (MDIP),
and are all bidirectional pins.

Pin to Constant Mapping	
Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CFG3	ANEG[0]	ENA_XC	DIS_125	111	
CFG4	HWCFG_MD[2]	HWCFG_MD[1]	HWCFG_MD[0]	111	GMII to Cu mode. Fiber/copper auto-detect diasabled. Sleep mode disabled.
CFG5	DIS_FC	DIS_SLEEP	HWCFG_MD[3]	111	
CFG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active LOW interrupt 50Ohm SERDES option.

LED Silkscreen:
"10"
"100"
"1000"
"DUP"
"RX"
"TX"

Silkscreen:
1-2: GMII to Cu
2-3: RGMII to Cu

10/100/1000 PHY

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0381239	10/100/1000 PHY
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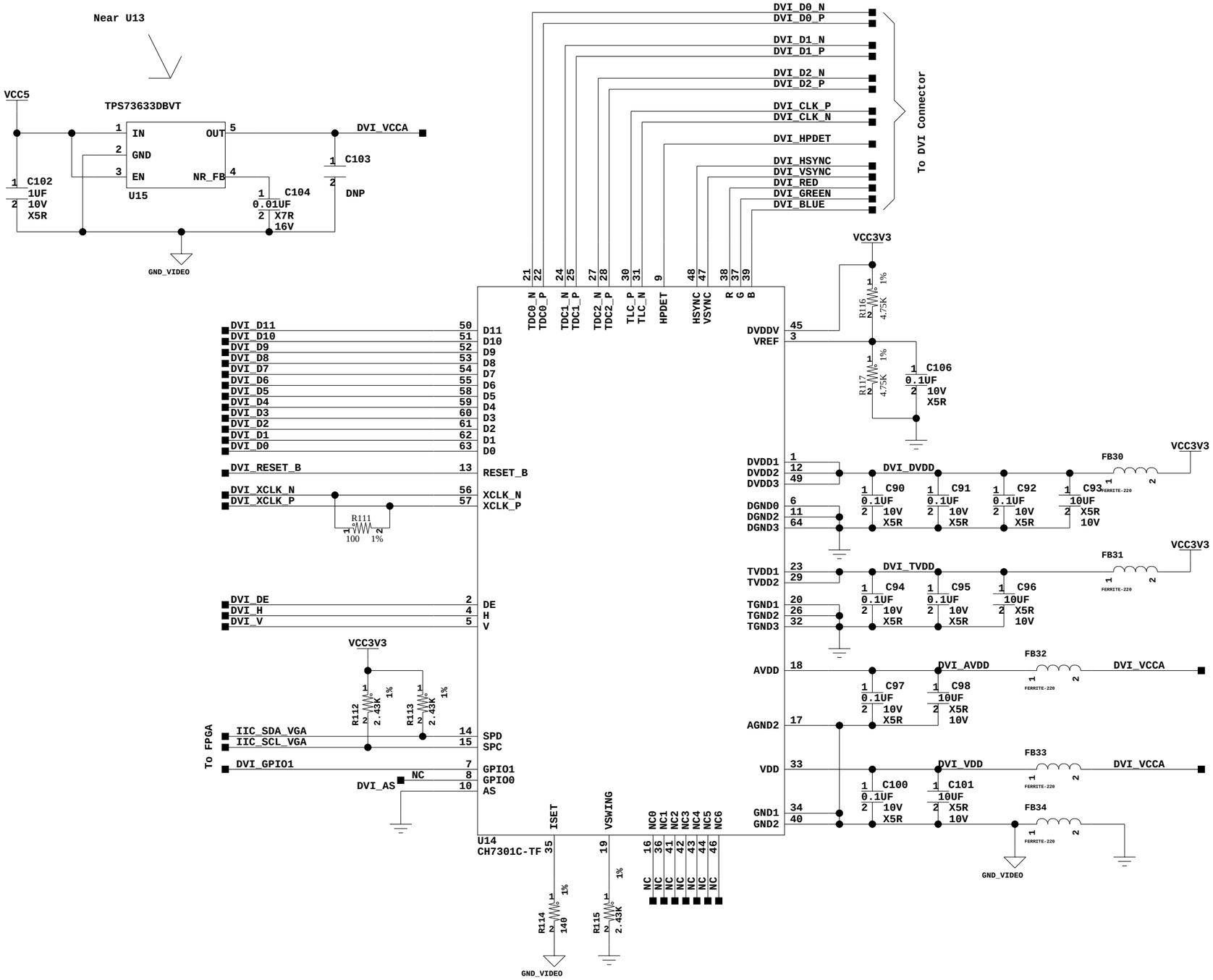

DI Codec

XILINX

Title: 0381239	SCHEM, ML501 EVAL PLATFORM DVI Codec		
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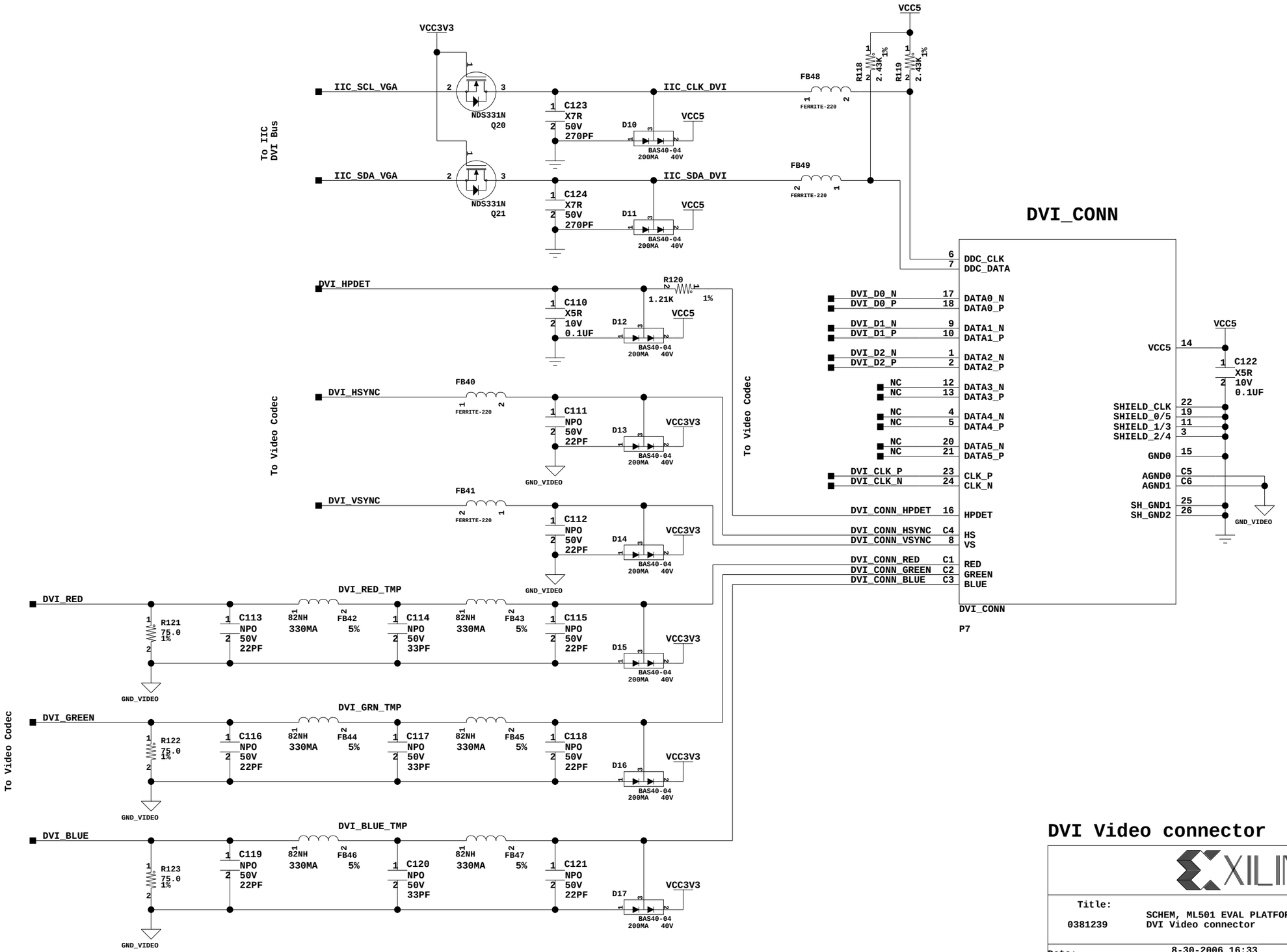

DVI Video connector

XILINX

Title: 0381239	SCHEM, ML501 EVAL PLATFORM DVI Video connector		
Date:	8-30-2006_16:33	Ver:	01
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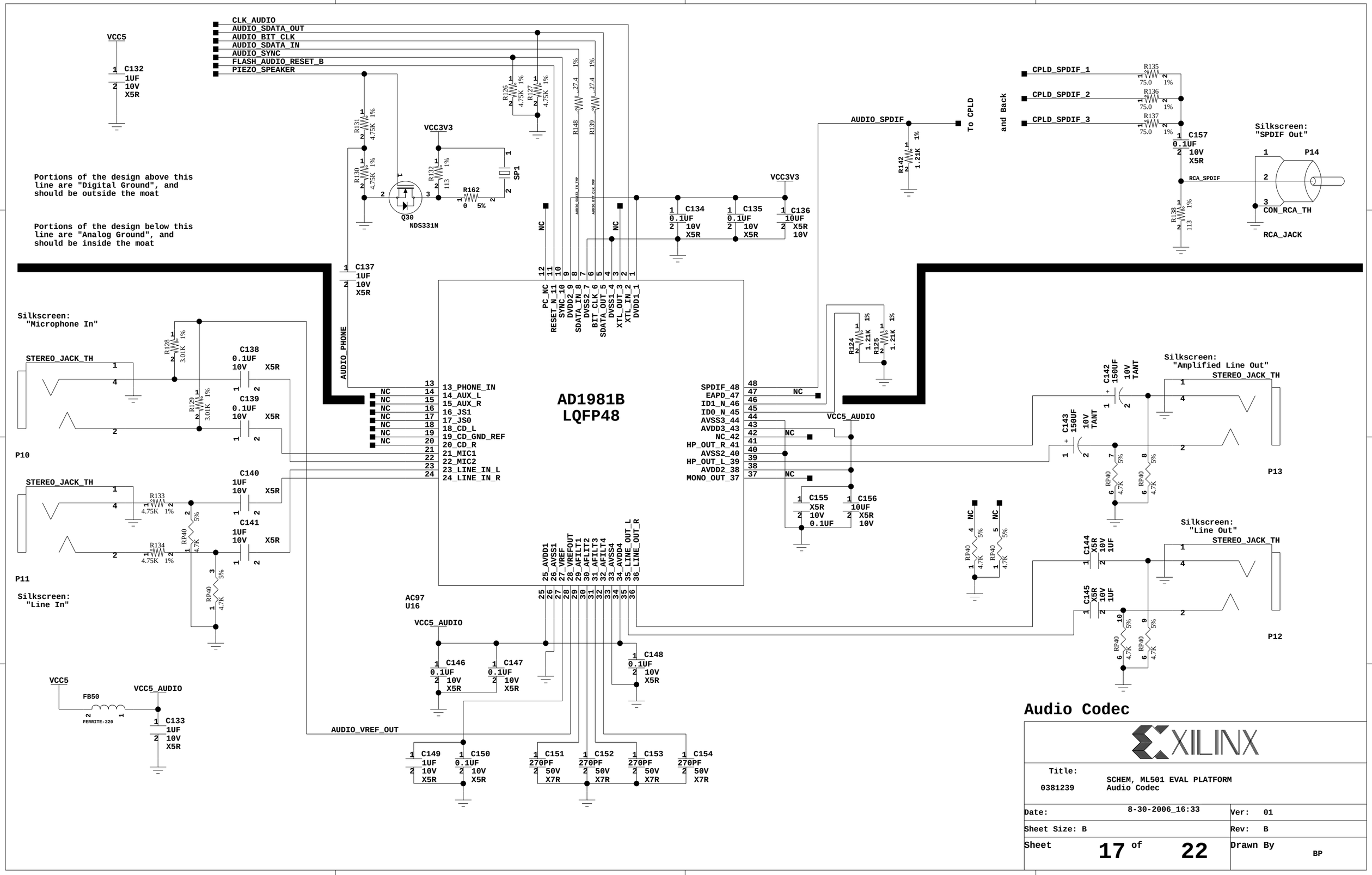

Audio Codec

XILINX

Title: 0381239	SCHEM, ML501 EVAL PLATFORM Audio Codec		
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Silkscreen:
"USB Peripheral 1"

VCC3V3

USB_PERI1_VCC
USB_PERI1_D-
USB_PERI1_D+
USB_GPIO25

R140 20.5K 1%
R141 49.9K 1%
C160 0.1UF 10V X5R

P17
SH1 SH2

NC NC NC NC NC SYSACE_USB_D0 SYSACE_USB_D1 SYSACE_USB_D2 SYSACE_USB_D3 SYSACE_USB_D4 SYSACE_USB_D5 SYSACE_USB_D6 SYSACE_USB_D7 USB_RESET_B

NC NC NC NC NC NC NC NC

VCC3V3

100 GND3_100
99 A0_99
98 BEH_N_98
97 A16_97
96 A18_96
95 A17_95
94 GPIO0_D0_94
93 GPIO1_D1_93
92 GPIO2_D2_92
91 GPIO3_D3_91
90 GPIO4_D4_90
89 GPIO5_D5_89
88 VCC2_88
87 GPIO6_D6_87
86 GPIO7_D7_86
85 RESET_N_85
84 RSVD_84
83 D0_83
82 D1_82
81 D2_81
80 D3_80
79 D4_79
78 D5_78
77 D6_77
76 D7_76

NC 1 1_A1
NC 2 2_A2
NC 3 3_A3
NC 4 4_DM2B
NC 5 5_DP2B
6 6_AGND
NC 7 7_A4
NC 8 8_A5
9 9_DM2A
10 10_DP2A
NC 11 11_OTGVBUS
NC 12 12_CSWITCHB
NC 13 13_CSWITCHA
NC 14 14_VSWITCH
15 15_BOOSTGND
16 16_BOOSTVCC
NC 17 17_A6
NC 18 18_DM1B
NC 19 19_DP1B
NC 20 20_A7
21 21_AVCC
22 22_DM1A
23 23_DP1A
NC 24 24_A8
NC 25 25_A9

CY7C67300-100AI

(DIE UP)

VCC3V3

GND2_75 75
D8_MISO_74 74 NC
D9_nSSI_73 73 NC
D10_SCK_72 72 NC
D11_MOSI_71 71 NC
D12_TXD_70 70 NC
D13_RXD_69 69 NC
D14_RTS_68 68 NC
D15_CTS_67 67 NC
GPIO8_D8_MISO_66 66 SYSACE_USB_D8
GPIO9_D9_nSSI_65 65 SYSACE_USB_D9
WR_N_64 64 NC
VCC0_63 63
RD_N_62 62 NC
GPIO10_D10_SCK_61 61 SYSACE_USB_D10
GPIO11_D11_MOSI_60 60 SYSACE_USB_D11
GPIO12_D12_59 59 SYSACE_USB_D12
GPIO13_D13_58 58 SYSACE_USB_D13
GPIO14_D14_57 57 SYSACE_USB_D14
GPIO15_D15_SSI_N_56 56 SYSACE_USB_D15
GPIO16_A0_TXD_PWM0_55 55 NC
GPIO17_A1_RXD__54 54 NC
GPIO18_A2_RTS__53 53 NC
GPIO19_A0_CS0_52 52 SYSACE_MPA01_USB_A0
GND1_51 51

Silkscreen:
"USB Host"

VCC3V3

USB_HOST1_VCC
USB_HOST1_D-
USB_HOST1_D+
USB_HOST1_GND

FB60 FERRITE-220
FB61 FERRITE-220

C164 10V 0.1UF X5R

P19
SH1 SH2 SH3 SH4

VCC3V3

R143 4.75K 1%
R144 4.75K 1%

USB_GPIO29
USB_GPIO26
NC

MIC2025
U17
EN
FLG
GND
NC1

VCC5

OUT2
IN
OUT1
NC2

USB_HOST_VCC

C170 0.1UF 10V X5R
C171 150UF 10V TANT

USB Host Power

U18

CYP_USB_HOST

26 GND0
27 A10
28 XTALOUT
29 XTALIN
30 A11
31 A12
32 A13
33 A14
34 MEMSEL_N
35 ROMSEL_N
36 RAMSEL_N
37 VCC1
38 A15
39 GPIO31_SCK
40 GPIO30_SDA
41 GPIO29_OTGID
42 GPIO28_TX
43 GPIO27_RX
44 GPIO26_CTS_PWM3
45 GPIO25_IRQ1
46 GPIO24_INT_IORDY_IRQ0
47 GPIO23_RD_N_IOR
48 GPIO22_WR_N_IOW
49 GPIO21_CS_N
50 GPIO20_A1_CS1

NC NC

R147 49.9K 1%

CLK_12MHZ_USB
IIC_SCL_USB
IIC_SDA_USB
USB_GPIO29
USB_SERIAL_TX
USB_SERIAL_RX
USB_GPIO26
USB_GPIO25
USB_INT
SYSACE_MPOE_USB_RD_B
SYSACE_MPWE_USB_WR_B
USB_CS_B
SYSACE_MPA02_USB_A1

VCC3V3

R145 4.75K 1%
R146 4.75K 1%

"Abort Boot"
J50

VCC3V3

C172 0.1UF 10V X5R

VCC3V3

U28
WP
VCC
GND
SCL
SDA
A0
A1
A2

M24128-BWDW6TP

SDA/SCL lines swapped for an
EEPROM larger than 16KB

VCC3V3

C165 0.1UF 10V X5R
C166 0.1UF 10V X5R
C167 0.1UF 10V X5R
C168 0.1UF 10V X5R

Bypass cap for USB chip

USB Controller

XILINX

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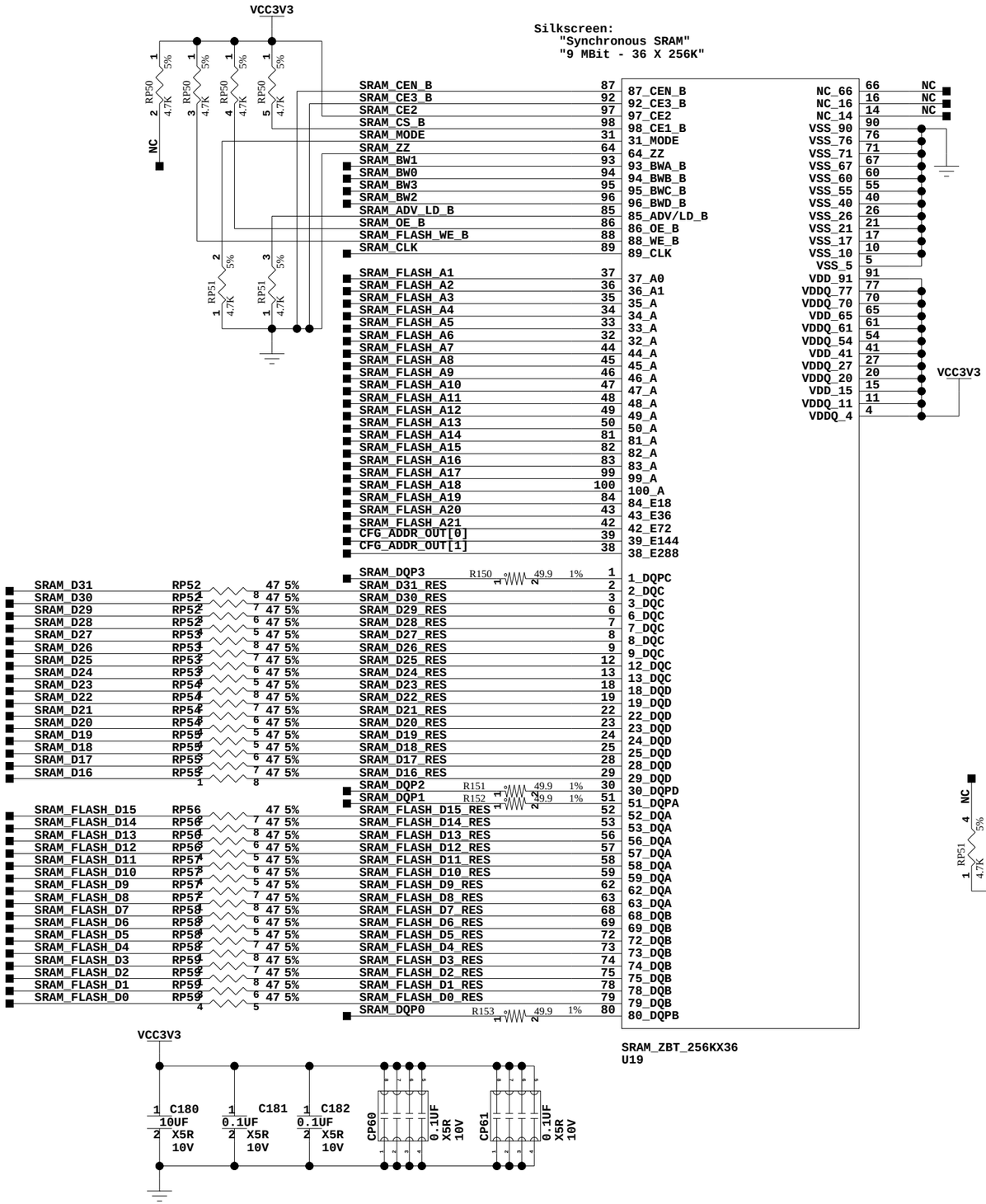
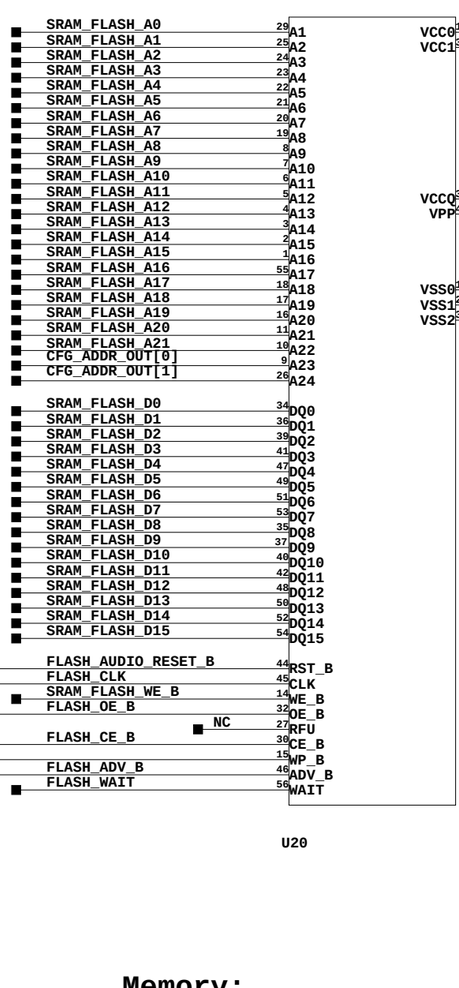
The burst order mode of the SRAM is set to "Linear" by default

Silkscreen:
"Synchronous SRAM"
"9 MBit - 36 X 256K"



Silkscreen:
"Strata FLASH"
"256 MBit"



Memory:
Synchronous SRAM,
Strata FLASH

XILINX

Title: 0381239	SCHEM, ML501 EVAL PLATFORM Sync. SRAM, FLASH		
Date:	8-30-2006_16:33	Ver:	01
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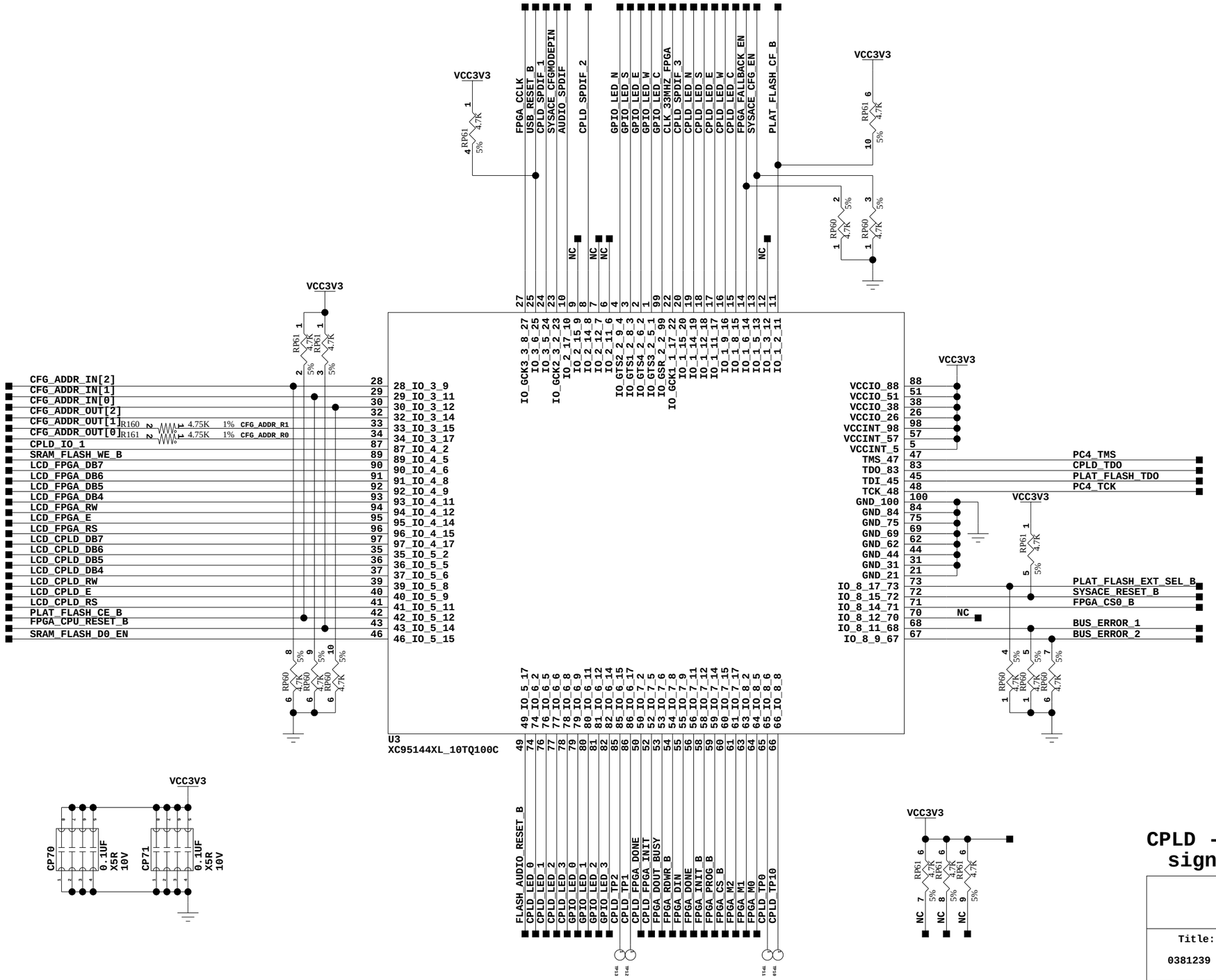

CPLD - Misc signal control

Title: 0381239	SCHEM, ML501 EVAL PLATFORM CPLD - Misc signal control		
Date:	8-30-2006_16:33	Ver:	01
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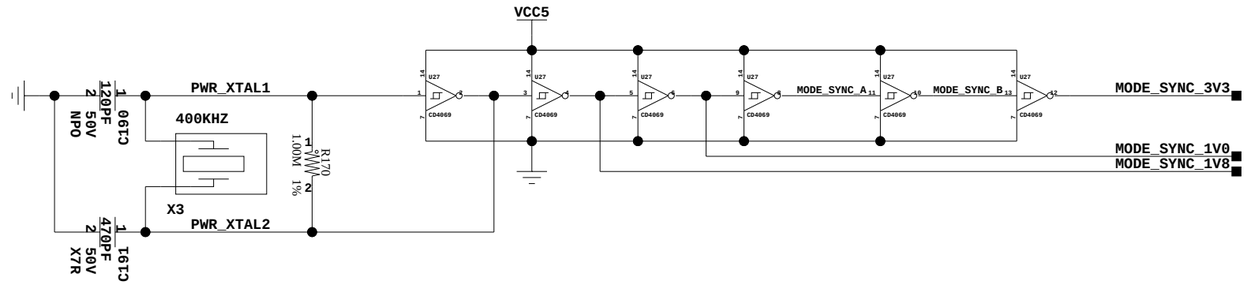

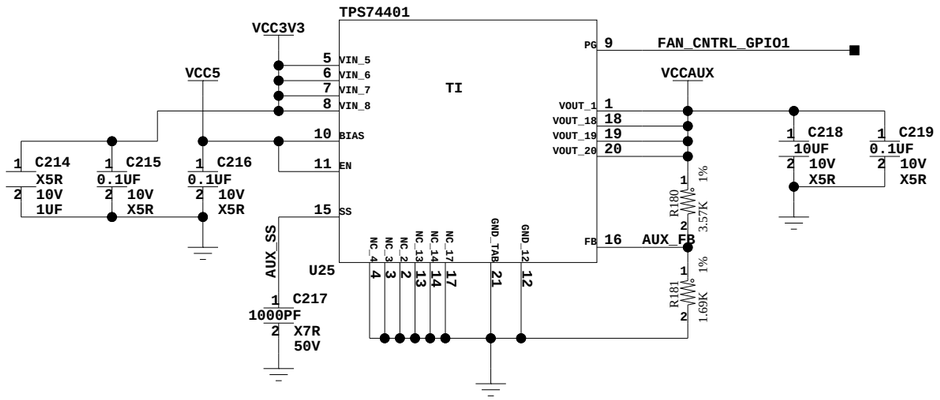

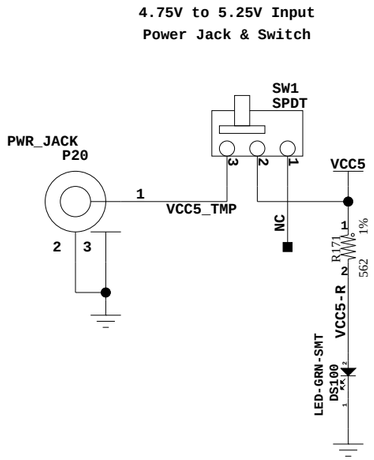

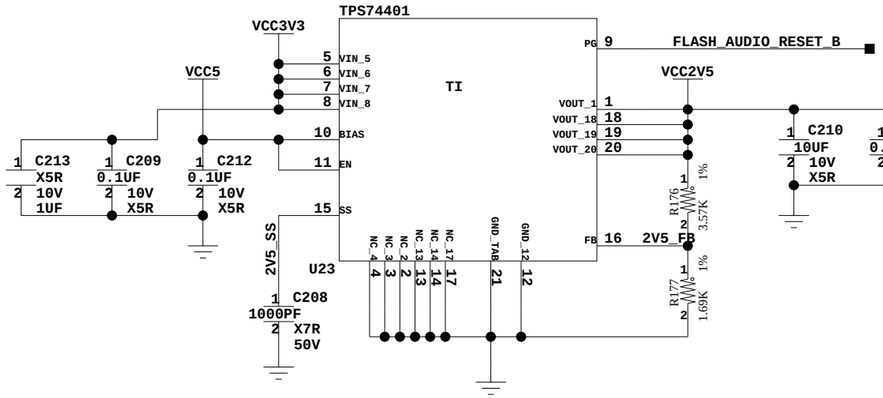

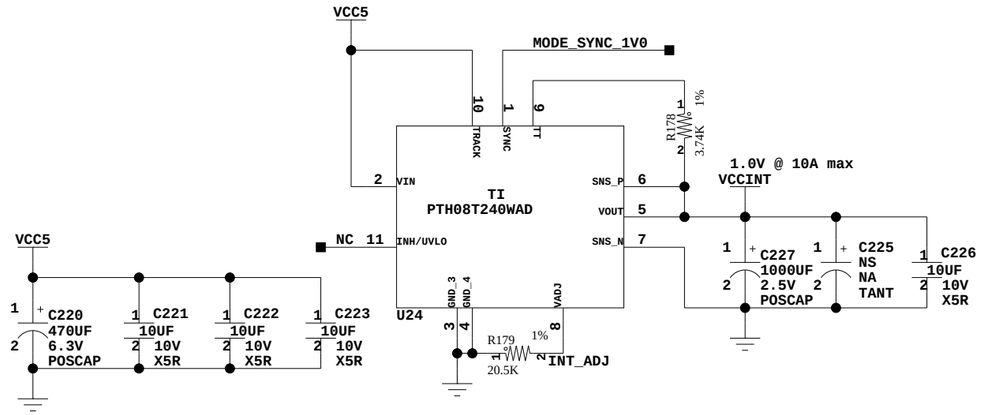

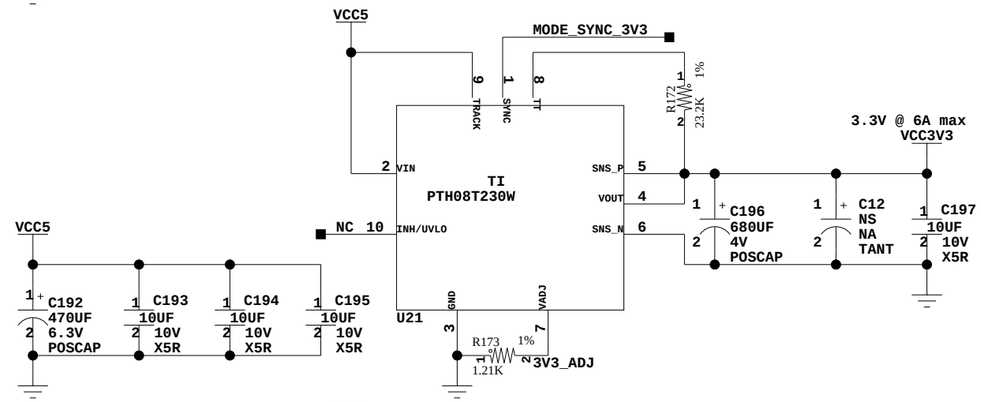

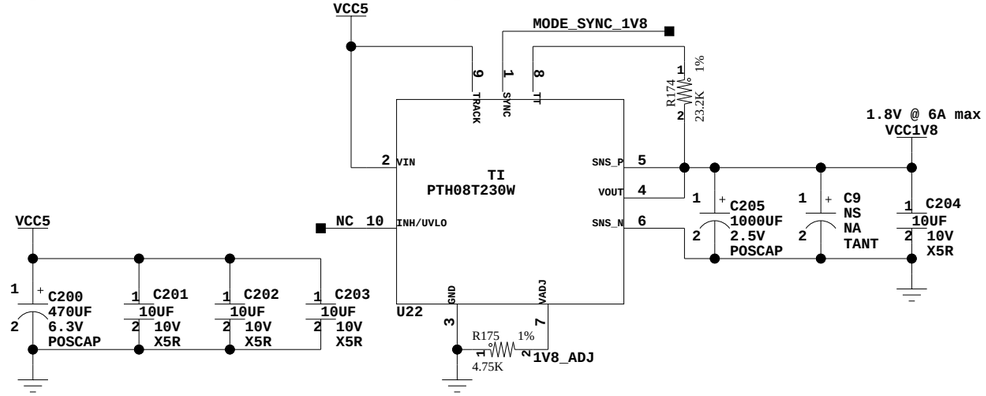

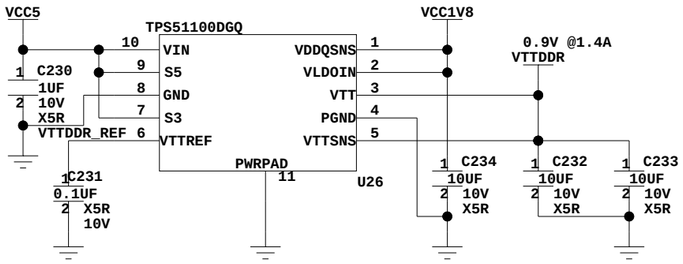

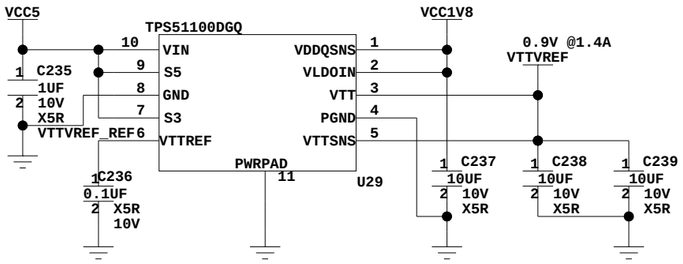

Power Supplies

XILINX

Title: 0381239	SCHEM, ML501 EVAL PLATFORM Power Supplies		
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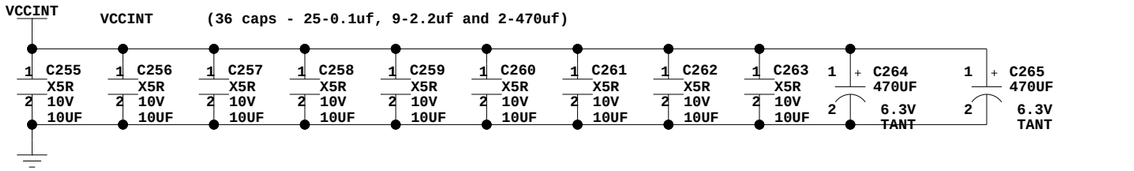
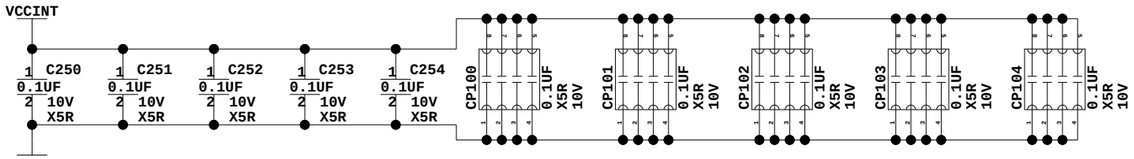
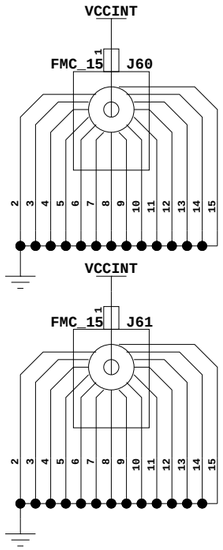
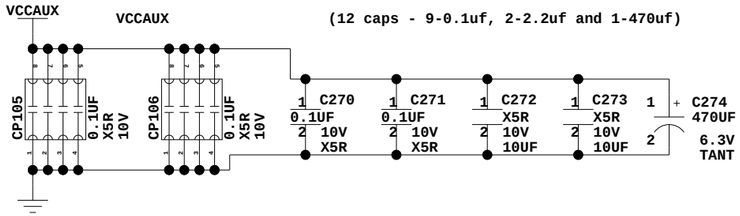
VCCINT Caps

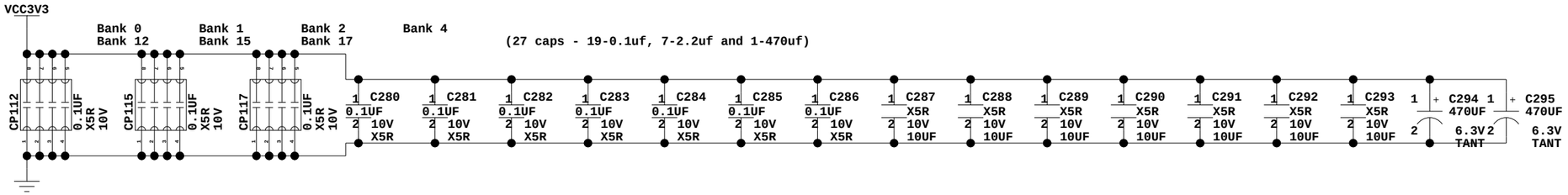


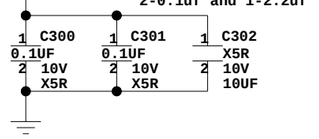


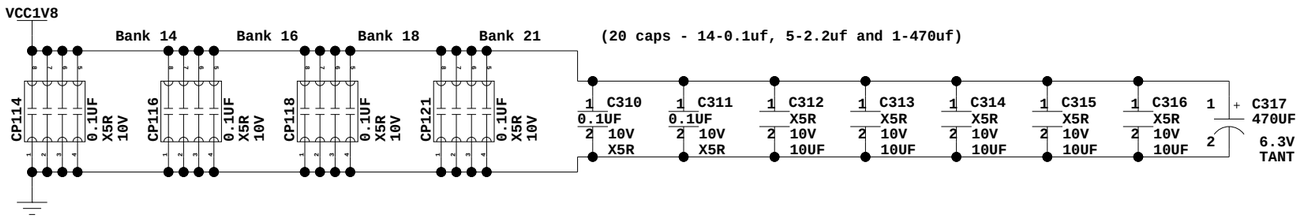


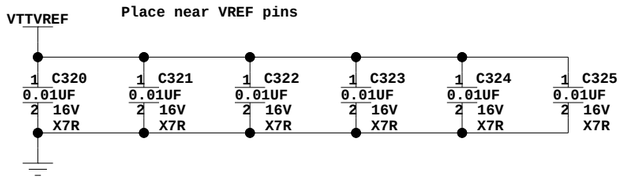


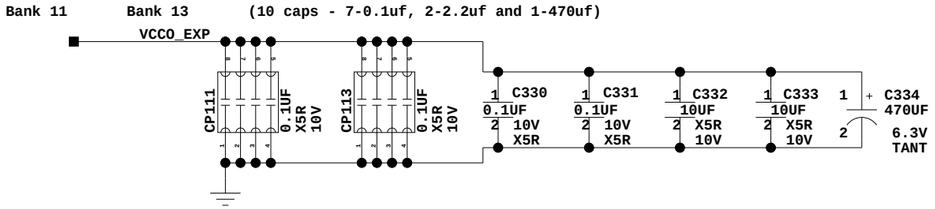
VCCO Caps











XILINX

Title: 0381239	SCHEM, ML501 EVAL PLATFORM FPGA Decoupling	
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