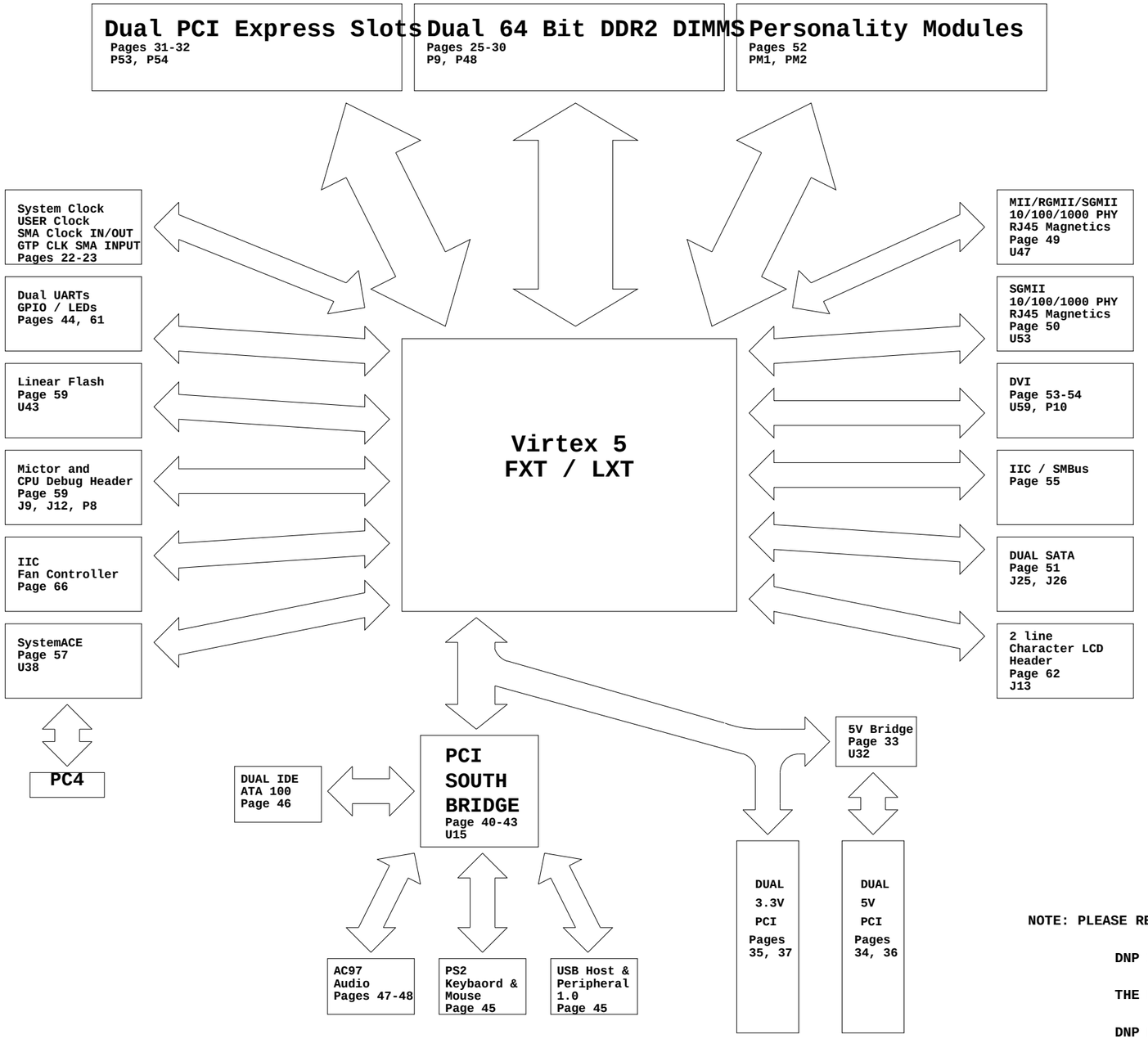
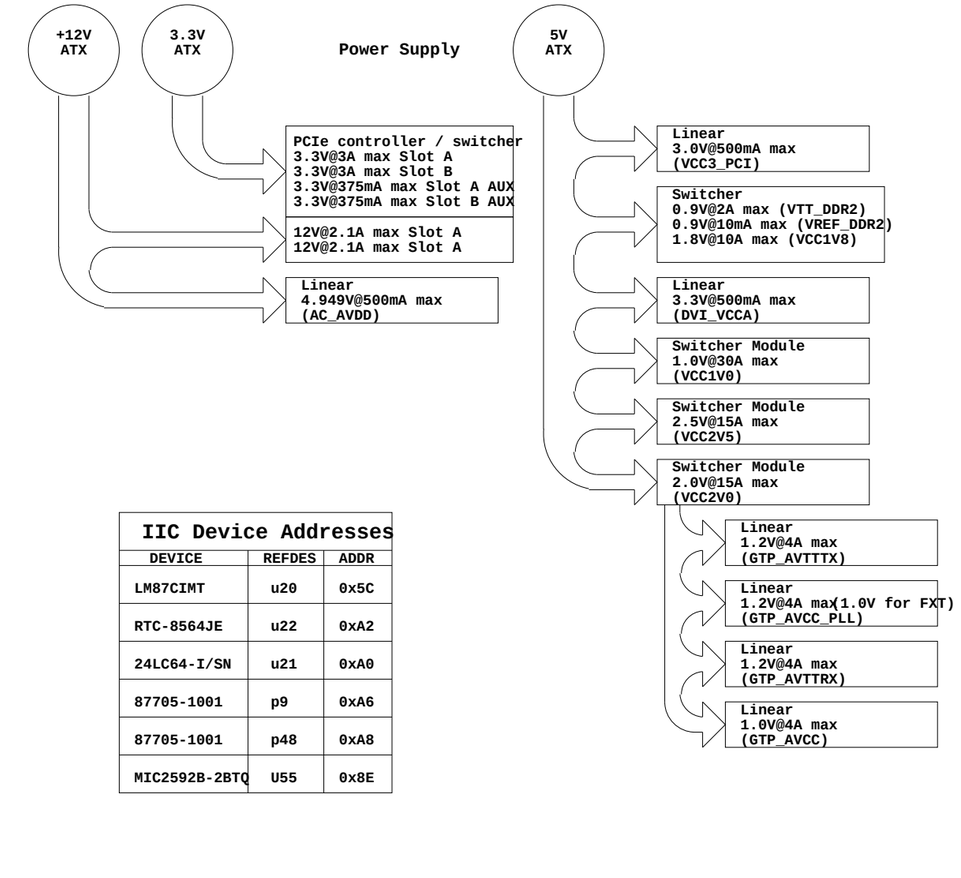
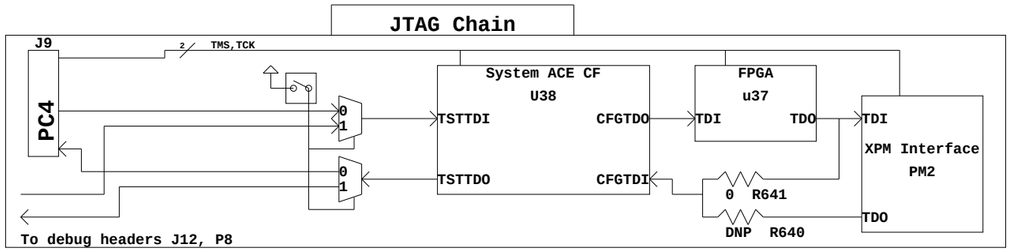




IIC Device Addresses

DEVICE	REFDES	ADDR
LM87CIMT	u20	0x5C
RTC-8564JE	u22	0xA2
24LC64-I/SN	u21	0xA0
87705-1001	p9	0xA6
87705-1001	p48	0xA8
MIC2592B-2BTQ	U55	0x8E



XILINX PART NUMBERS

SCHEMATICS	0381255
PCB ARTWORK	0532059
PCB FABRICATION	1280432

NOTE: PLEASE REVIEW THE ML510 BOM FOR ITEMS DESIGNATED AS "DNP".

DNP ITEMS ARE NOT POPULATED ON THE PCB.

THE ML510 BOM CONTAINS THE MOST ACCURATE INFORMATION ABOUT

DNP DISCRETES AND COMPONENTS

XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

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XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

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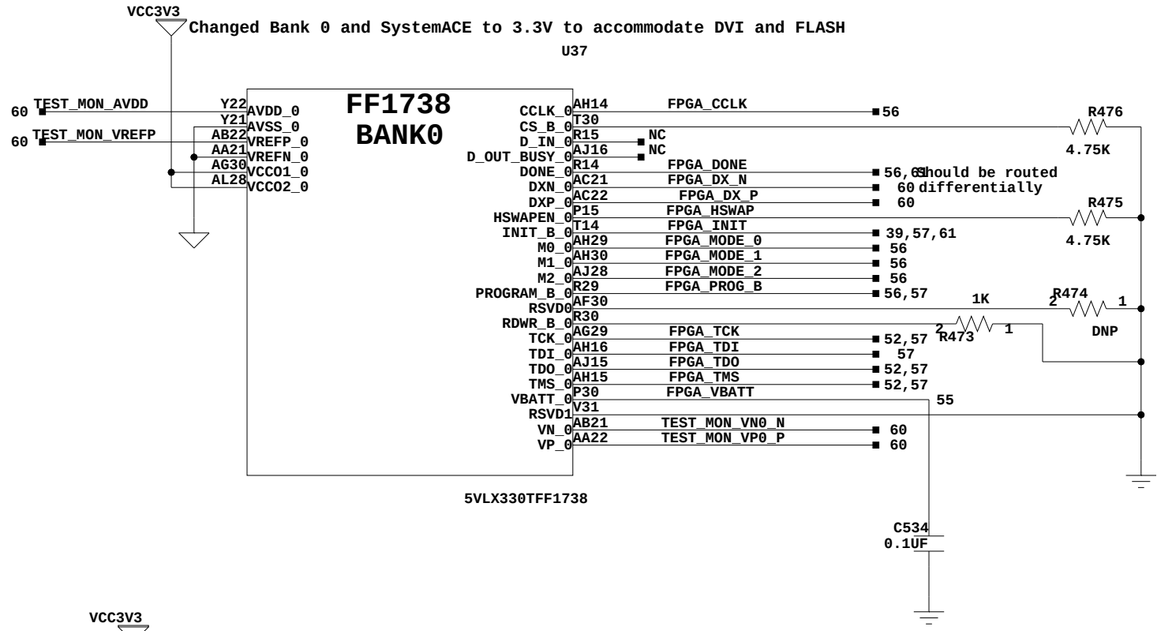
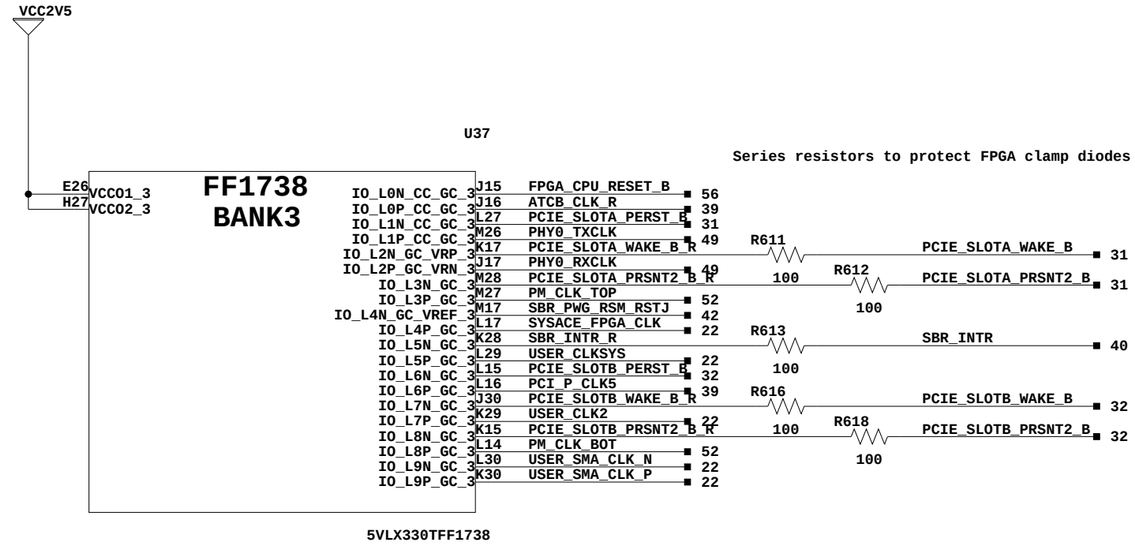
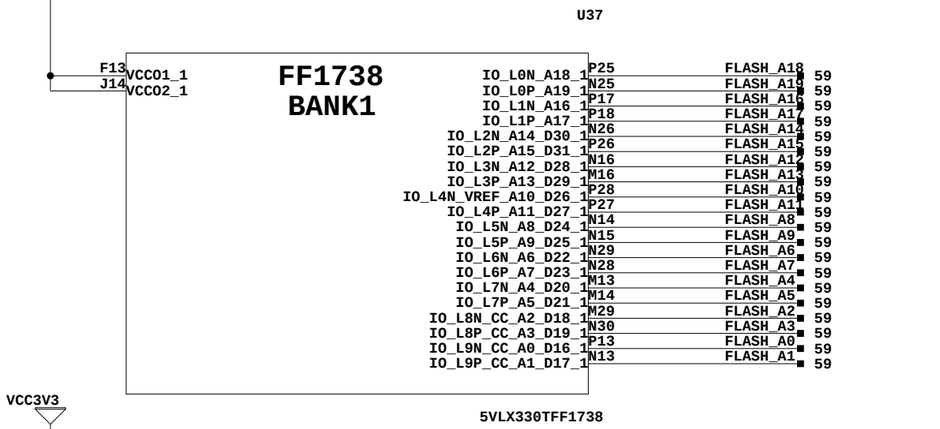
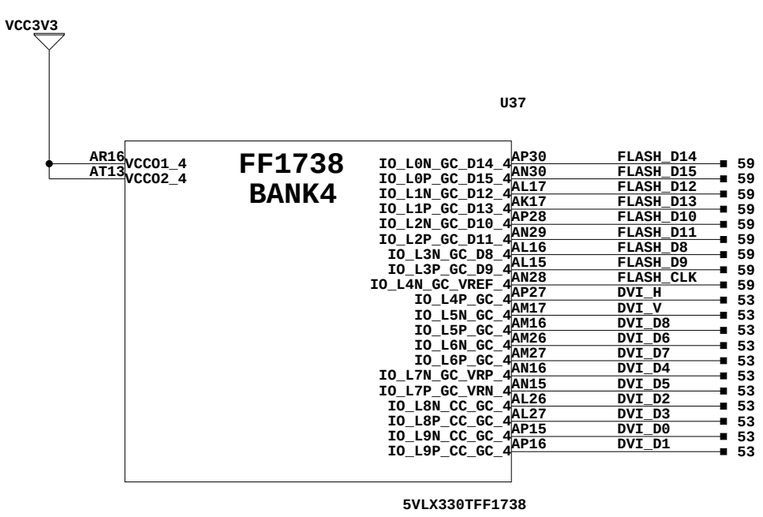
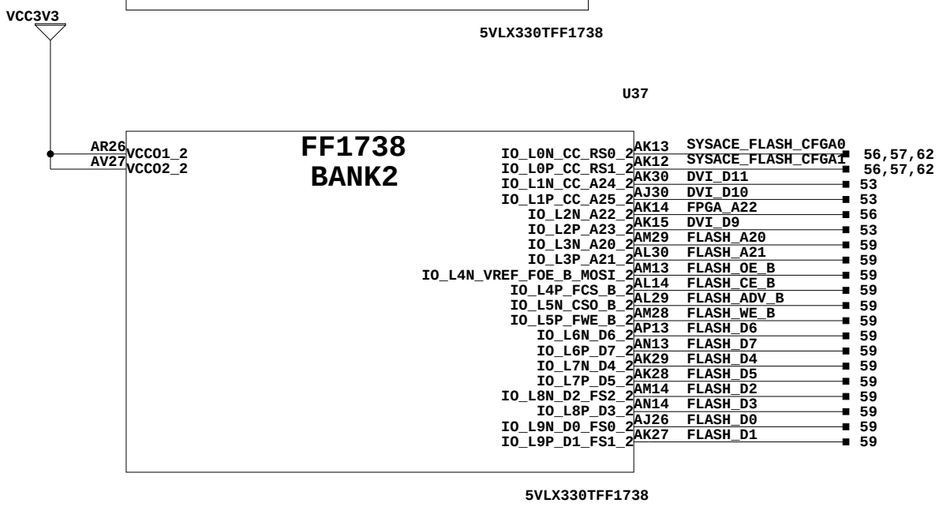
Changed Bank 0 and SystemACE to 3.3V to accommodate DVI and FLASH











FPGA - BANK 0, 1, 2, 3, 4

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA - BANK 0, 1, 2, 3, 4 - CONFIG, MISC, FLASH, CLOCKS, DVI

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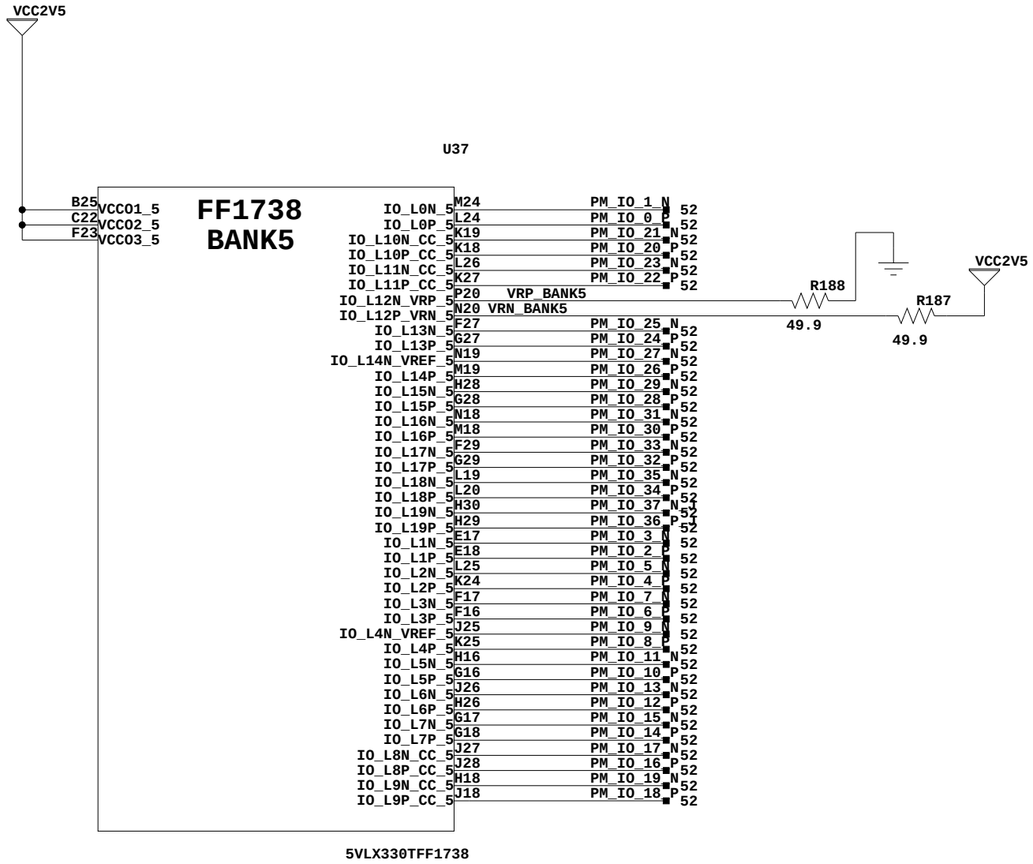

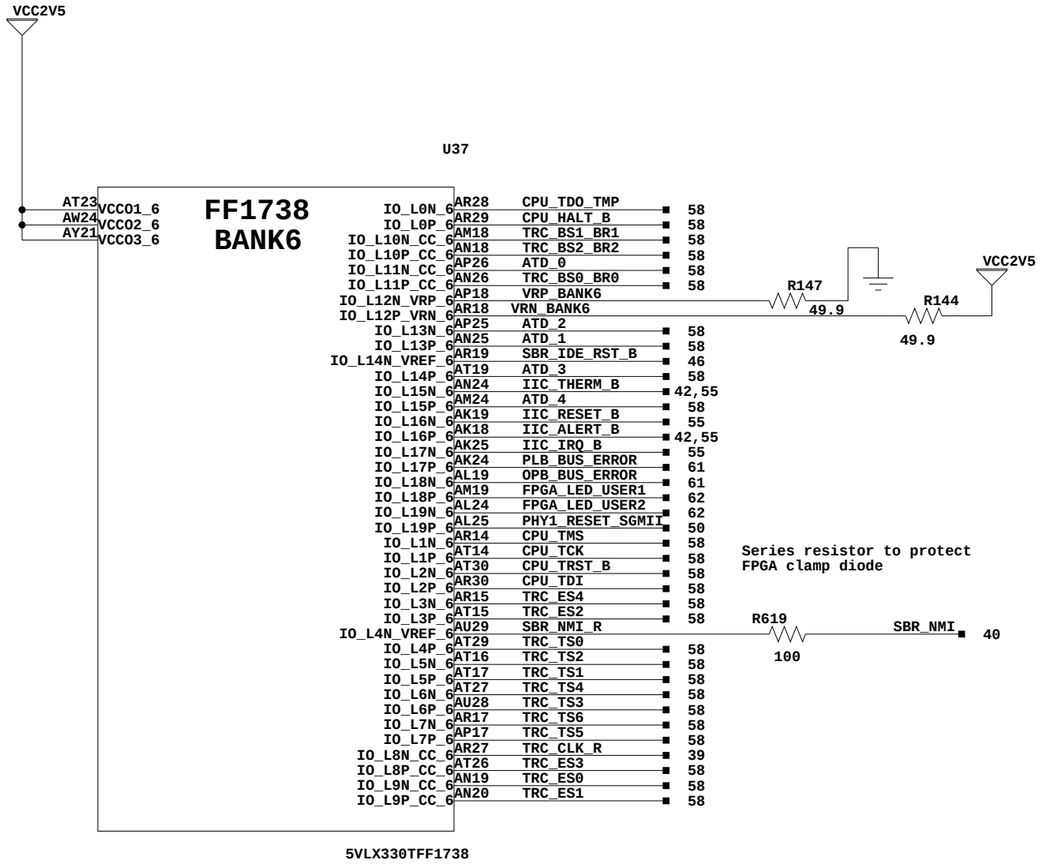

FPGA - BANK 5,6

XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA - BANK 5,6 - PM, DEBUG

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VCC1V8

AA38 VCCO1_11
V37 VCCO2_11
Y41 VCCO_11

U37

FF1738
BANK11

IO_L15N_SM13N_11	P40	DIMM0_DDR2_A1	25,26
IO_L15P_SM13P_11	AA42	DIMM0_DDR2_A0	25,26
IO_L10N_CC_SM15N_11	Y38	DIMM1_DDR2_PLL_CLKIN_N	29
IO_L10P_CC_SM15P_11	Y39	DIMM1_DDR2_PLL_CLKIN_P	29
IO_L7N_11	V41	DIMM1_DDR2_RAS_B	28,29
IO_L7P_11	V40	DIMM1_DDR2_WE_B	28,29
IO_L4P_11	W41	DIMM1_DDR2_A13	28,29
IO_L3N_11	Y42	DIMM1_DDR2_CAS_B	28,29
IO_L19N_SM9N_11	G41	DIMM1_DDR2_A11	28,29
IO_L3P_11	F41	DIMM1_DDR2_A12	28,29
IO_L14N_VREF_11	T41		
IO_L2N_11	W42	DIMM1_DDR2_A10	
IO_L1P_11	G42	DIMM1_DDR2_A8	28,29
IO_L1N_11	F42	DIMM1_DDR2_A9	28,29
IO_L11N_CC_SM14N_11	H41	DIMM1_DDR2_A6	28,29
IO_L2P_11	J42	DIMM1_DDR2_A7	28,29
IO_L12N_VRP_11	L42	DIMM1_DDR2_A4	28,29
IO_L11P_CC_SM14P_11	M42	DIMM1_DDR2_A5	28,29
IO_L12P_VRN_11	M41	DIMM1_DDR2_A2	28,29
IO_L14P_11	K42	DIMM1_DDR2_A3	28,29
IO_L5N_11	R40	DIMM1_DDR2_A0	28,29
IO_L0P_11	J41	DIMM1_DDR2_A1	28,29
IO_L13N_11	T42	DIMM0_DDR2_A3	25,26
IO_L13P_11	U41	DIMM0_DDR2_A2	25,26
IO_L19P_SM9P_11	T40	DIMM0_DDR2_A5	25,26
IO_L16N_SM12N_11	U42	DIMM0_DDR2_A4	25,26
IO_L18P_SM10P_11	R42	DIMM0_DDR2_A7	25,26
IO_L16P_SM12P_11	P41	DIMM0_DDR2_A6	25,26
IO_L4N_VREF_11	L41		
IO_L5P_11	P42	DIMM0_DDR2_A8	25,26
IO_L18N_SM10N_11	AA41	DIMM0_DDR2_A10	25,26
IO_L17N_SM11N_11	L40	DIMM0_DDR2_A9	25,26
IO_L6N_11	N41	DIMM0_DDR2_A12	25,26
IO_L17P_SM11P_11	N40	DIMM0_DDR2_A11	25,26
IO_L0N_11	AA37	DIMM0_DDR2_CAS_B	25,26
IO_L6P_11	Y37	DIMM0_DDR2_A13	25,26
IO_L8N_CC_11	Y40	DIMM0_DDR2_WE_B	25,26
IO_L8P_CC_11	W40	DIMM0_DDR2_RAS_B	25,26
IO_L9N_CC_11	AA39	DIMM0_DDR2_PLL_CLKIN_N	26
IO_L9P_CC_11	AA40	DIMM0_DDR2_PLL_CLKIN_P	26

VREF_DDR2
6,7,8,9,25,27,28,30,69

5VLX330TFF1738

5 VCCO_12

AA8 VCCO1_12
U10 VCCO2_12
V7 VCCO3_12

U37

FF1738
BANK12

IO_L0N_12	AA6	PM_IO_3V_10_N	52
IO_L0P_12	AA7	PM_IO_3V_4_P	52
IO_L10N_CC_12	N6	PM_IO_3V_17_N	52
IO_L10P_CC_12	N5	PM_IO_3V_5_P	52
IO_L11N_CC_12	U6	PM_IO_3V_9_N	52
IO_L11P_CC_12	U7	PM_IO_3V_13_P	52
IO_L12N_VRP_12	P6	VRP_BANK12	
IO_L12P_VRN_12	P5	VRN_BANK12	
IO_L13N_12	T6	PM_IO_3V_19_N	52
IO_L13P_12	T7	PM_IO_3V_24_P	52
IO_L14N_VREF_12	R5	FPGA_LCD_DB1	62
IO_L14P_12	R4	FPGA_LCD_DB0	62
IO_L15N_12	T4	FPGA_LCD_DB3	62
IO_L15P_12	T5	FPGA_LCD_DB2	62
IO_L16N_12	AA10	FPGA_LCD_DB5	62
IO_L16P_12	AA11	FPGA_LCD_DB4	62
IO_L17N_12	Y10	FPGA_LCD_DB7	62
IO_L17P_12	AA9	FPGA_LCD_DB6	62
IO_L18N_12	W10	FPGA_LCD_E	61,62
IO_L18P_12	W11	FLASH_WAIT	59
IO_L19N_12	Y8	FPGA_LCD_RS	61
IO_L19P_12	Y9	FPGA_LCD_RW	61,62
IO_L1N_12	H5	PM_IO_3V_21_N	52
IO_L1P_12	G6	PM_IO_3V_20_P	52
IO_L2N_12	W6	PM_IO_3V_15_N	52
IO_L2P_12	W5	PM_IO_3V_0_P	52
IO_L3N_12	J5	PM_IO_3V_8_N	52
IO_L3P_12	H6	PM_IO_3V_6_P	52
IO_L4N_VREF_12	W7	PM_IO_3V_23_N	52
IO_L4P_12	Y7	PM_IO_3V_11_P	52
IO_L5N_12	K5	PM_IO_3V_2_N	52
IO_L5P_12	J6	PM_IO_3V_14_P	52
IO_L6N_12	V8	PM_IO_3V_16_N	52
IO_L6P_12	W8	PM_IO_3V_12_P	52
IO_L7N_12	L5	PM_IO_3V_1_N	52
IO_L7P_12	K4	PM_IO_3V_3_P	52
IO_L8N_CC_12	V6	PM_IO_3V_25_N	52
IO_L8P_CC_12	V5	PM_IO_3V_18_P	52
IO_L9N_CC_12	M6	PM_IO_3V_7_N	52
IO_L9P_CC_12	L6	PM_IO_3V_22_P	52

R179
R166
49.9
49.9
VCCO_12
5

5VLX330TFF1738

VCC3_PCI
R486
0
VCCO_12
5

VCC3_PCI
R487
0
VCCO_12
5

VCC3_PCI
R488
0
VCCO_12
5

VCC2V5
R491
0-DNP
VCCO_12
5

VCC2V5
R490
0-DNP
VCCO_12
5

VCC2V5
R489
0-DNP
VCCO_12
5

FPGA - BANK 11,12

XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA - BANK 11,12 DDR2, PM, LCD

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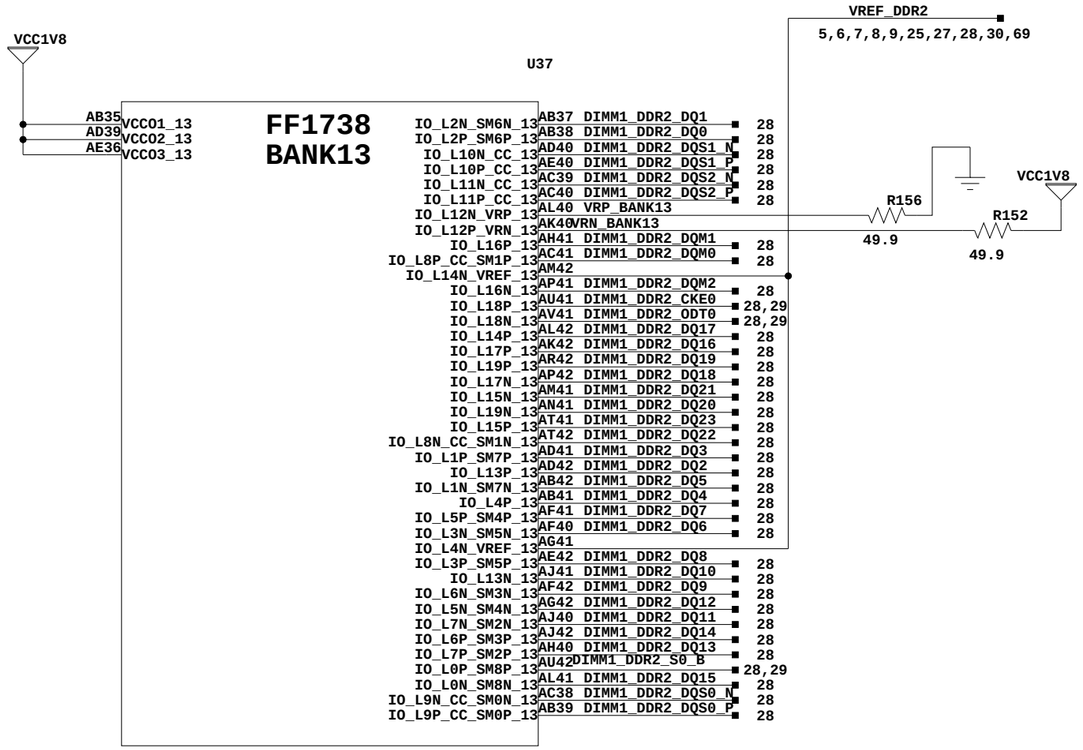

FPGA - BANK 13,15

XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA - BANK 13,15 - DDR2

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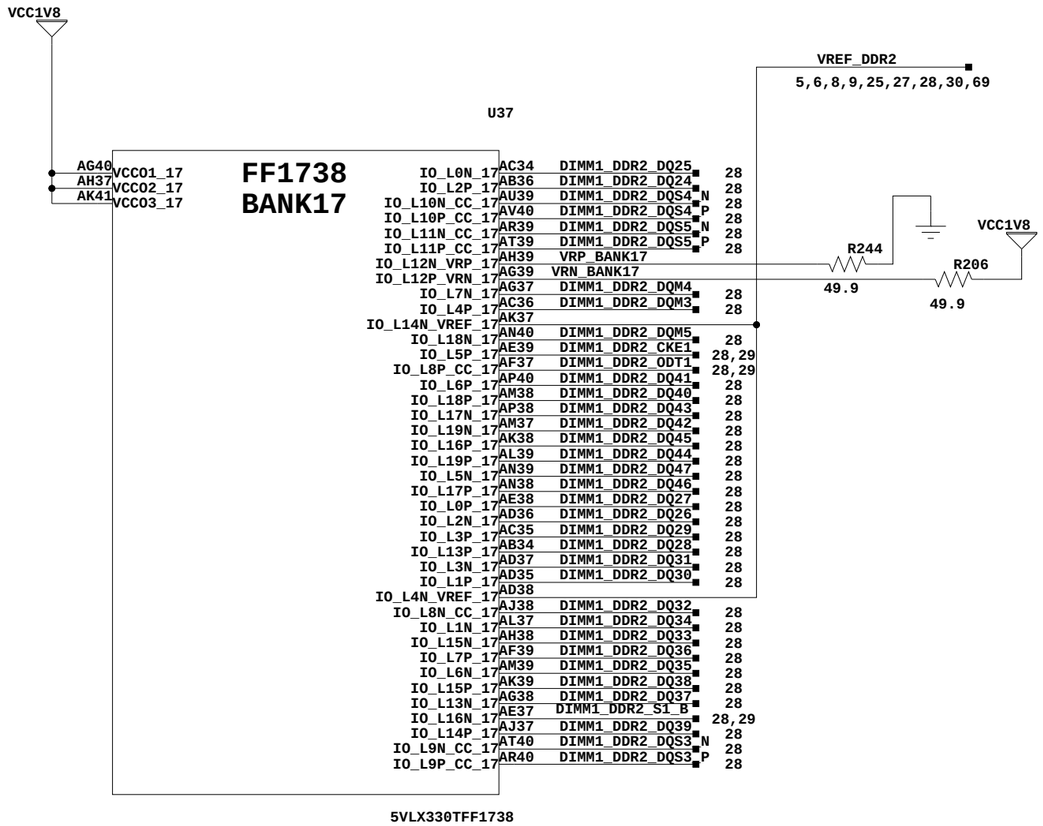

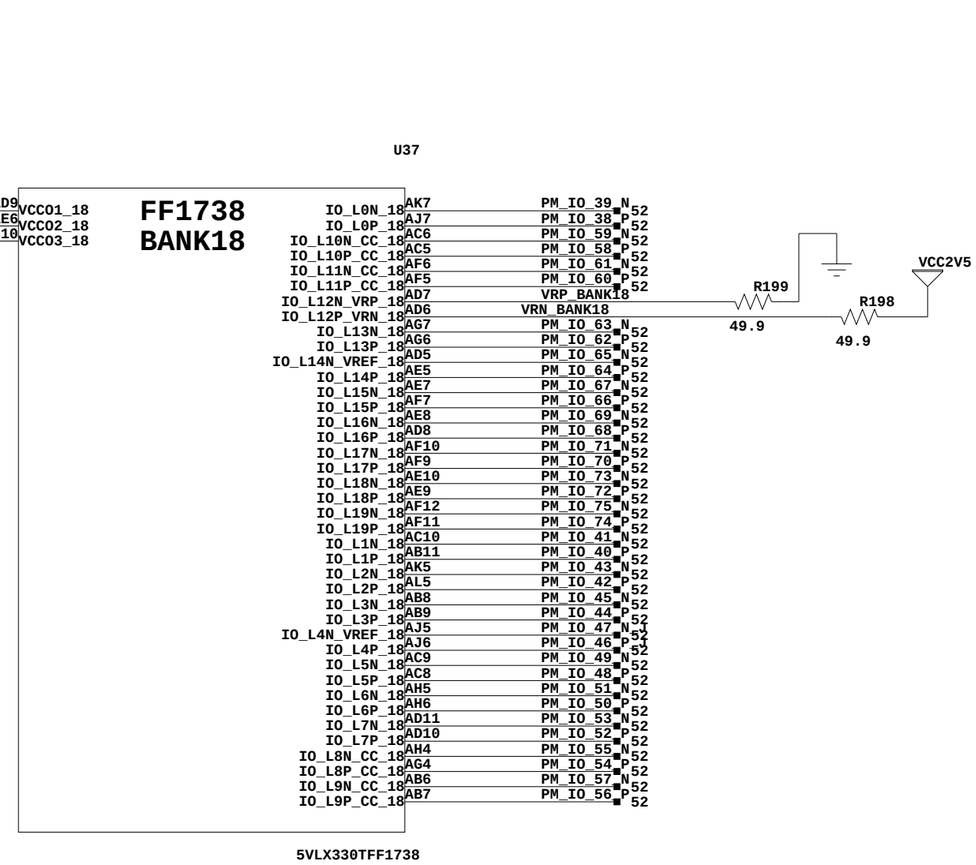

FPGA - BANK 17,18

XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA - BANK 17,18 - DDR2, PM

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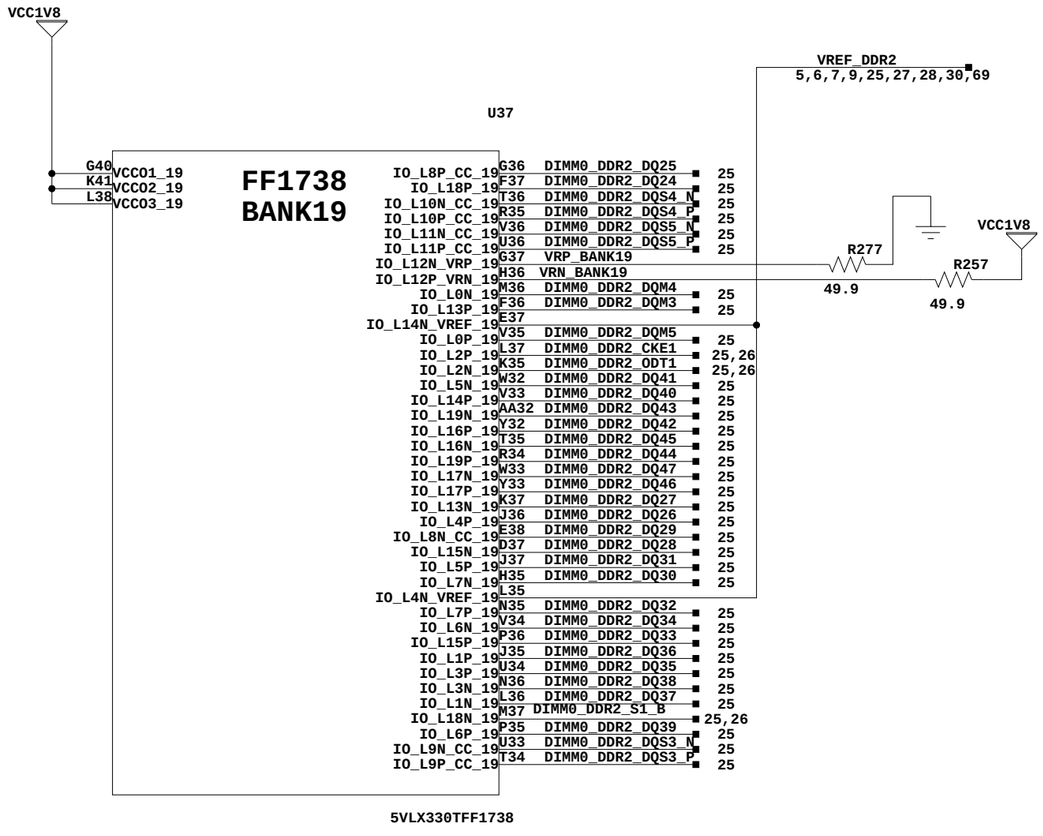

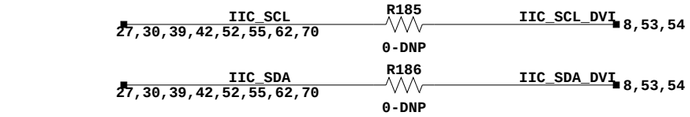

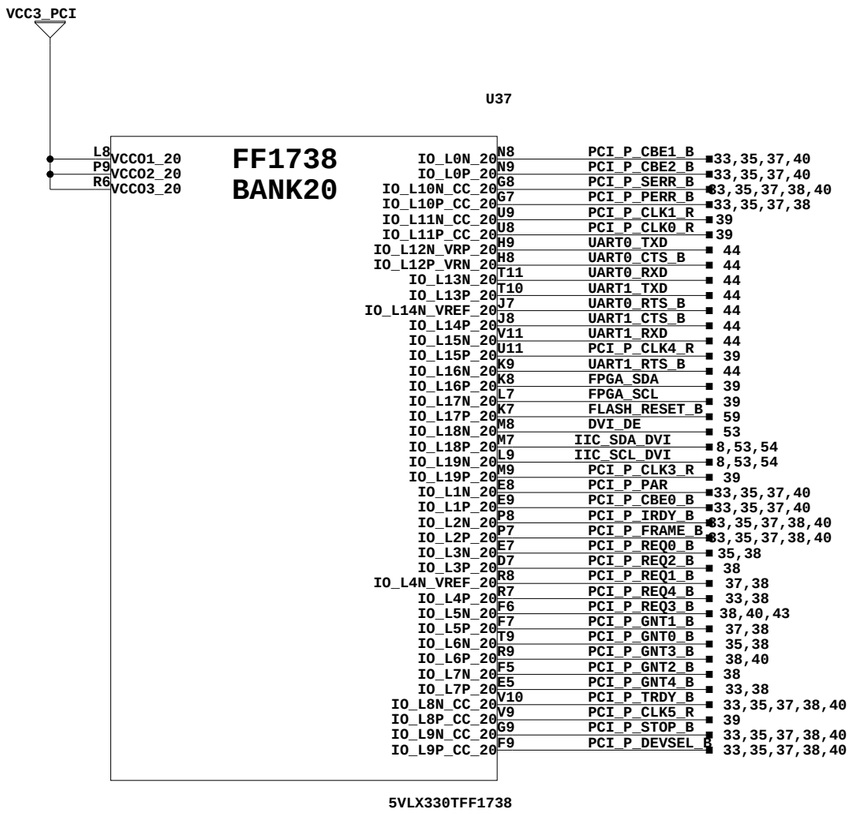

FPGA - BANK 19,20

XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA - BANK 19,20 DDR2, PCI, IIC, UART

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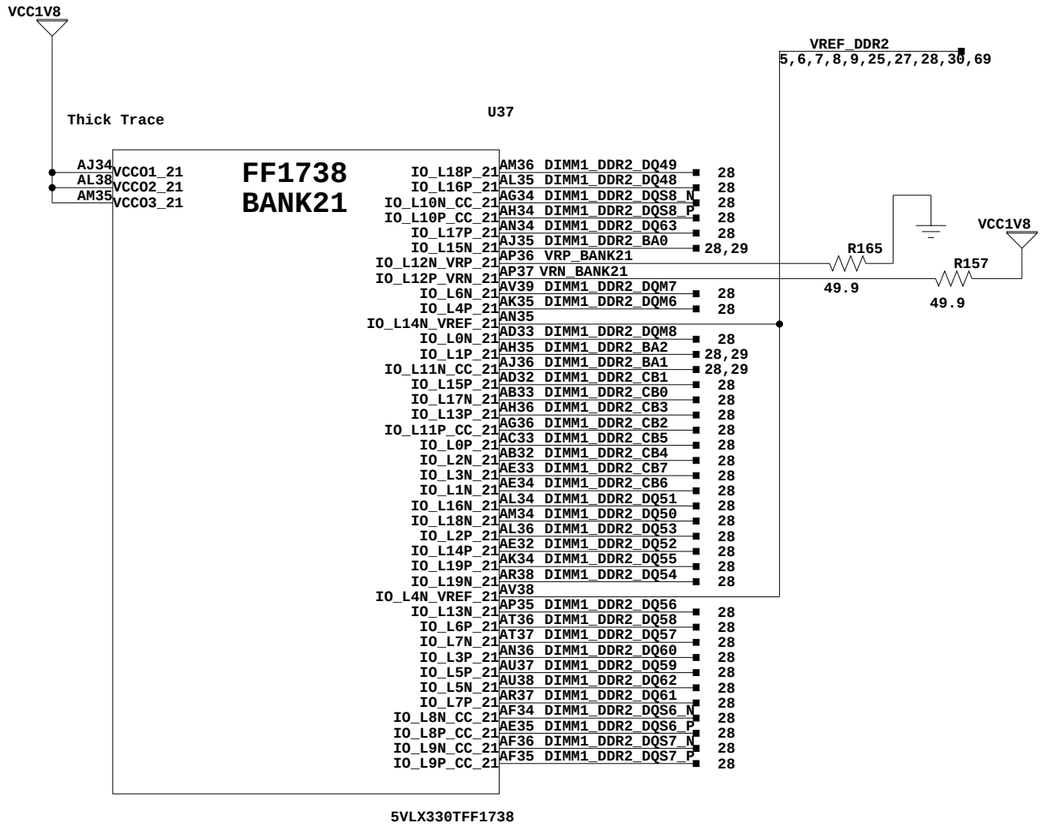

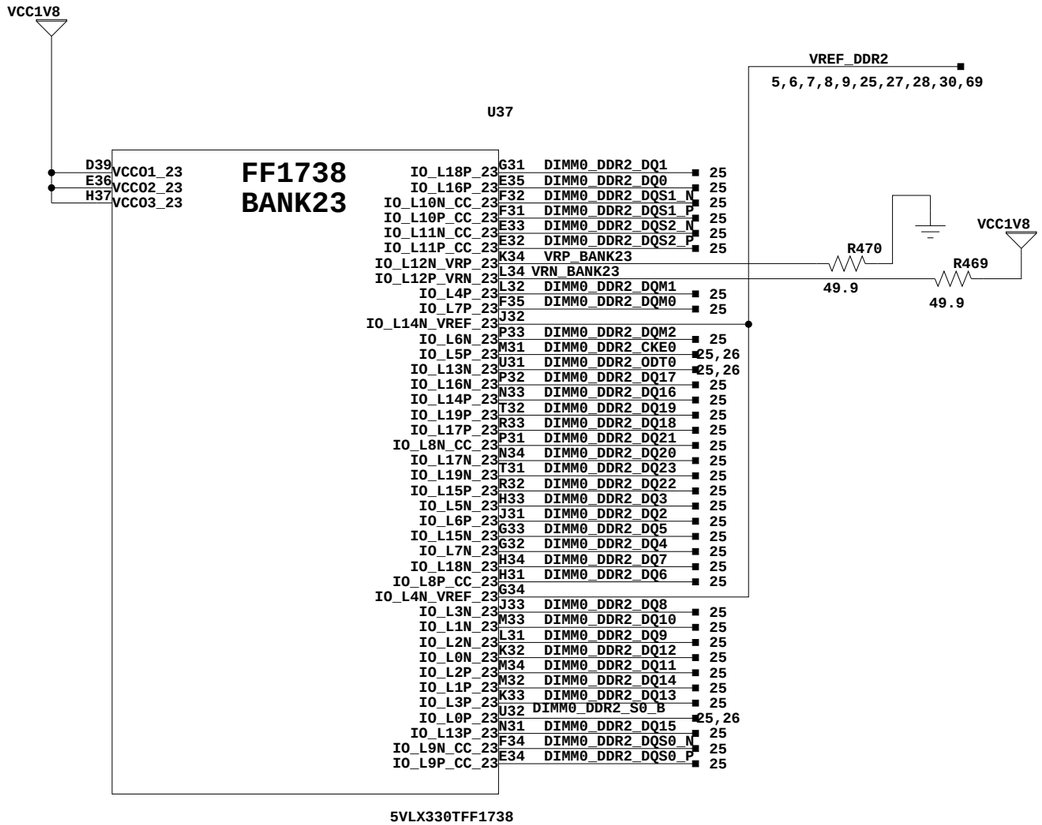

FPGA - BANK 21,23

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA - BANK 21,23 DDR2

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VCC3_PCI

U37

FF1738
BANK24

E6	VCCO1_24		
G10	VCCO2_24		
H7	VCCO3_24		
IO_L0N_24	H11	PCI_P_RST_B	
IO_L0P_24	J12	PCI_P_LOCK_B	33,35,37,38
IO_L10N_CC_24	L11	PCI_P_AD17	33,35,37,38
IO_L10P_CC_24	L12	PCI_P_AD18	33,35,37,40
IO_L11N_CC_24	G14	PCI_P_AD15	33,35,37,40
IO_L11P_CC_24	G13	PCI_P_AD16	33,35,37,40
IO_L12N_VRP_24	M12	PCI_P_AD13	33,35,37,40
IO_L12P_VRN_24	M11	PCI_P_AD14	33,35,37,40
IO_L13N_24	E13	PCI_P_AD11	33,35,37,40
IO_L13P_24	F14	PCI_P_AD12	33,35,37,40
IO_L14N_VREF_24	P12	PCI_P_AD9	33,35,37,40
IO_L14P_24	N11	PCI_P_AD10	33,35,37,40
IO_L15N_24	D12	PCI_P_AD7	33,35,37,40
IO_L15P_24	E12	PCI_P_AD8	33,35,37,40
IO_L16N_24	N10	PCI_P_AD5	33,35,37,40
IO_L16P_24	P11	PCI_P_AD6	33,35,37,40
IO_L17N_24	E14	PCI_P_AD3	33,35,37,40
IO_L17P_24	D13	PCI_P_AD4	33,35,37,40
IO_L18N_24	P10	PCI_P_AD1	33,35,37,40
IO_L18P_24	R10	PCI_P_AD2	33,35,37,40
IO_L19N_24	F15	PCI_P_CBE3_B	33,35,37,40
IO_L19P_24	E15	PCI_P_AD0	33,35,37,40
IO_L1N_24	G11	PCI_P_INTB_B	34,35,36,37,38,40
IO_L1P_24	G12	PCI_P_INTA_B	34,35,36,37,38,40
IO_L2N_24	F11	PCI_P_INTD_B	34,35,36,37,38,40
IO_L2P_24	F12	PCI_P_INTC_B	34,35,36,37,38,40
IO_L3N_24	F10	PCI_P_AD31	33,35,37,40
IO_L3P_24	E10	PCI_FPGA_IDSEL	39
IO_L4N_VREF_24	K13	PCI_P_AD29	33,35,37,40
IO_L4P_24	K14	PCI_P_AD30	33,35,37,40
IO_L5N_24	J11	PCI_P_AD27	33,35,37,40
IO_L5P_24	K12	PCI_P_AD28	33,35,37,40
IO_L6N_24	H13	PCI_P_AD25	33,35,37,40
IO_L6P_24	J13	PCI_P_AD26	33,35,37,40
IO_L7N_24	J10	PCI_P_AD23	33,35,37,40
IO_L7P_24	H10	PCI_P_AD24	33,35,37,39,40
IO_L8N_CC_24	H15	PCI_P_AD21	33,35,37,40
IO_L8P_CC_24	H14	PCI_P_AD22	33,35,37,40
IO_L9N_CC_24	L10	PCI_P_AD19	33,35,37,40
IO_L9P_CC_24	K10	PCI_P_AD20	33,35,37,40

5VLX330TFF1738

VCC2V5

U37

FF1738
BANK25

AP39	VCCO1_25		
AR36	VCCO2_25		
AU40	VCCO3_25		
IO_L0N_25	AF31	PM_IO_77_N	52
IO_L0P_25	AG31	PM_IO_76_P	52
IO_L10N_CC_25	AU31	PHY1_MDC	50
IO_L10P_CC_25	AV31	PHY1_INT_SGMII	50
IO_L11N_CC_25	AT31	PHY0_TXER	49
IO_L11P_CC_25	AT32	PHY1_MDIO	50
IO_L12N_VRP_25	AN31	PHY0_TXD3	49
IO_L12P_VRN_25	AP31	PHY0_TXCTL_TXEN	49
IO_L13N_25	AP32	PHY0_TXD1	49
IO_L13P_25	AR32	PHY0_TXD2	49
IO_L14N_VREF_25	AP33	PHY0_RXER	49
IO_L14P_25	AR33	PHY0_TXD0	49
IO_L15N_25	AM33	PHY0_RXD3	49
IO_L15P_25	AN33	PHY0_RXCTL_RXDV	49
IO_L16N_25	AJ33	PHY0_RXD1	49
IO_L16P_25	AK33	PHY0_RXD2	49
IO_L17N_25	AK32	PHY0_RESET	49
IO_L17P_25	AJ32	PHY0_RXD0	49
IO_L18N_25	AM32	PHY0_MDC	49
IO_L18P_25	AL32	PHY0_INT	49
IO_L19N_25	AM31	PHY0_GTXCLK	49
IO_L19P_25	AL31	PHY0_MDIO	49
IO_L1N_25	AG33	PM_IO_79_N	52
IO_L1P_25	AF32	PM_IO_78_P	52
IO_L2N_25	AG32	PM_IO_81_N	52
IO_L2P_25	AH33	PM_IO_80_P	52
IO_L3N_25	AJ31	PM_IO_83_N	52
IO_L3P_25	AH31	PM_IO_82_P	52
IO_L4N_VREF_25	AV36	PM_IO_85_N	52
IO_L4P_25	AV35	PM_IO_84_P	52
IO_L5N_25	AT35	PM_IO_87_N	52
IO_L5P_25	AU36	PM_IO_86_P	52
IO_L6N_25	AT34	PM_IO_89_N	52
IO_L6P_25	AU34	PM_IO_88_P	52
IO_L7N_25	AR34	PM_IO_91_N	52
IO_L7P_25	AR35	PM_IO_90_P	52
IO_L8N_CC_25	AU33	PM_IO_93_N	52
IO_L8P_CC_25	AU32	PM_IO_92_P	52
IO_L9N_CC_25	AV34	PM_IO_95_N	52
IO_L9P_CC_25	AV33	PM_IO_94_P	52

5VLX330TFF1738

FPGA - BANK 24,25

XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA - BANK 24,25 PCI, PERSONALITY MODULE, PHY

Date: 8-1-2008_15:03	Ver: C
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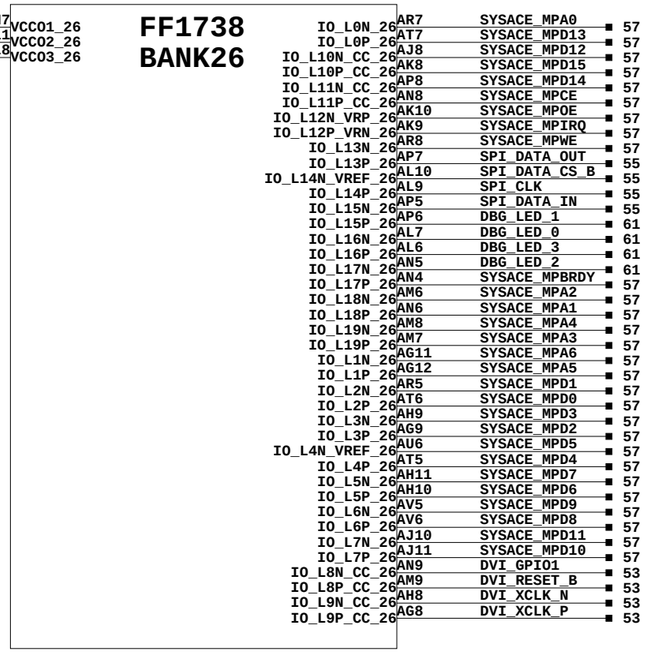
Sheet 10 of 70	Drawn By BF

VCC3V3

U37



FPGA - BANK 26

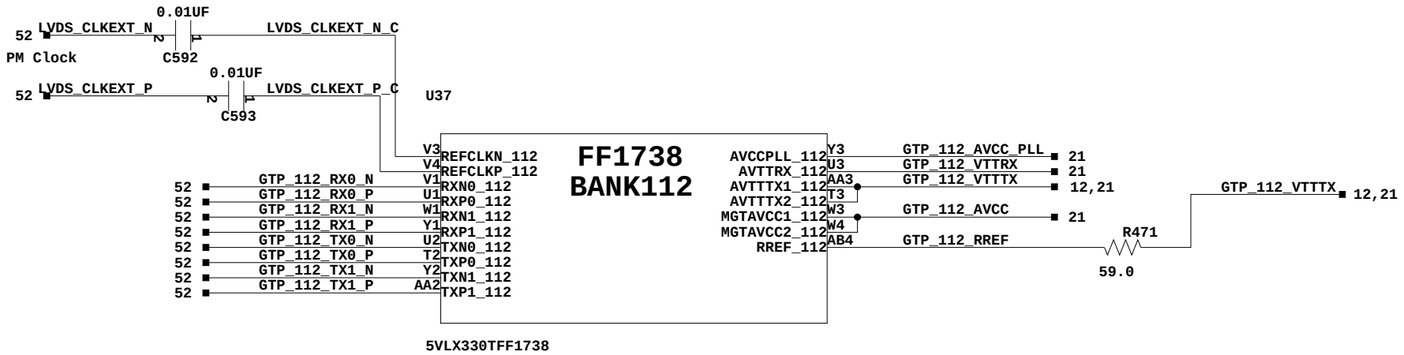
XILINX

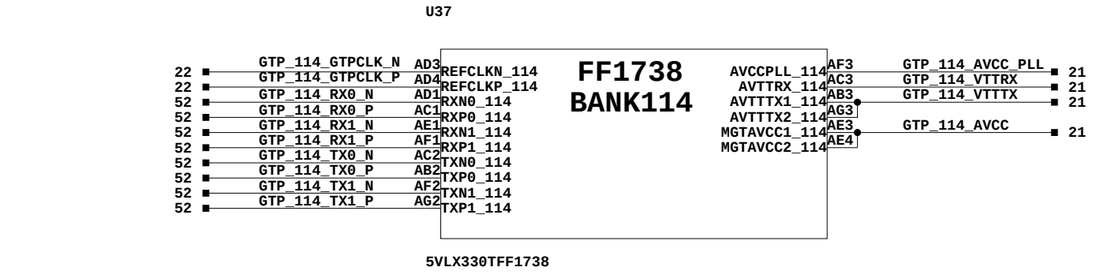
SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

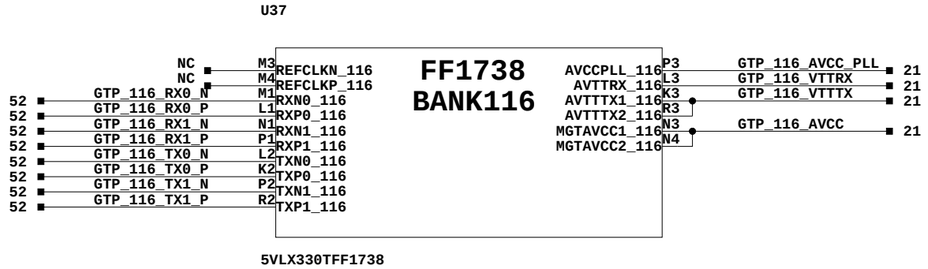
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA - BANK 26 SYSTEM ACE, DVI, SPI, LEDS

Date: 8-1-2008_15:03	Ver: C
Sheet Size: B	Rev: 01
Sheet 11 of 70	Drawn By BF







PM

PM

PM

FPGA - BANK 112, 114, 116

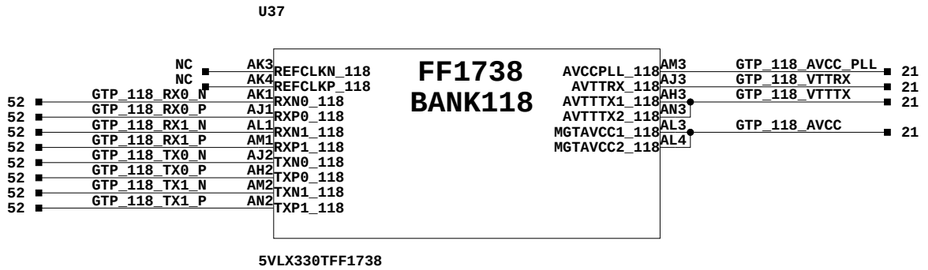
XILINX

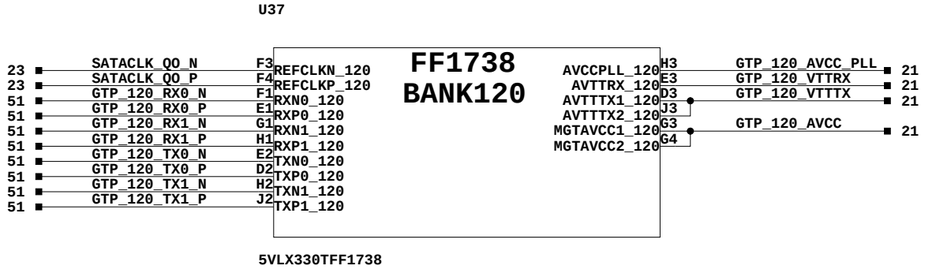
SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

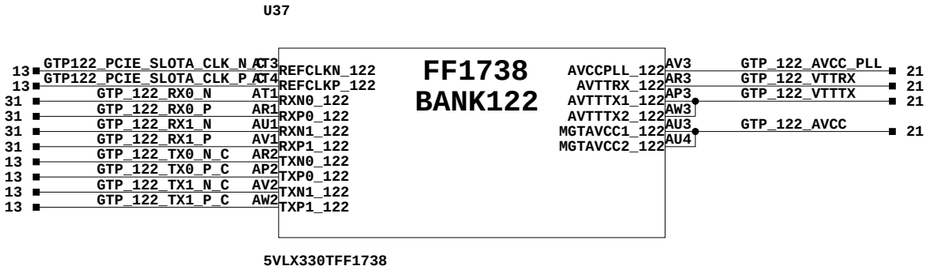
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

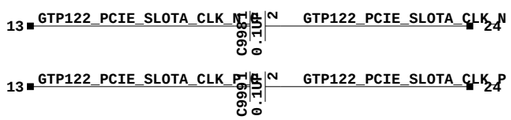
FPGA-BANK 112, 114, 116 PERSONALITY MODULES

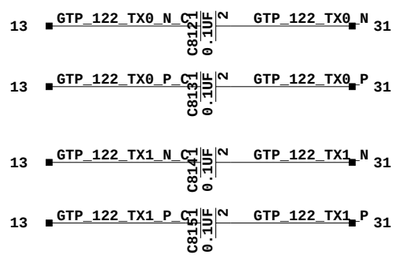
Date: 8-1-2008_15:03	Ver: C
Sheet Size: B	Rev: 01
Sheet 12 of 70	Drawn By BF











PM

SATA
SATA Clock

PCIe Slot A

FPGA - BANK 118,120,122

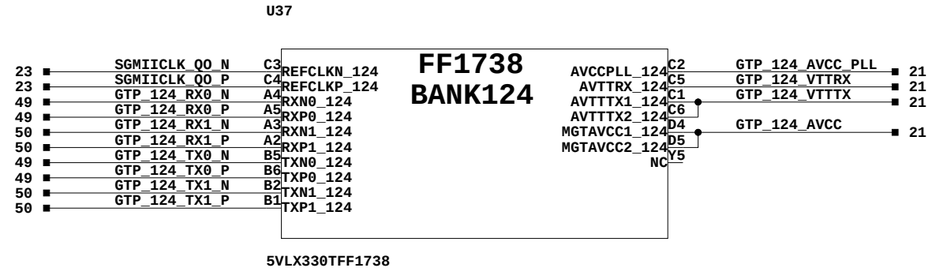
XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

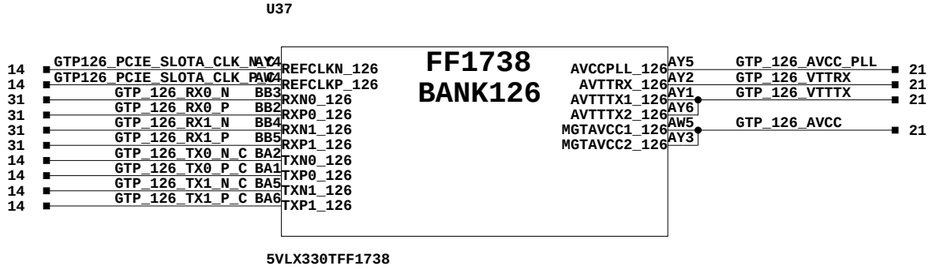
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA - BANK 118,120,122 PM, SATA, PCI-E

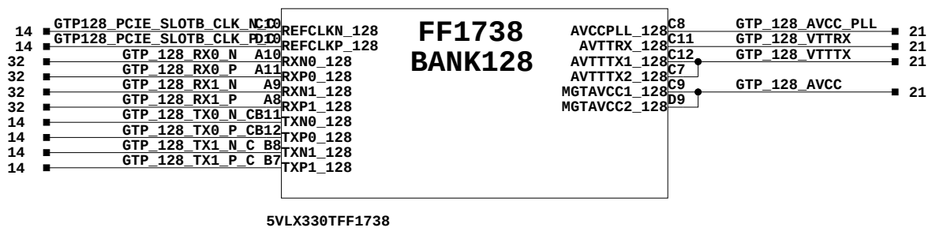
Date:	8-1-2008_15:03	Ver:	C
Sheet Size: B		Rev:	01
Sheet	13 of 70	Drawn By	BF



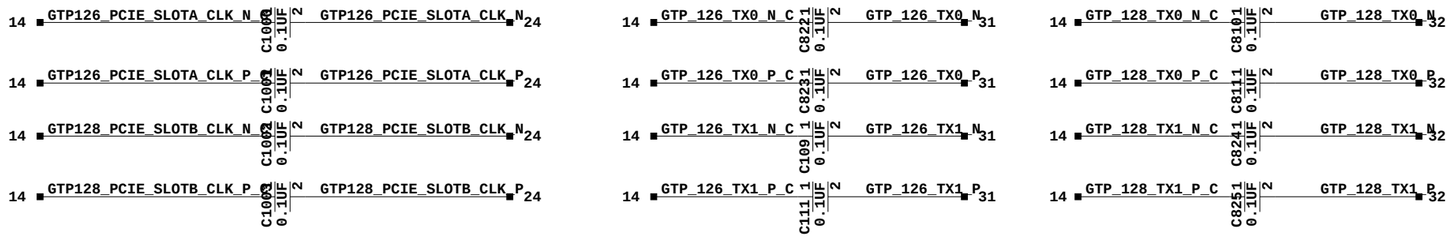
SGMII



PCIe Slot A



PCIe Slot B
(FX130T / FX200T / LX330T only)



FPGA - BANK 124,126,128

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA - BANK 124,126,128 SGMII, PCI-E

Date:	8-1-2008_15:03	Ver:	C
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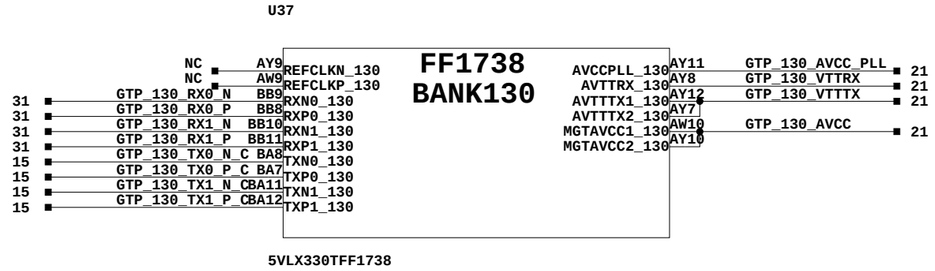
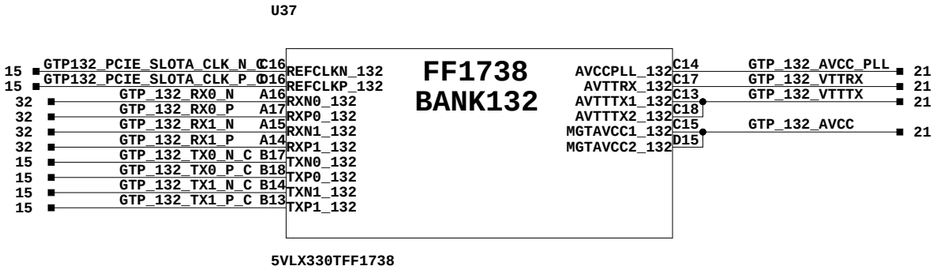
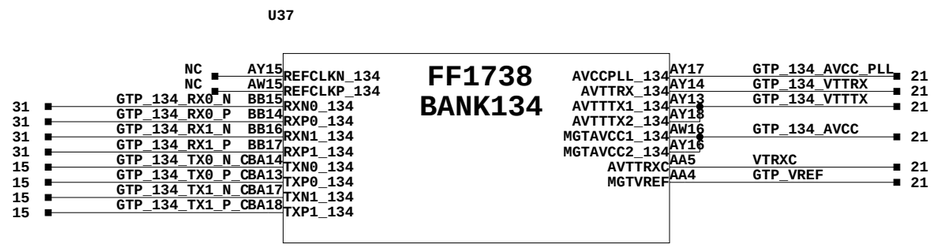


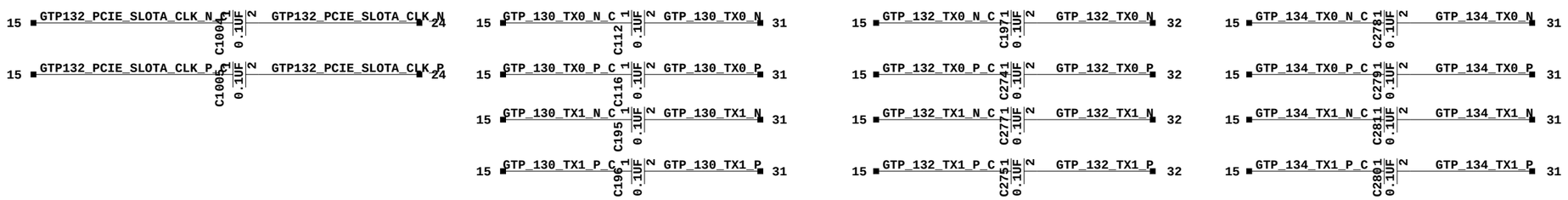
PCIe Slot A
(FX130T / FX200T / LX330T only)



PCIe Slot B
(FX200T / LX330T only)



PCIe Slot A
(FX200T / LX330T only)



FPGA - BANK 130,132,134

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA - BANK 130,132,134 PCI-E

Date:	8-1-2008_15:03	Ver:	C
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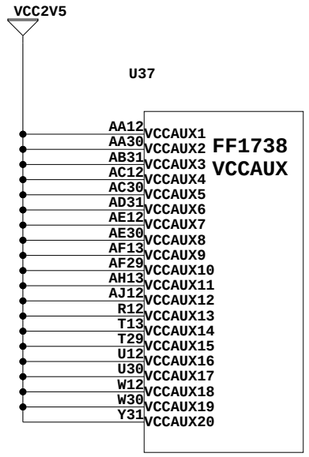

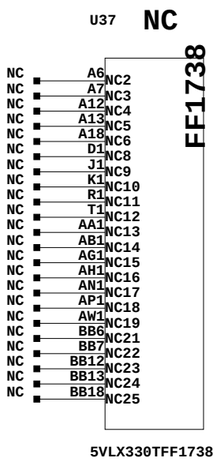

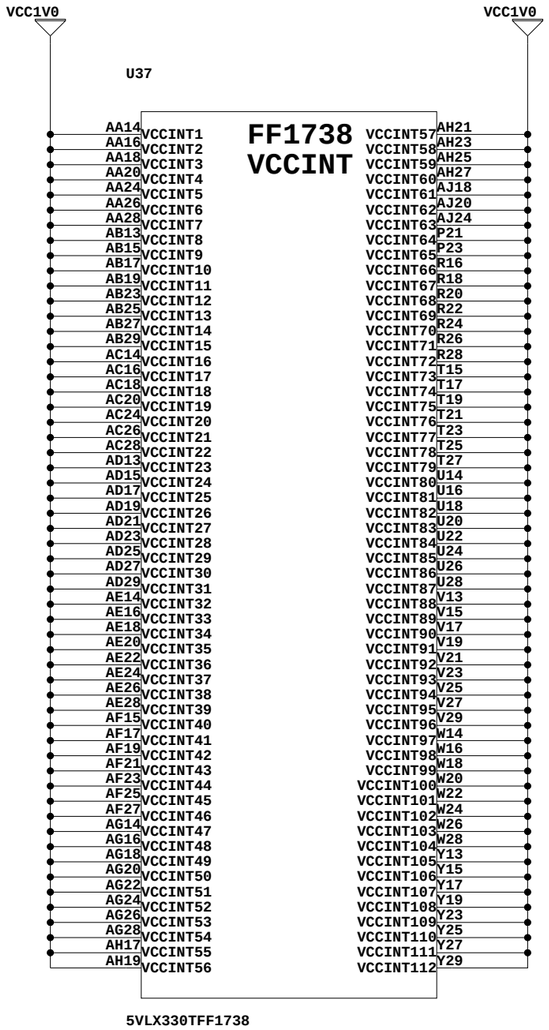

FPGA - VCCAUX, VCCINT, NC

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA - VCCAUX, VCCINT, NC

Date:	8-1-2008_15:04	Ver:	C
Sheet Size: B		Rev:	01
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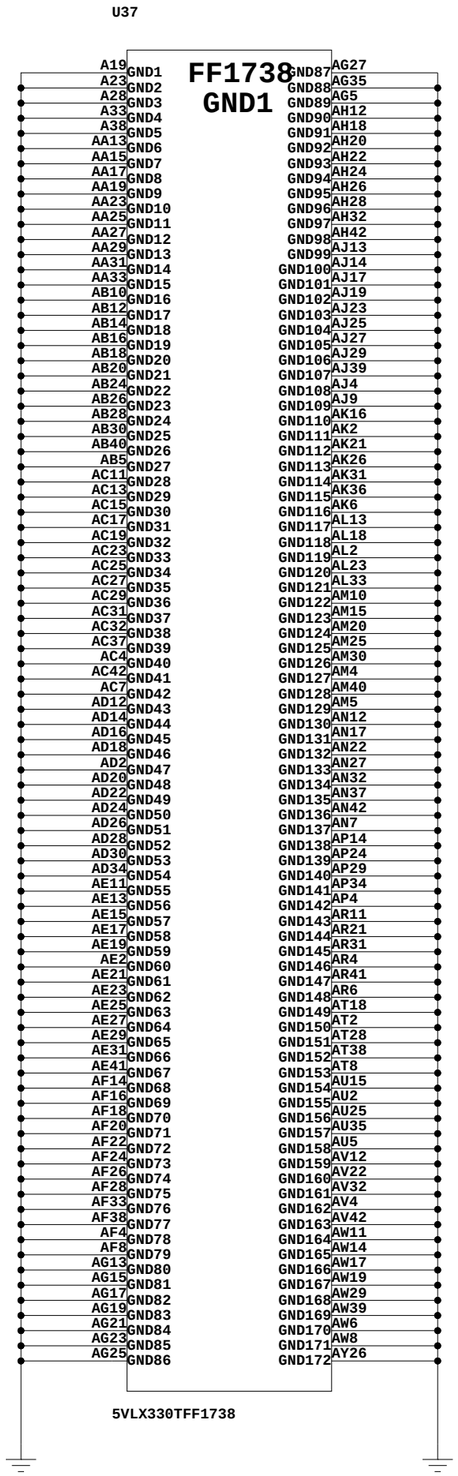

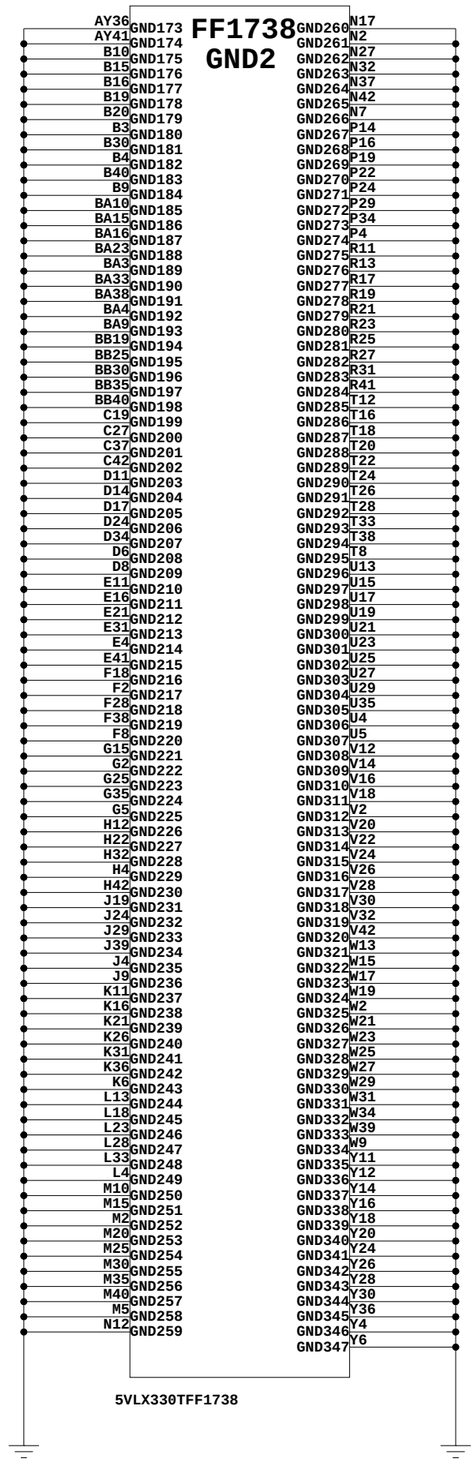

FPGA - GND

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA GROUND PINS

Date:	7-10-2008_10:19	Ver:	C
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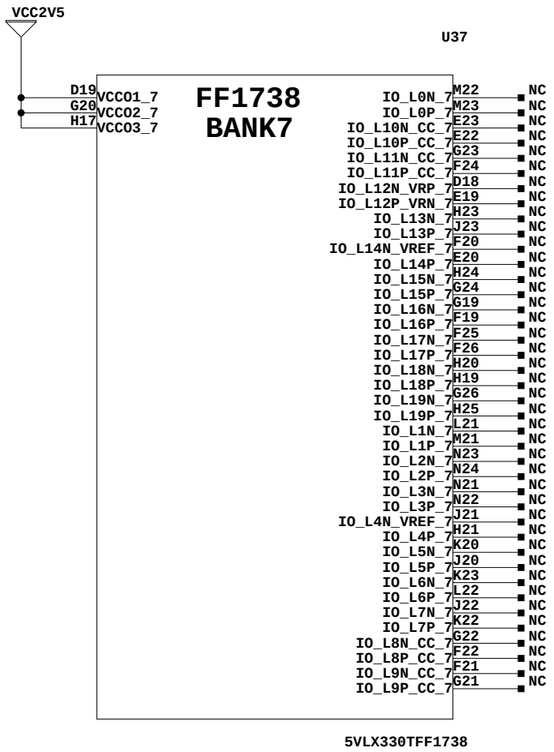

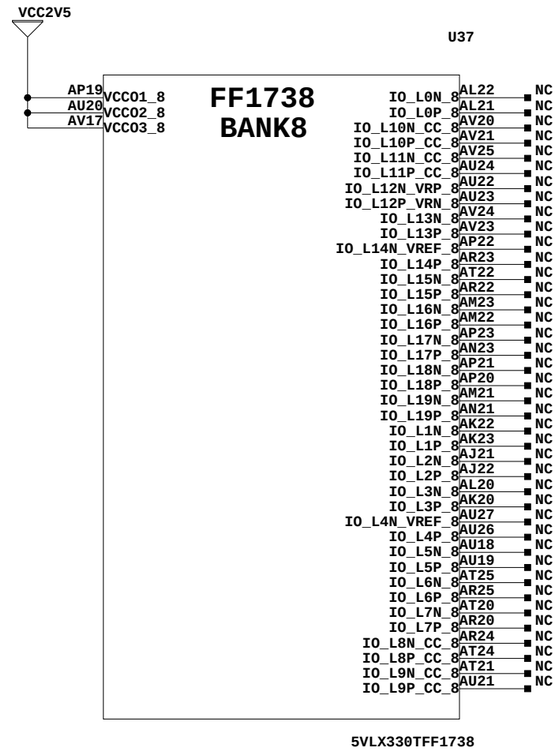

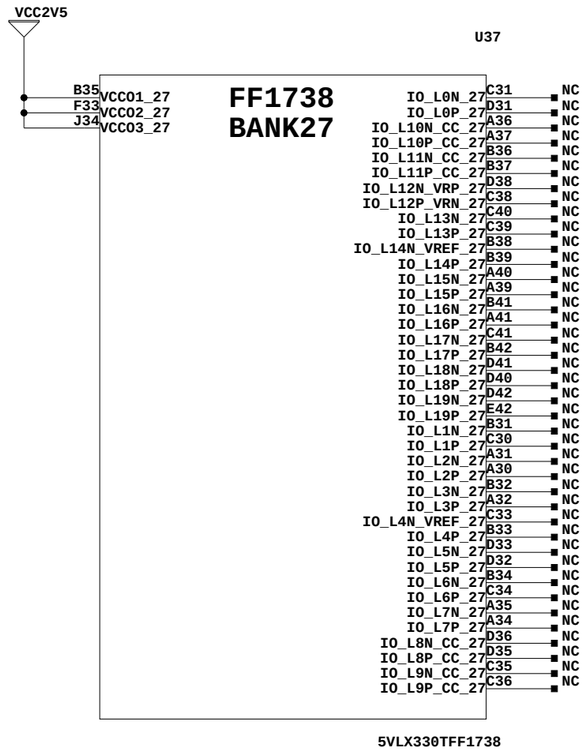

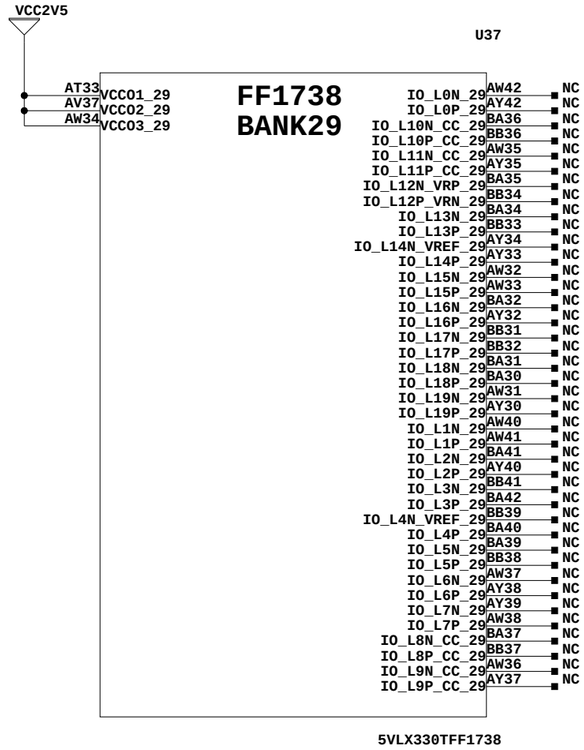

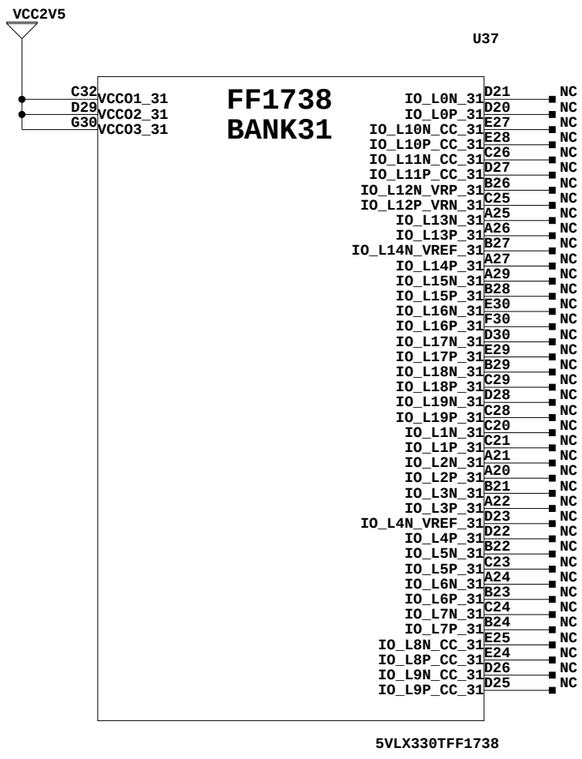

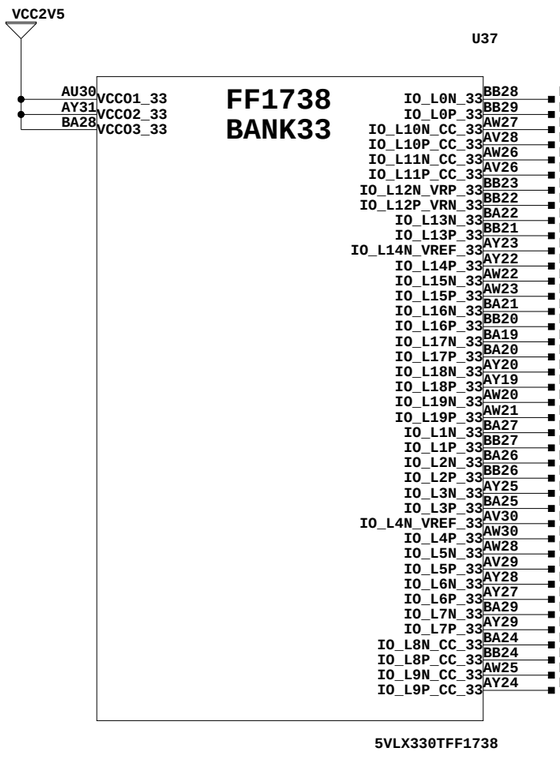

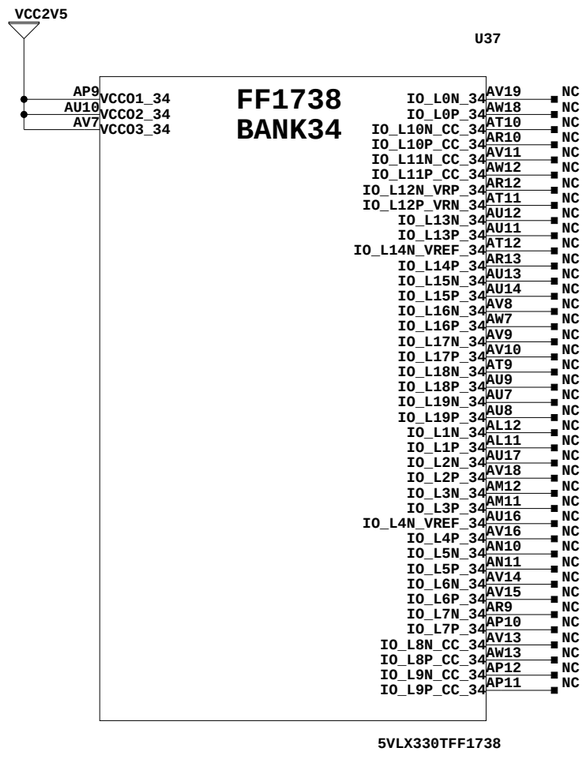

FPGA - BANK 7,8,27,29,31,33,34

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
FPGA - BANK 7,8,27,29,31,33,34 UNUSED BANKS

Date:	7-10-2008_10:19	Ver:	C
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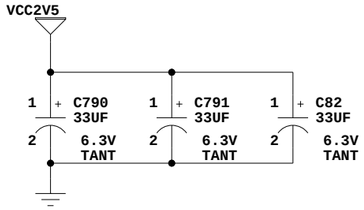
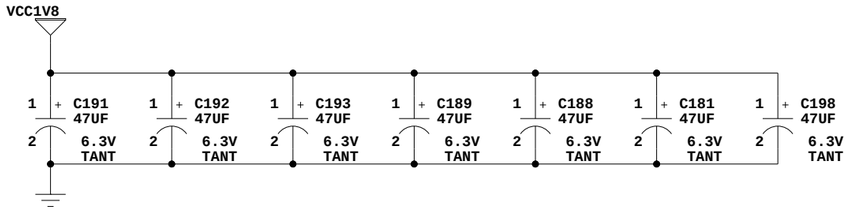
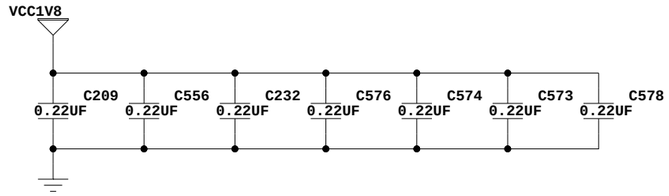
VCCAUX 2.5V

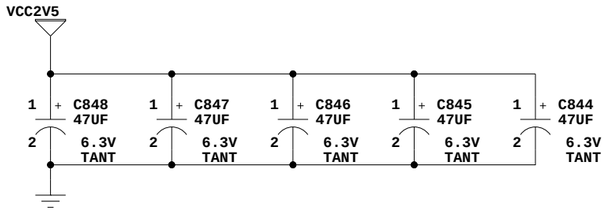


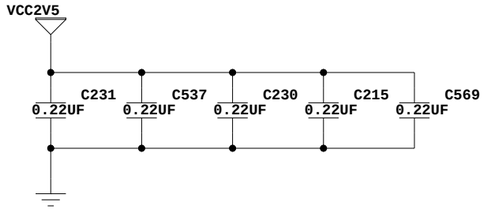
VCCO 1.8V



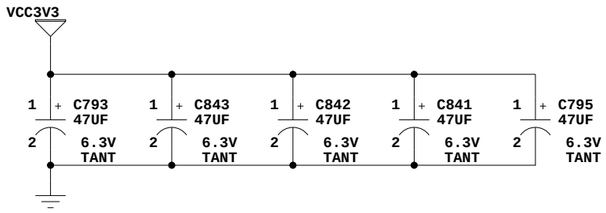


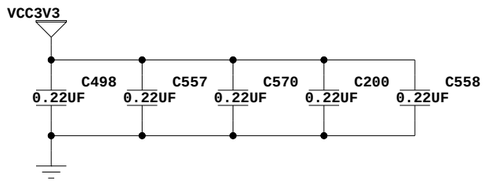
VCCO 2.5V



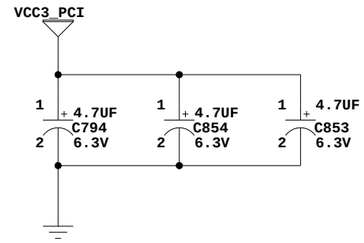


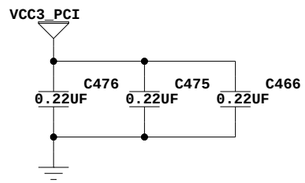
VCCO 3.3V





VCCO 3.0V PCI





Supply	Banks Used	Capacitors Used
VCCAUX 2.5V	N/A	33uf: 3
VCCINT 1.0V	N/A	330uf: 7 / 0.22uf: 52
VCCO 3.3V	0,1,2,4,26	47uf: 5 / 0.22uf: 5
VCCO 2.5V	3,5,6,18,25	47uf: 5 / 0.22uf: 5
VCCO 1.8V	11,13,15,17,19,21,23	47uf: 7 / 0.22uf: 7
VCCO 3.0V PCI	12,20,24	47uf: 3 / 0.22uf: 3

Note: Bank 12 defaults to 3.0V_PCI

FPGA DECOUPLING

XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA DECOUPLING

Date: 7-10-2008_10:19	Ver: C
Sheet Size: B	Rev: 01
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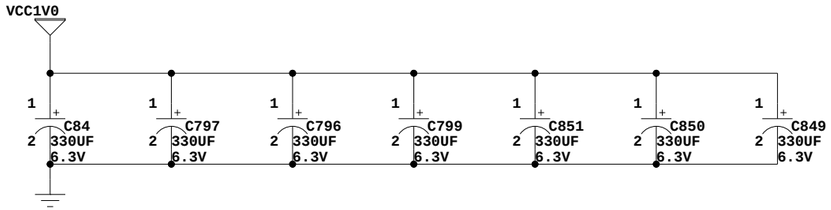
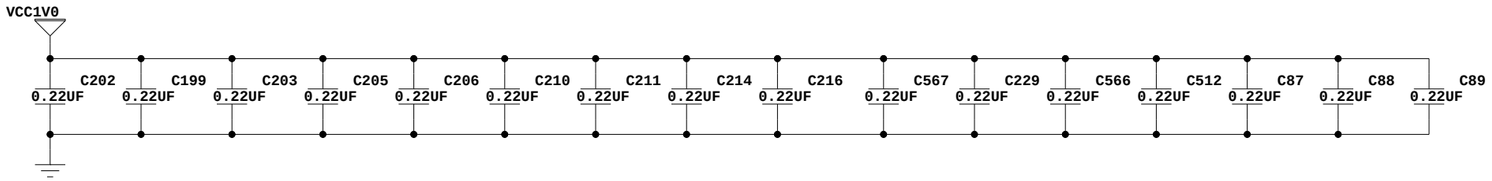
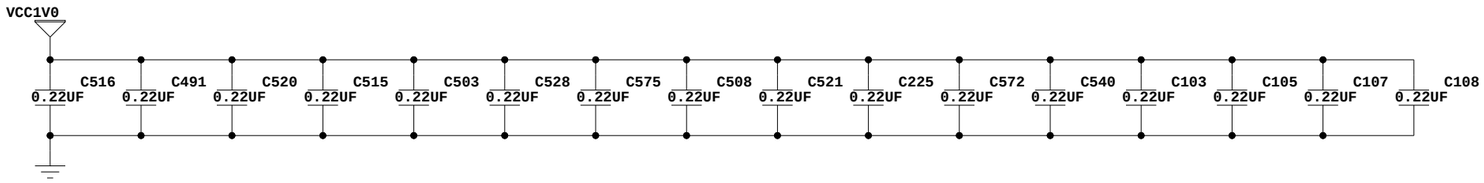
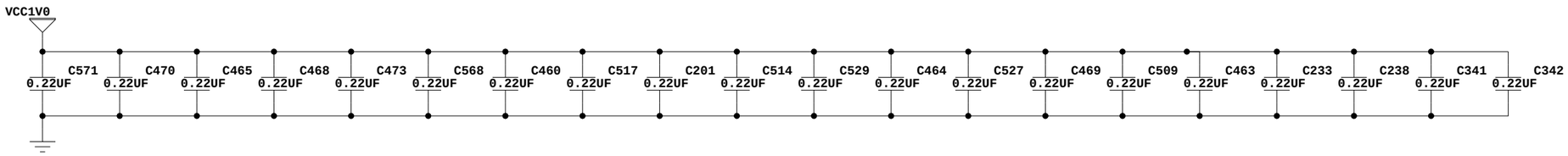
VCCINT 1.0V









FPGA DECOUPLING PAGE 2

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA DECOUPLING PAGE 2

Date:	7-10-2008_10:19	Ver:	C
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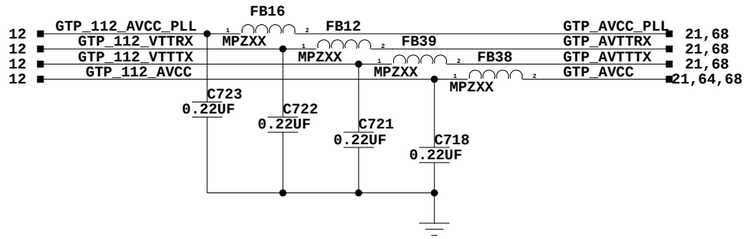
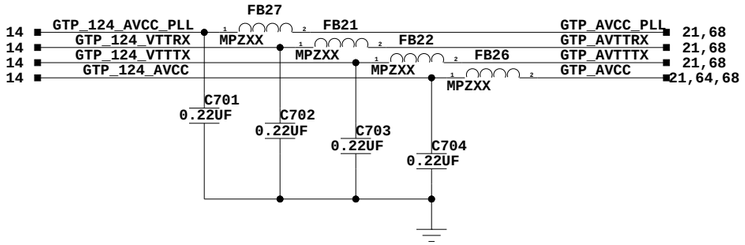
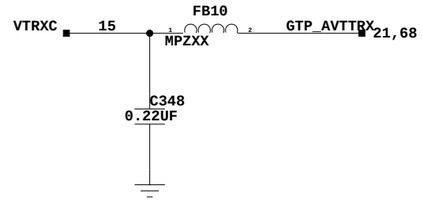
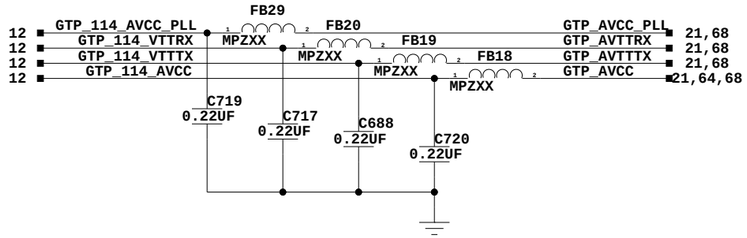
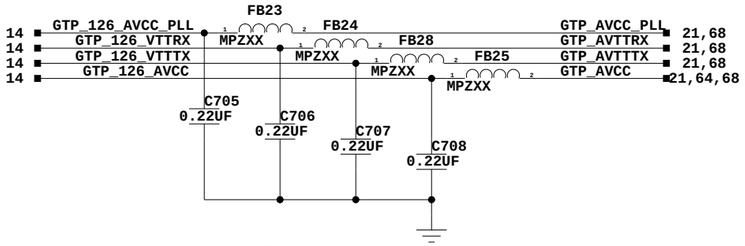
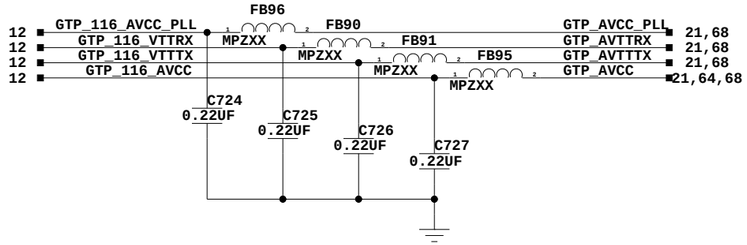


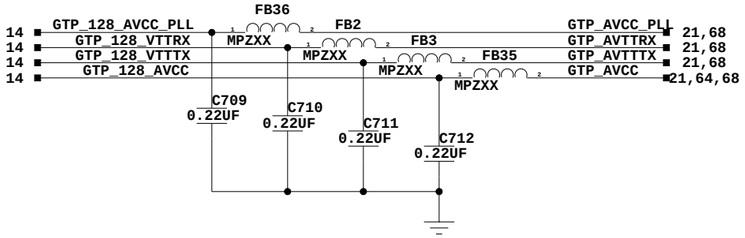


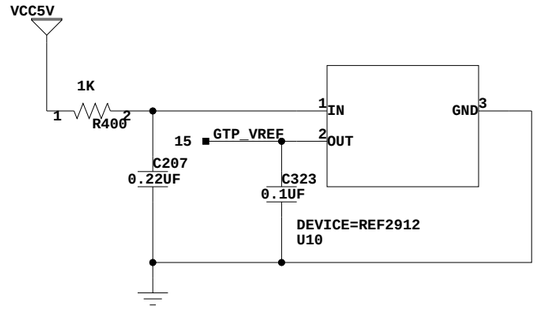


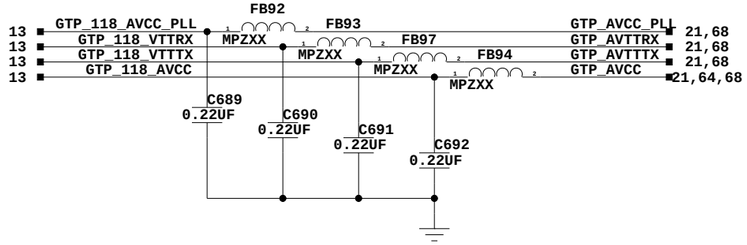


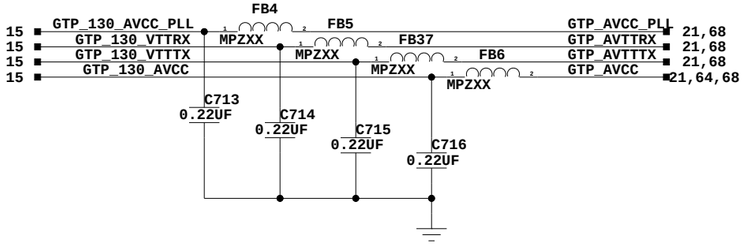


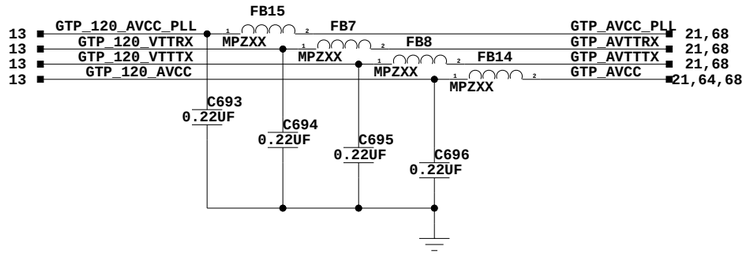


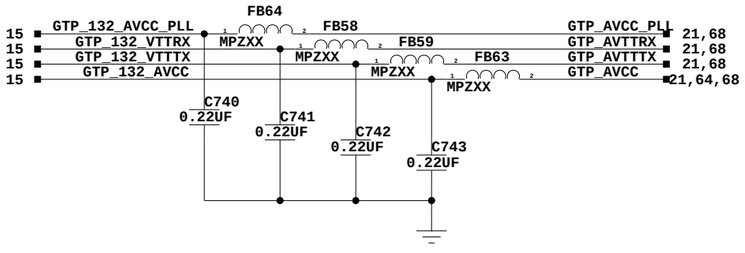


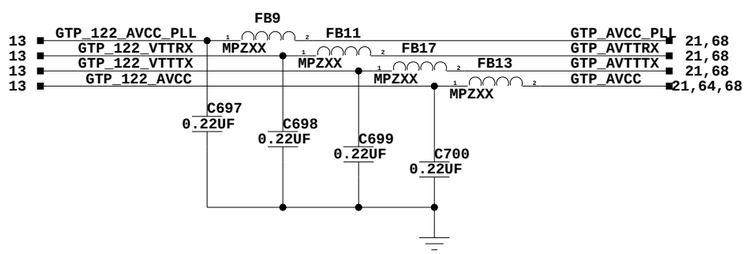


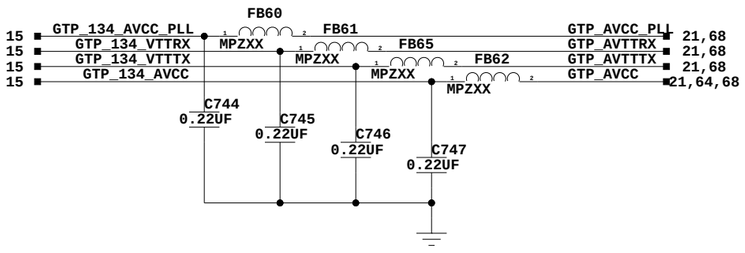






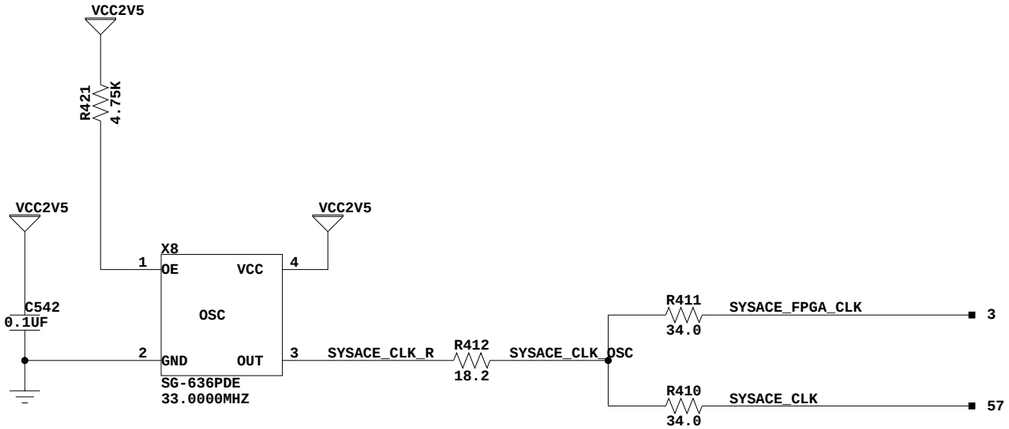


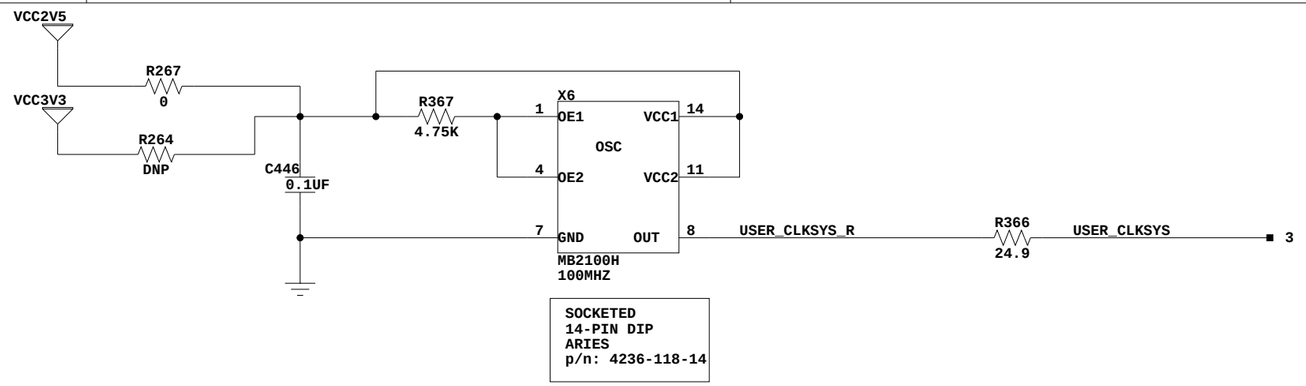


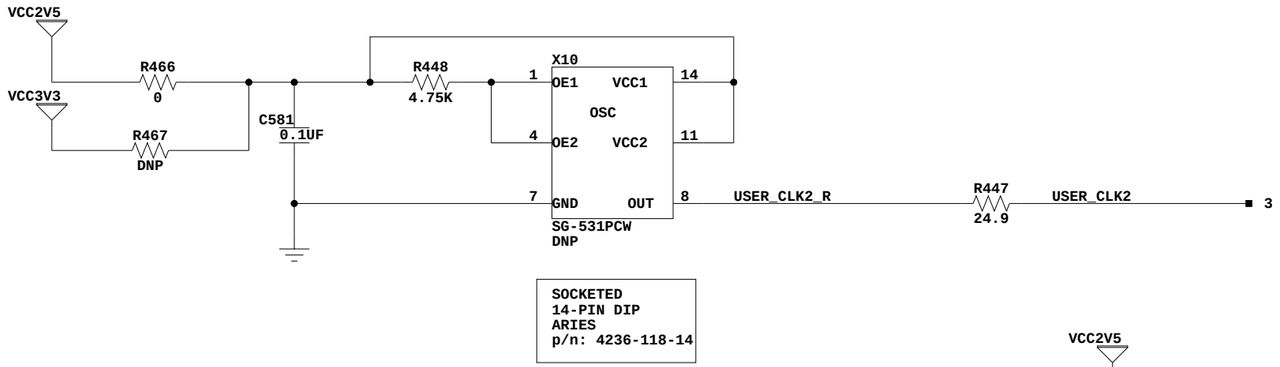


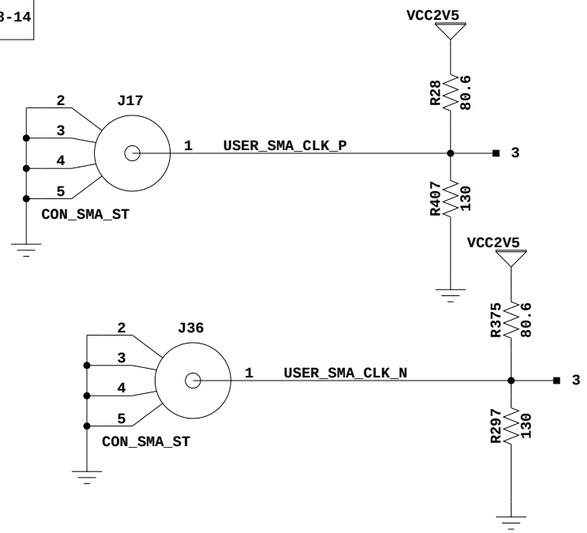
GTP POWER FILTER

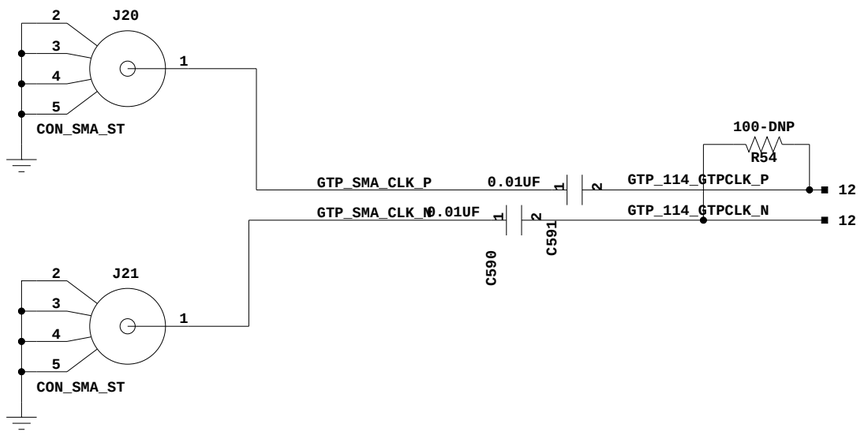
XILINX		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title:	SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM GTP POWER FILTER		
Date:	7-10-2008_10:19	Ver:	C
Sheet Size: B		Rev:	01
Sheet	21 of 70	Drawn By	BF











CLOCKS: USER,MGT,SYSACE

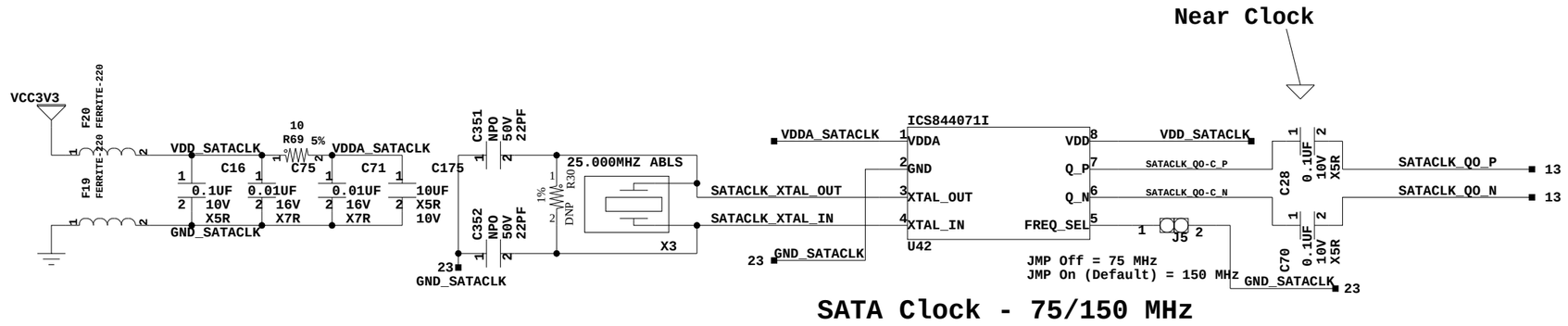
XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

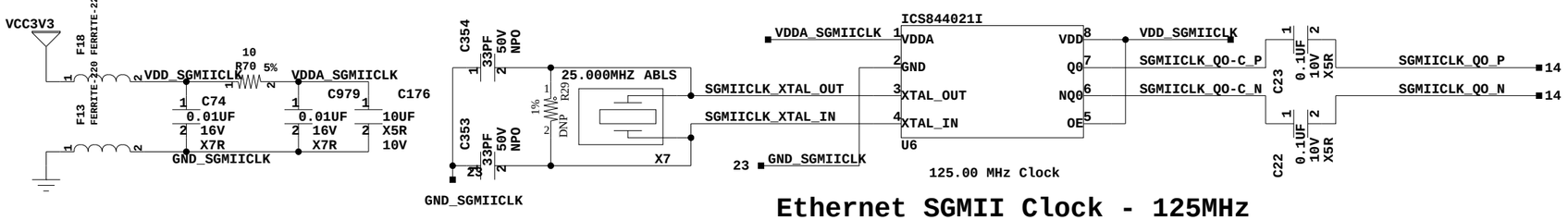
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

CLKS: USR,MGT,SYSACE

Date:	7-10-2008_10:19	Ver:	C
Sheet Size: B		Rev:	01
Sheet	22 of 70	Drawn By	BF



SATA Clock - 75/150 MHz



Ethernet SGMII Clock - 125MHz

SATA, SGMII CLOCKS

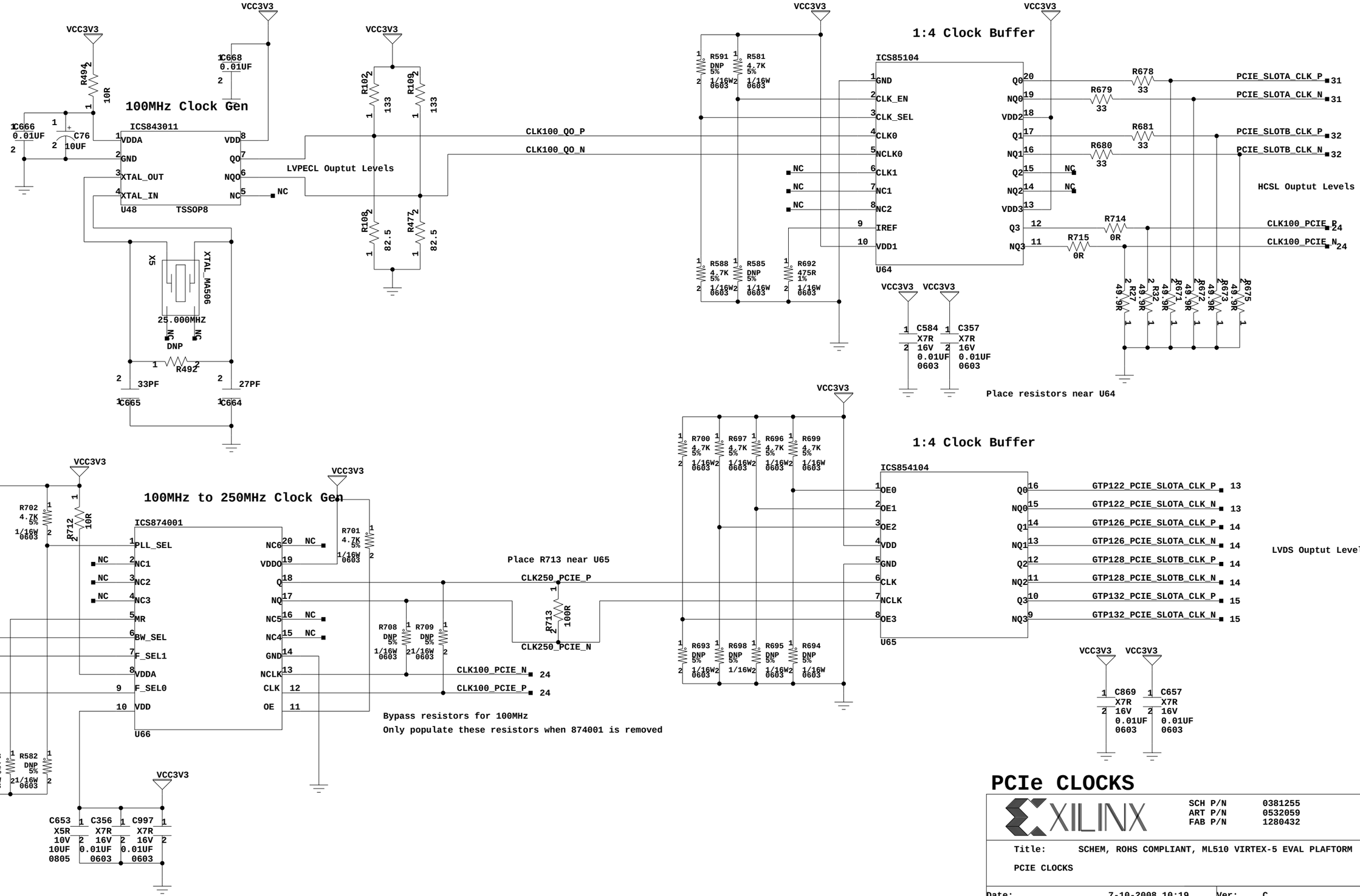
XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

SATA, SGMII CLOCKS

Date:	7-10-2008_10:19	Ver:	C
Sheet Size: B		Rev:	01
Sheet	23 of 70	Drawn By	BF



PCIe CLOCKS

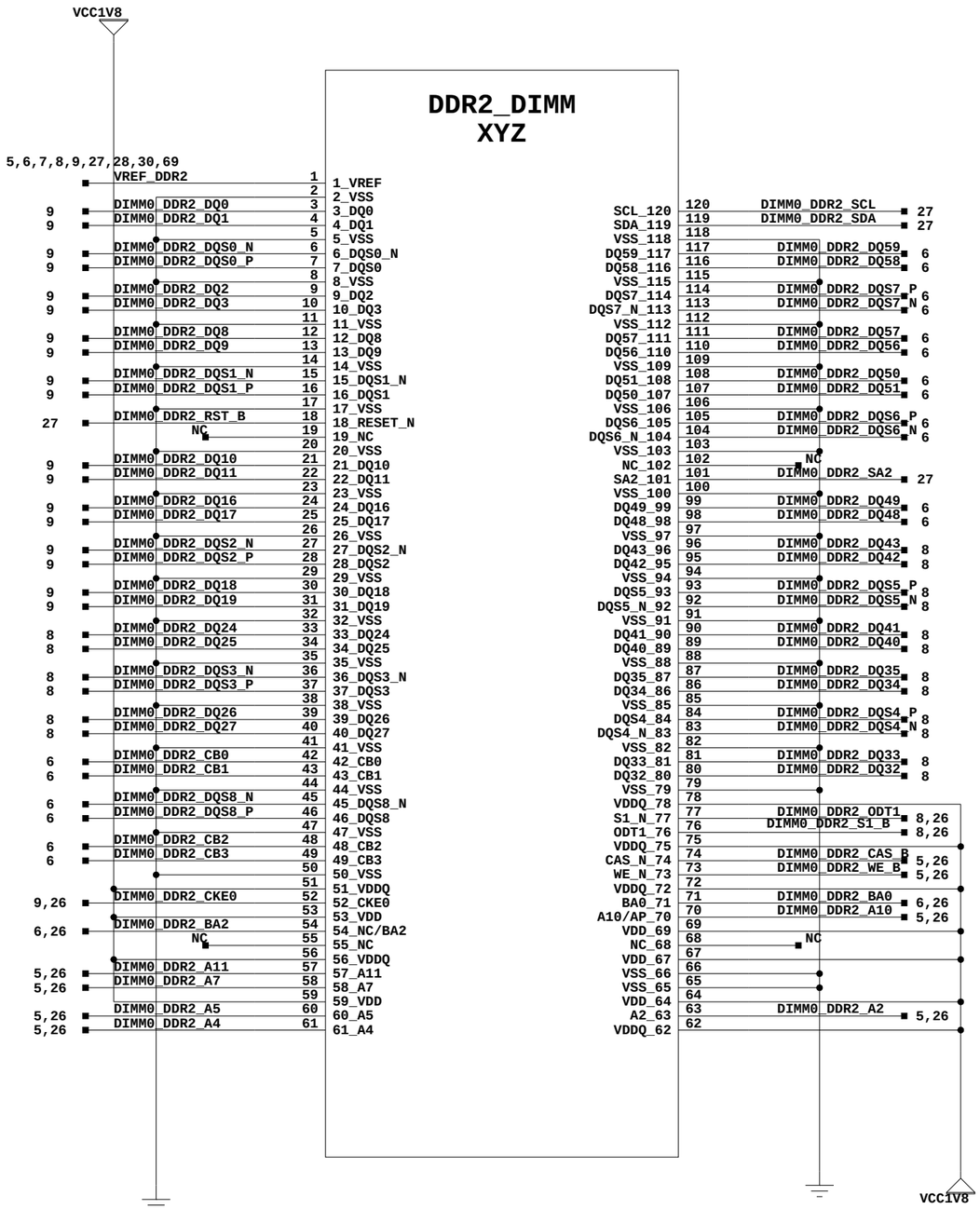
XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

PCIE CLOCKS

Date:	7-10-2008_10:19	Ver:	C
Sheet Size: B		Rev:	01
Sheet	24 of 70	Drawn By	BF



P48

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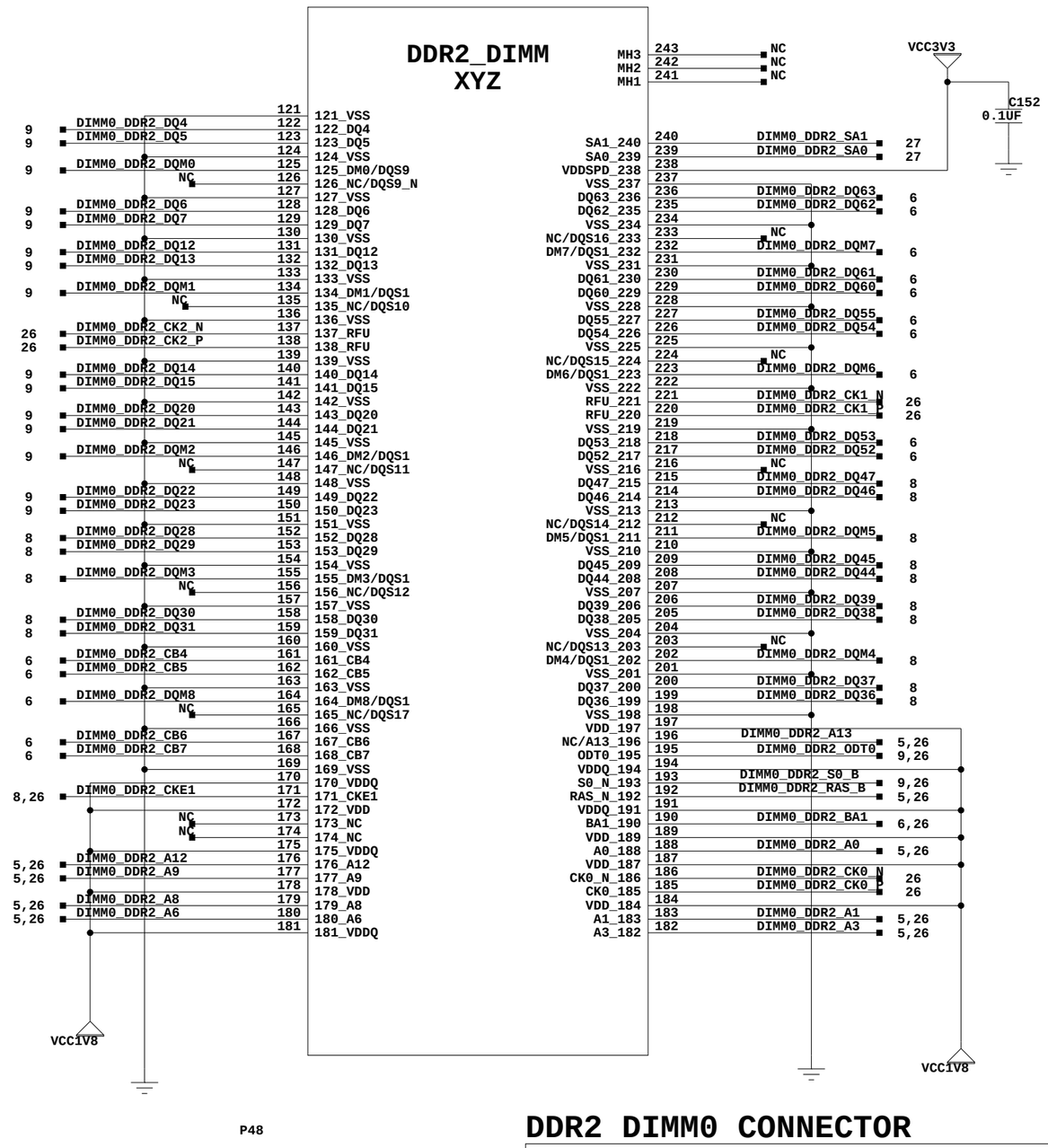
PKG_TYPE=CON-240-DDRAM
PARTS=1
LEVEL=STD



P48

DEVICE=DDR2_DIMM
PKG_TYPE=CON-240-DDRAM
PARTS=1
LEVEL=STD

I2C ADDR = 0xA8

DDR2 DIMM0 CONNECTOR

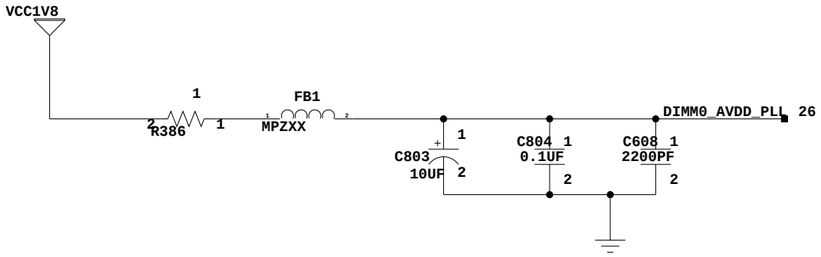
XILINX

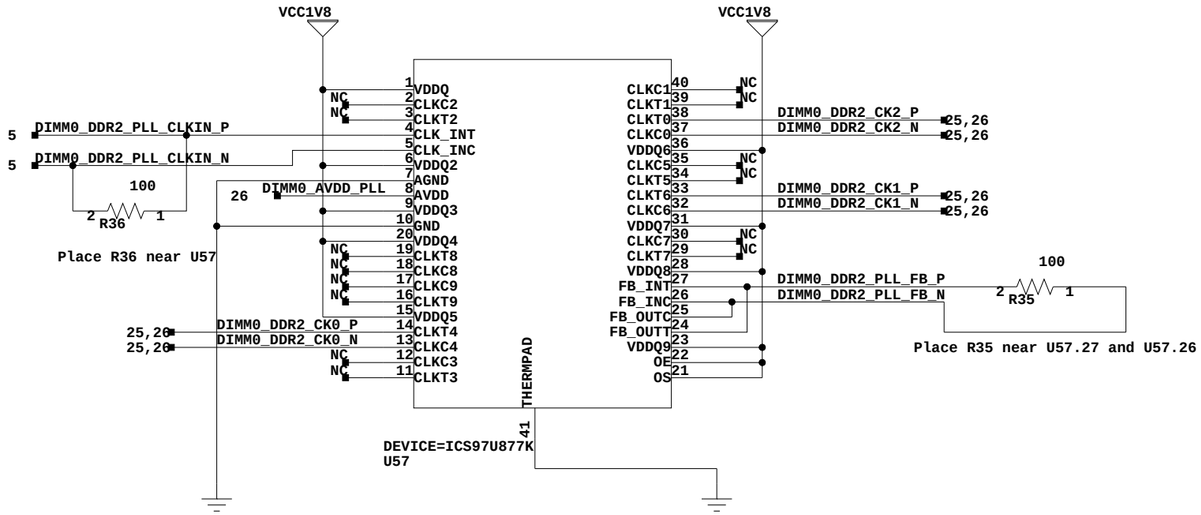
SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

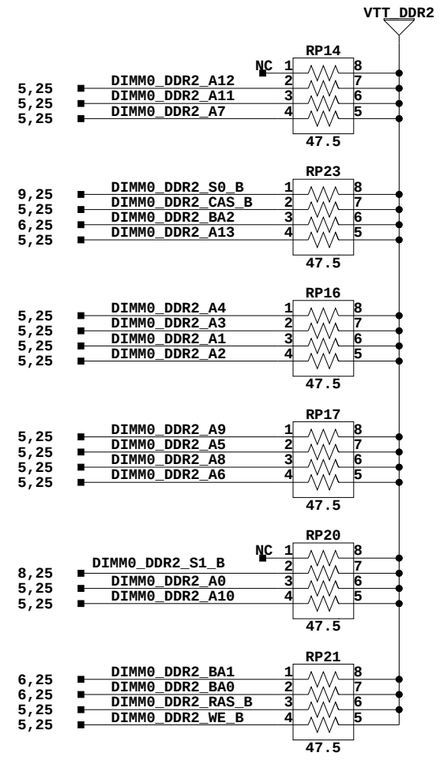
DDR2 DIMM0 CONNECTOR

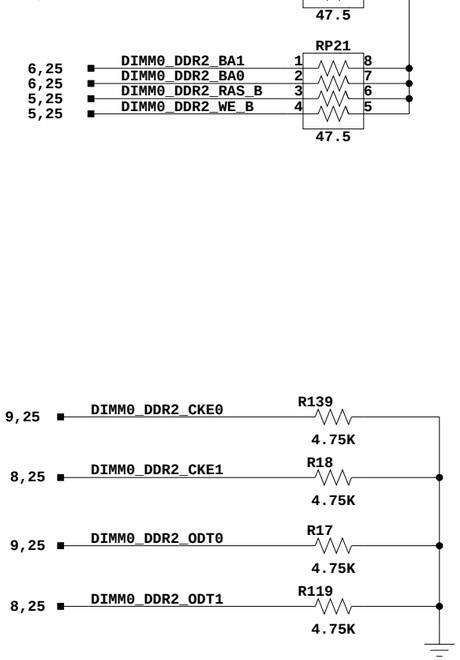
Date:	8-1-2008_15:08	Ver:	C
Sheet Size: B		Rev:	01
Sheet	25 of 70	Drawn By	BF



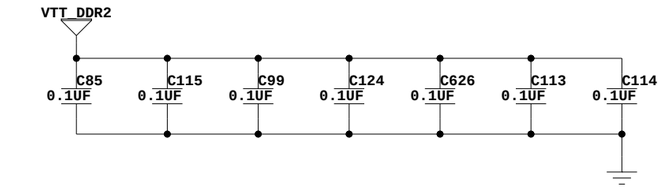


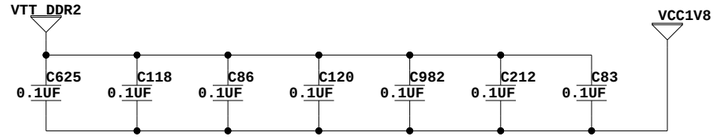
DIMM0_DDR2_PLL_FB* to be length matched to DIMM0_DDR2_CLKIN_*

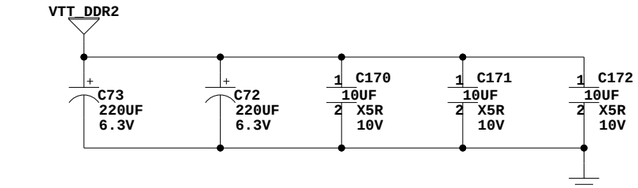


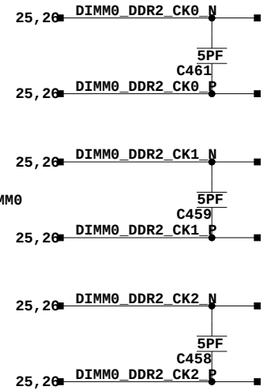


Since this is a source-sink power supply,
split of decoupling capacitors between VTT-GND and VTT-VCC1V8









Place these 5pf caps near DDR2 DIMM0

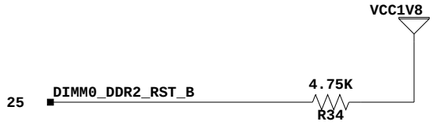
DIMM0 DDR2 SSTL-2 TERMINATION

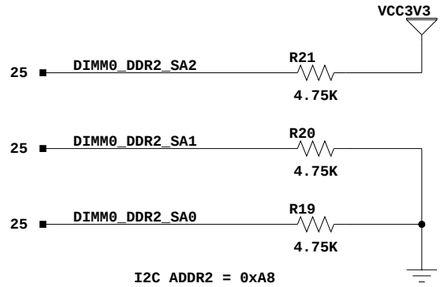
XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

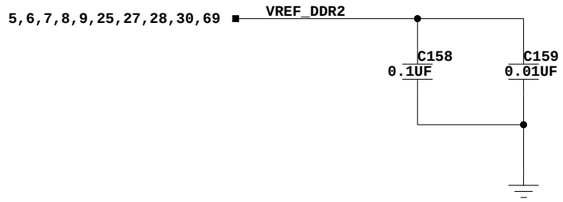
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
DIMM0 DDR2 SSTL-2 TERMINATION

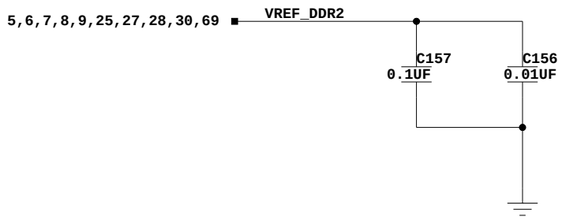
Date:	7-10-2008_10:19	Ver:	C
Sheet Size: B		Rev:	01
Sheet	26 of 70	Drawn By	BF

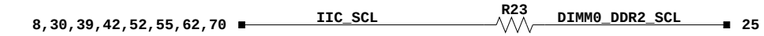


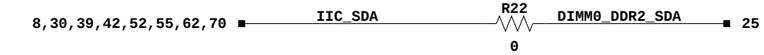


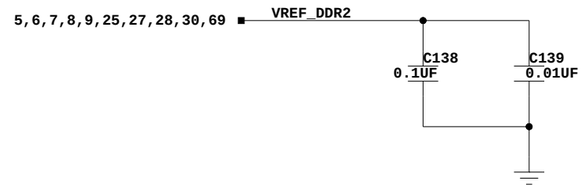
I2C ADDR2 = 0xA8

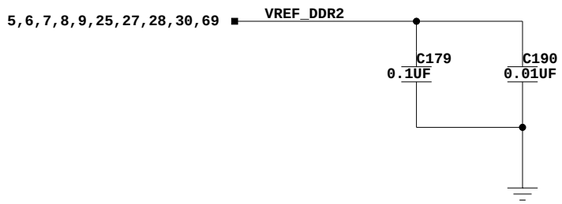


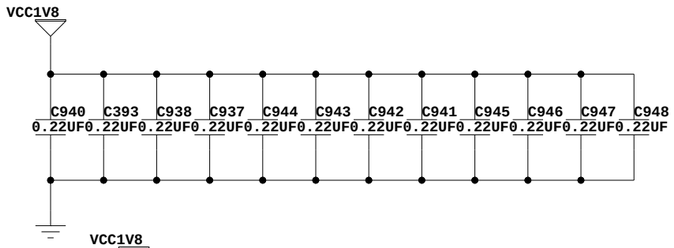


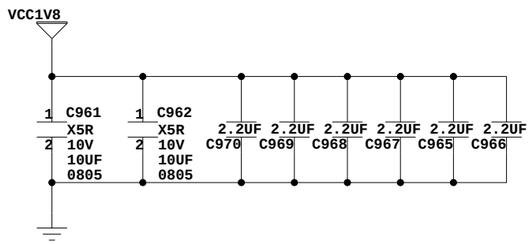










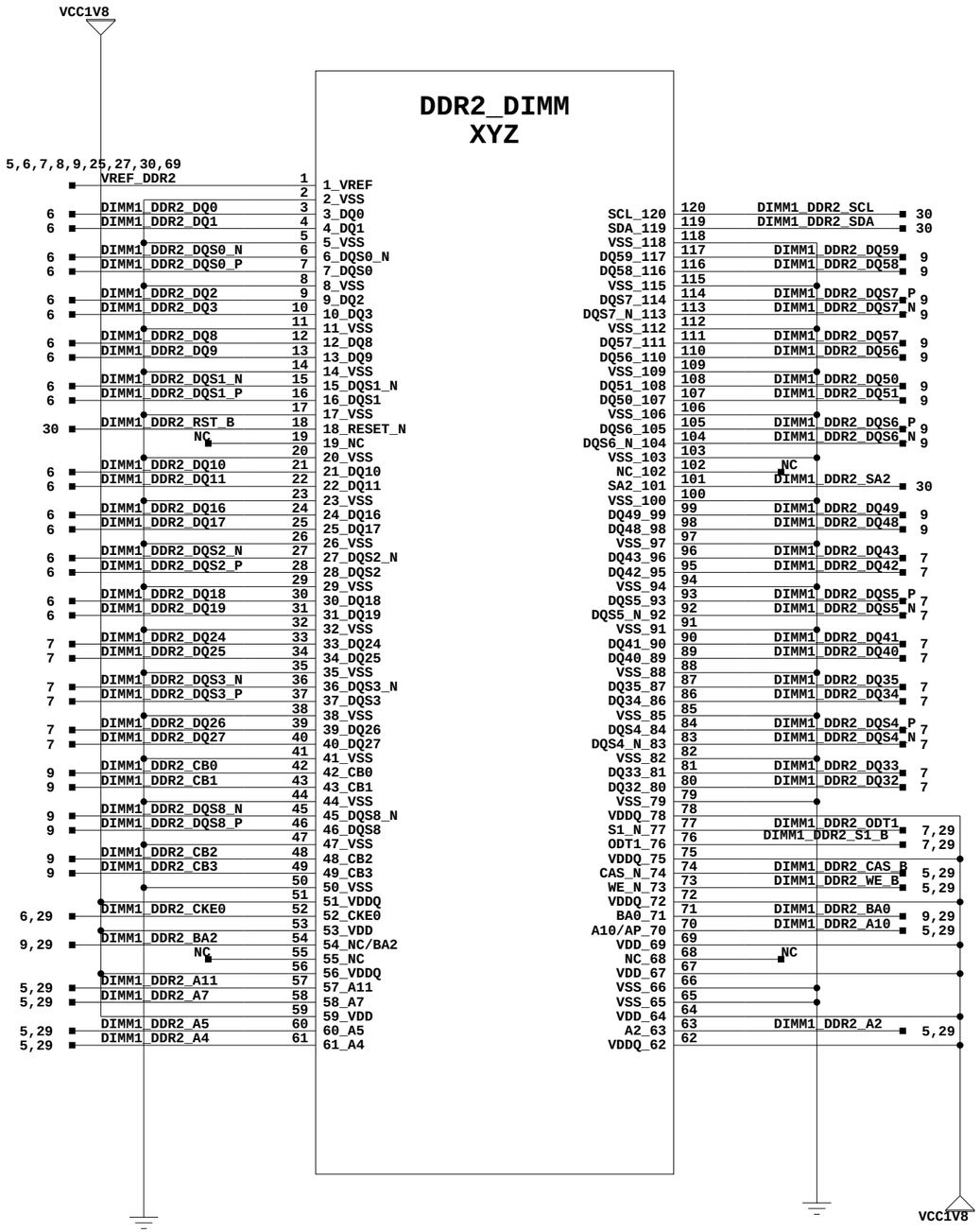


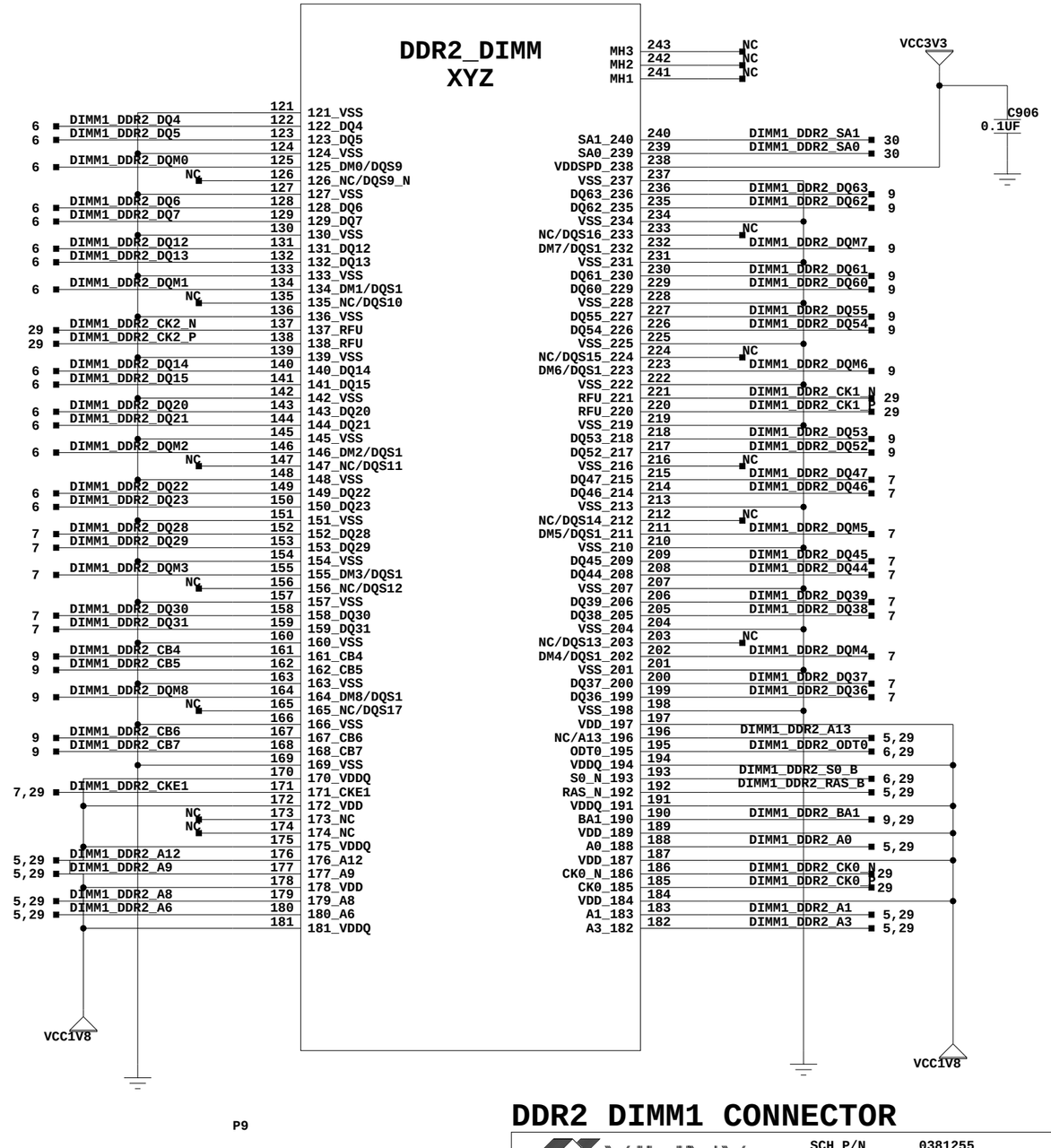
DIMM0 DDR2 DECOUPLING

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
DIMM0 DDR2 DECOUPLING

Date:	7-10-2008_10:19	Ver:	C
Sheet Size: B		Rev:	01
Sheet	27 of 70	Drawn By	BF





DDR2 DIMM1 CONNECTOR

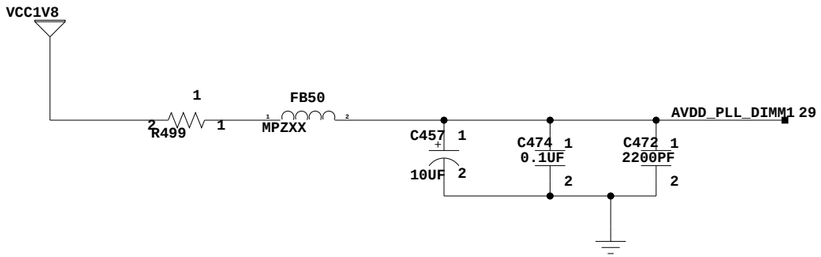
XILINX

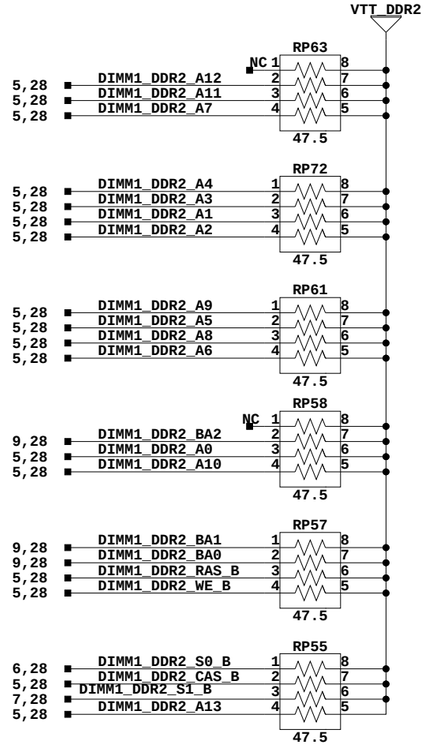
SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

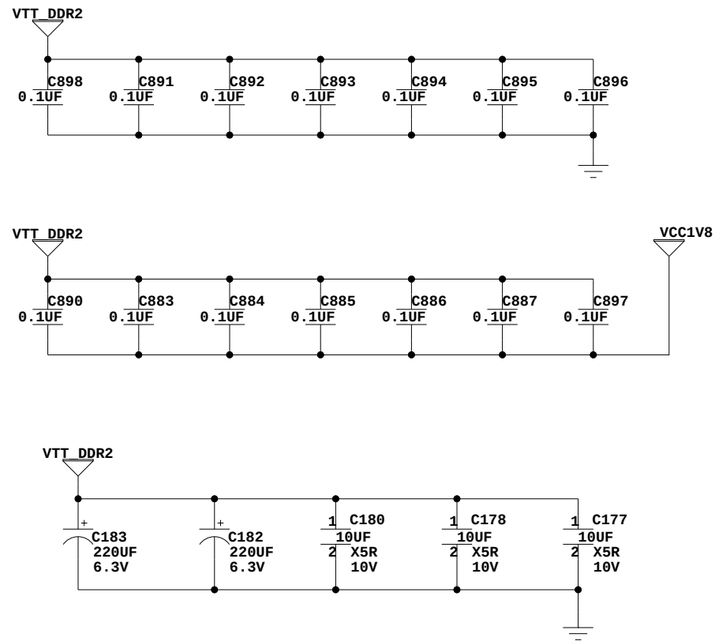
DDR2 DIMM2 CONNECTOR

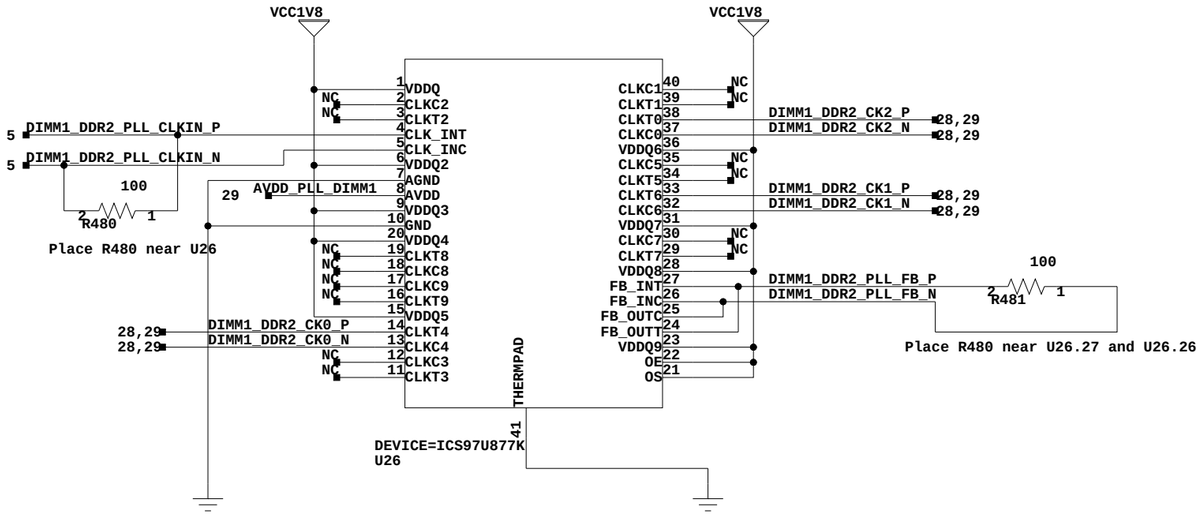
Date:	8-1-2008_15:08	Ver:	C
Sheet Size: B		Rev:	01
Sheet	28 of 70	Drawn By	BF



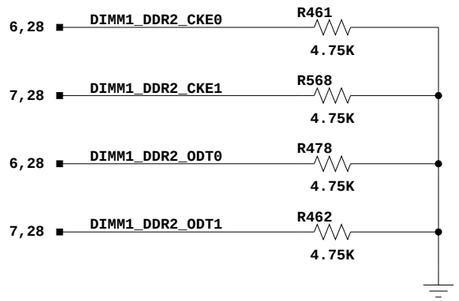


Since this is a source-sink power supply,
split of decoupling capacitors between VTT-GND and VTT-VCC1V8

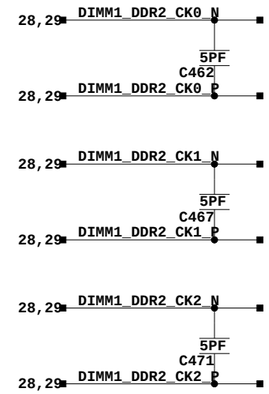




DIMM1_DDR2_PLL_FB* to be length matched to DIMM0_DDR2_CLKIN_*



Place these 5pf caps near DDR2 DIMM1



DIMM1 DDR2 SSTL-2 TERMINATION

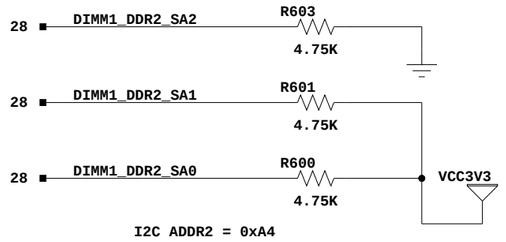
XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

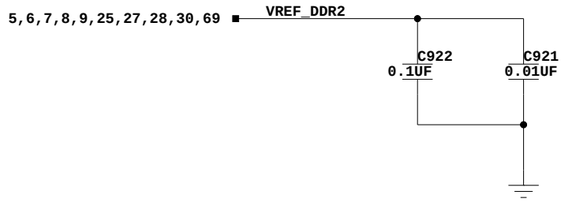
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

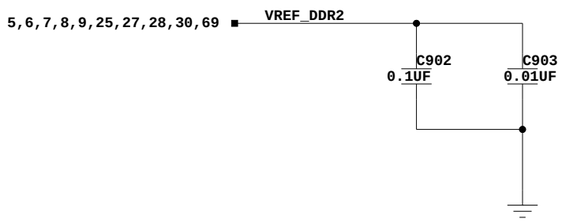
DIMM1 DDR2 SSTL-2 TERMINATION

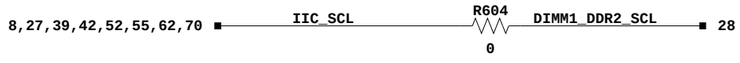
Date:	7-10-2008_10:19	Ver:	C
Sheet Size: B		Rev:	01
Sheet	29 of 70	Drawn By	BF

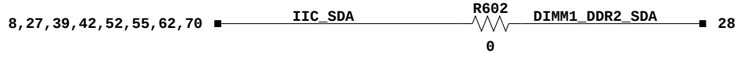


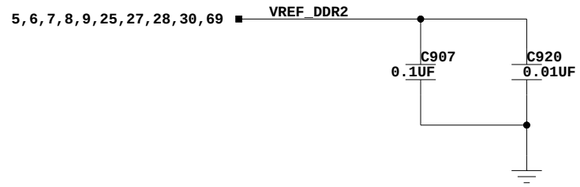
I2C ADDR2 = 0xA4

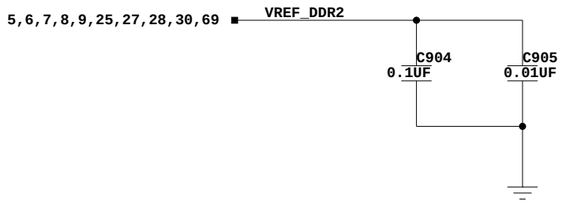


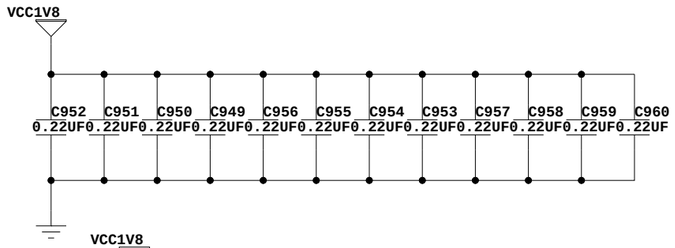


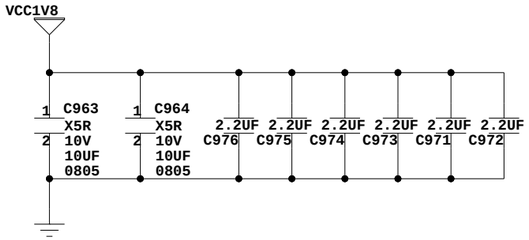












DIMM1 DDR2 DECOUPLING

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

DIMM1 DDR2 DECOUPLING

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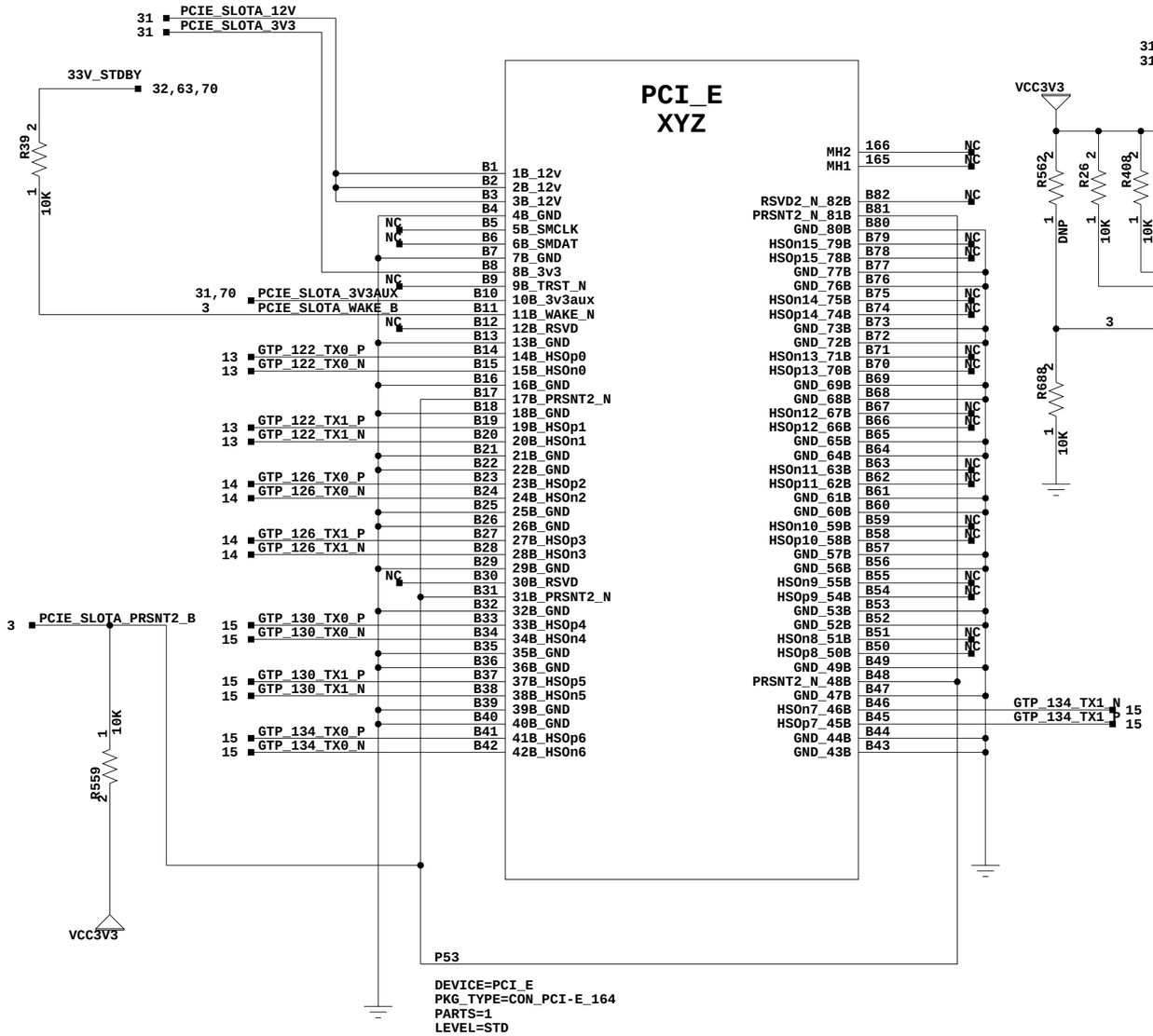

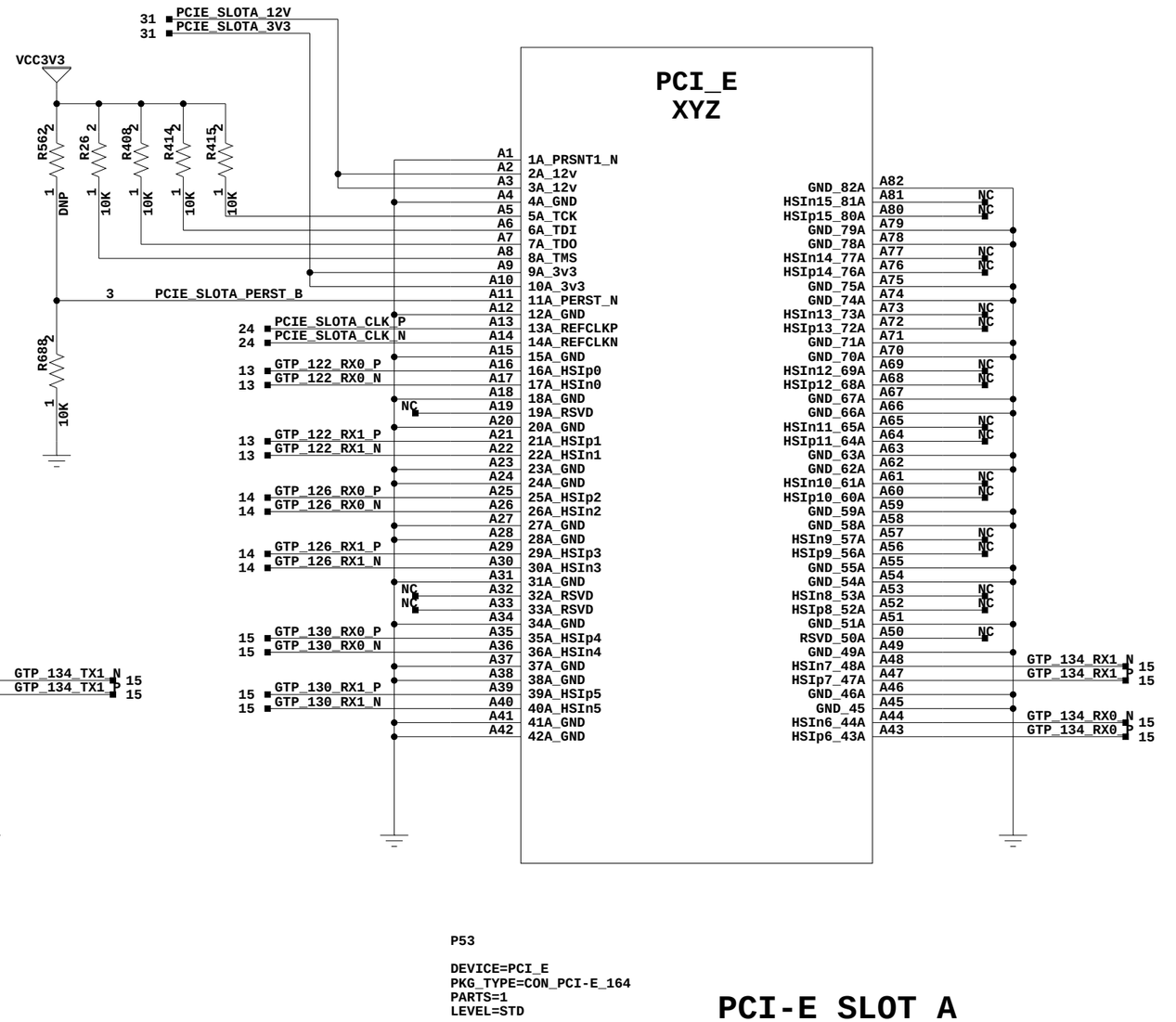

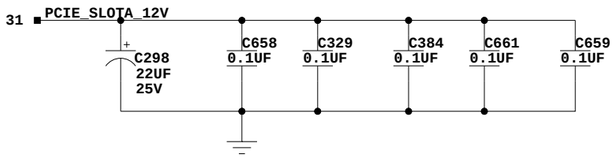

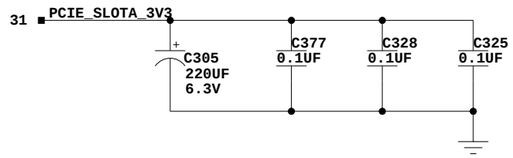

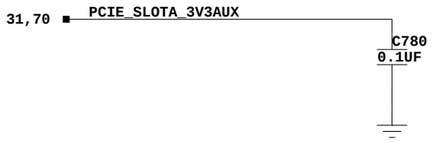

PCI-E SLOT A

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
PCI-E SLOT A

Date:	8-1-2008_15:08	Ver:	C
Sheet Size: B		Rev:	01
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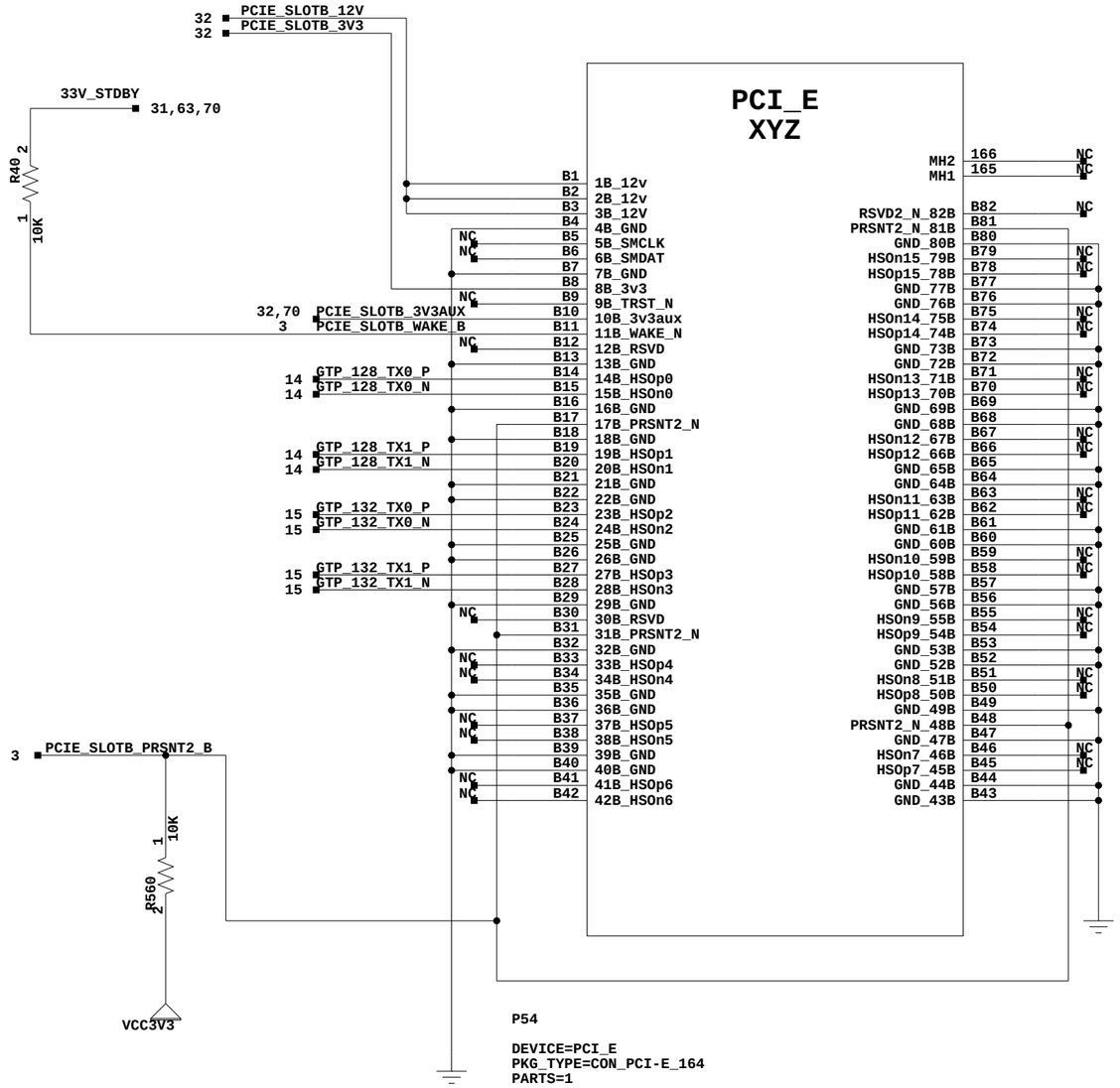

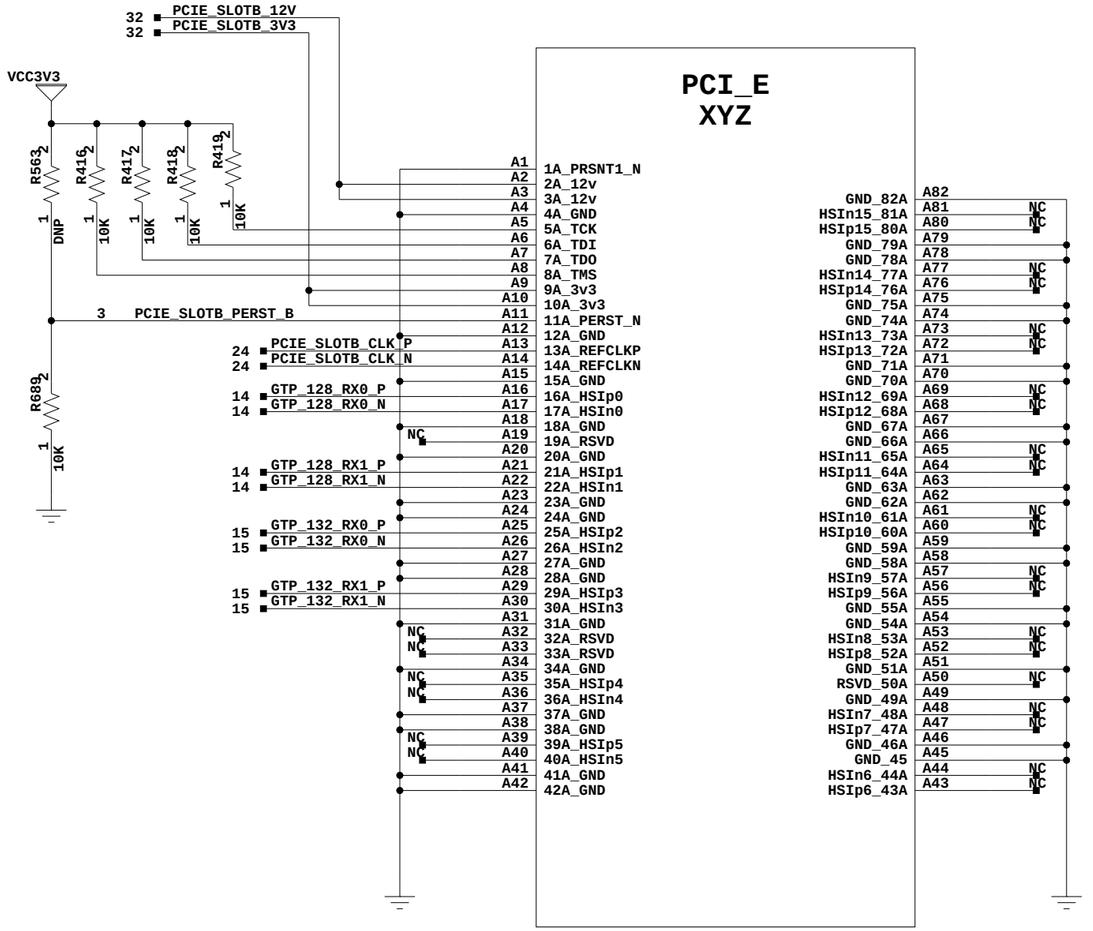

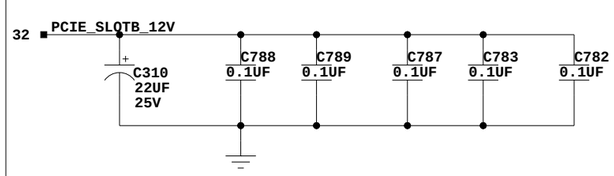

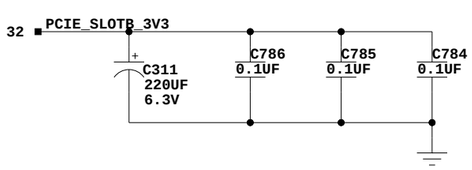

PCI-E SLOT B

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

PCI-E SLOT B

Date:	8-1-2008_15:08	Ver:	C
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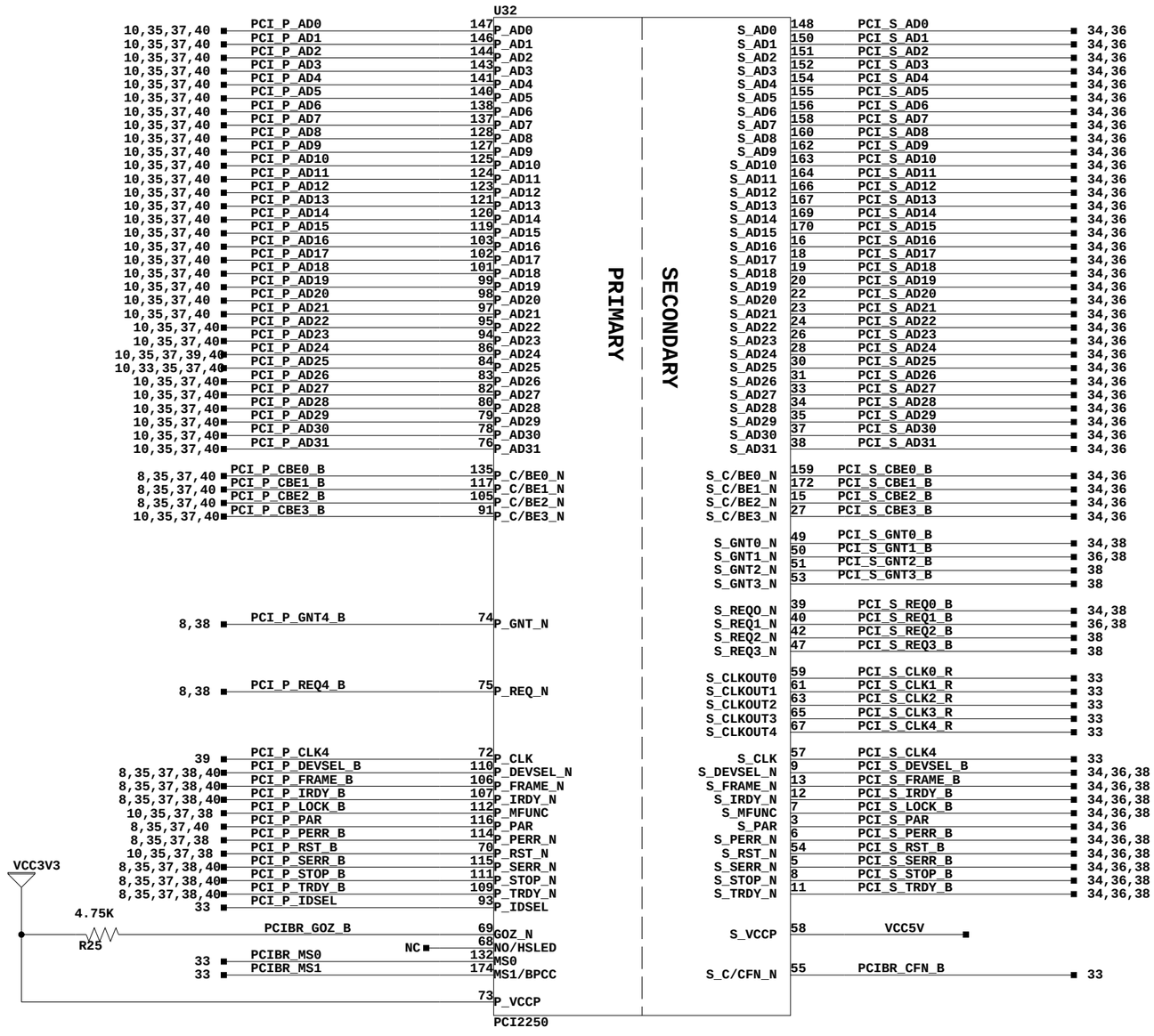
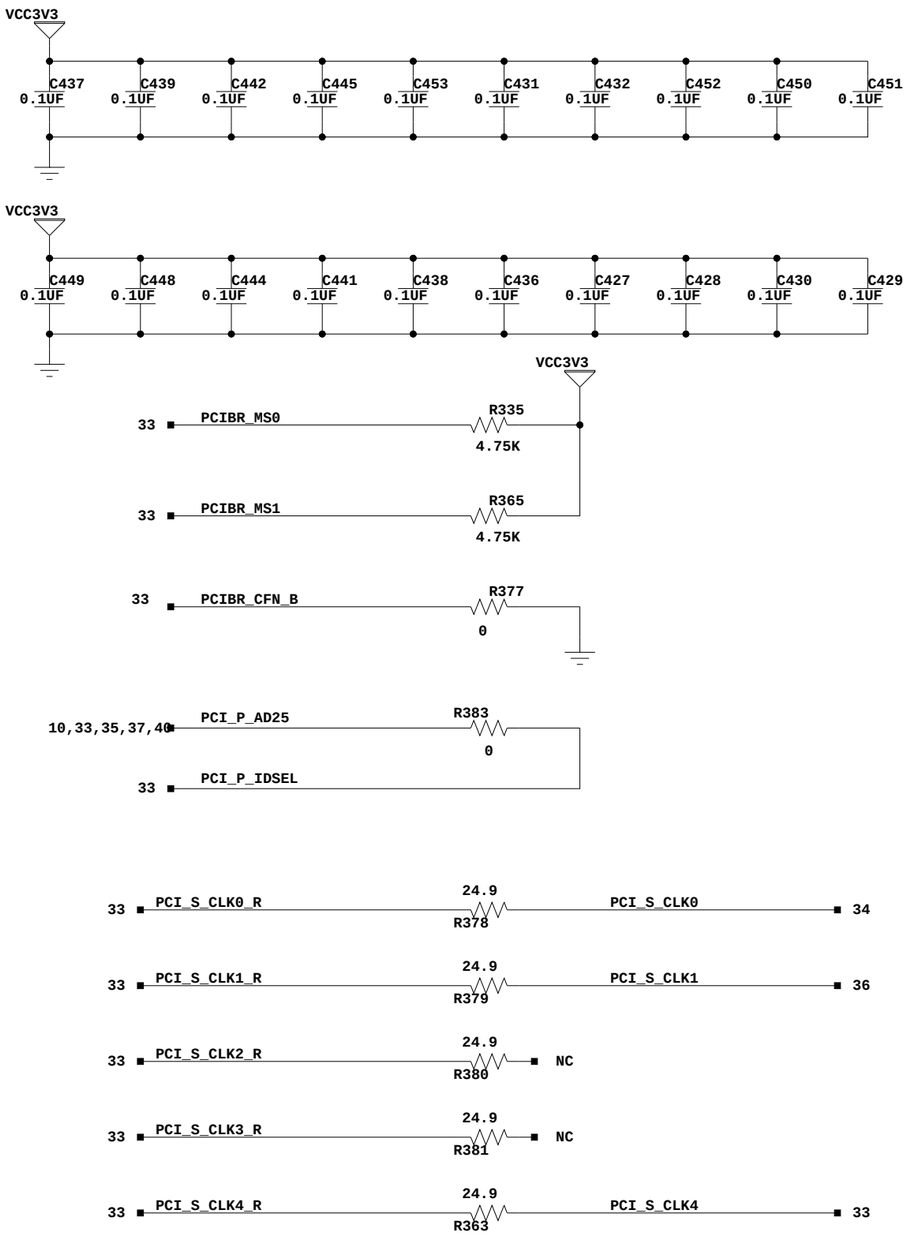
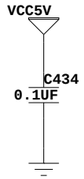
PCI-PCI BRIDGE

PCI2250_PGF







PCI-PCI BRIDGE

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

PCI-PCI BRIDGE

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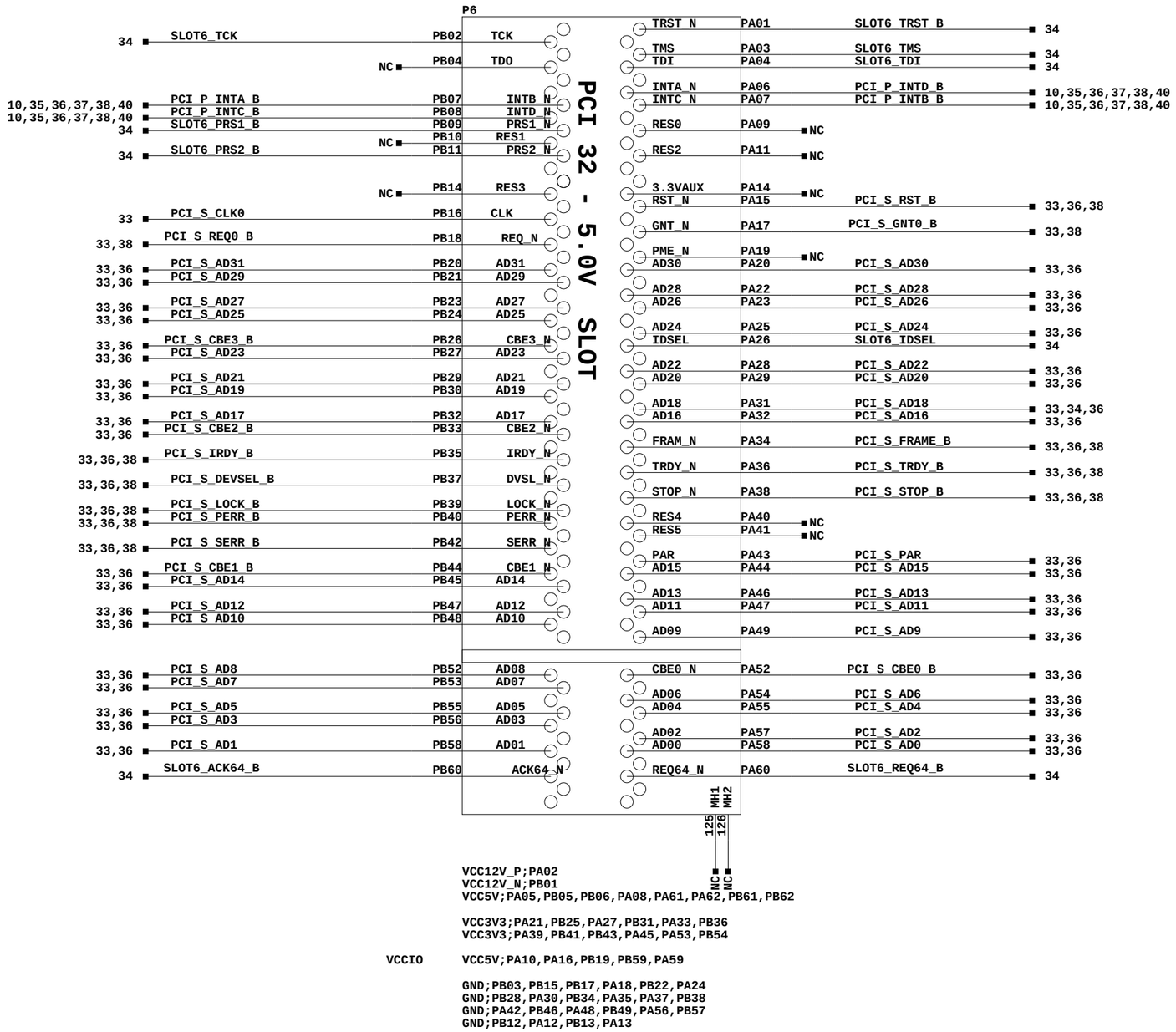
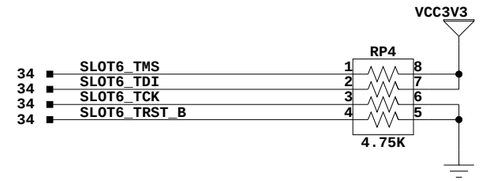
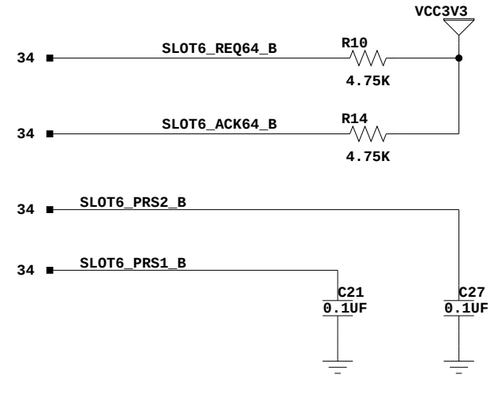
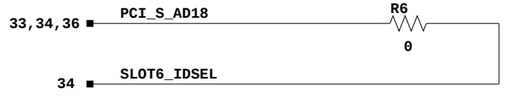
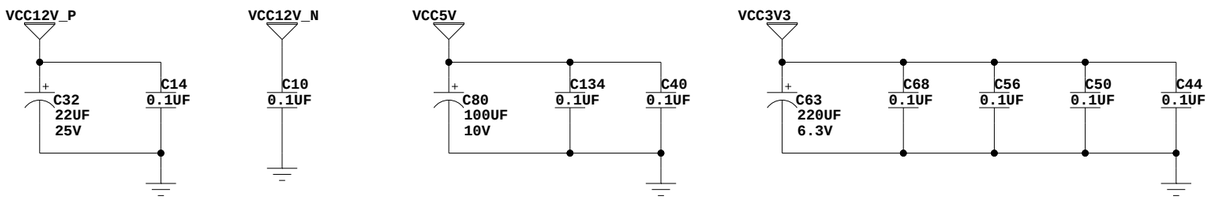
Sheet Size: B		Rev:	01
Sheet	33 of 70	Drawn By	BF











PCI SLOT 6, 5.0V, SECONDARY BUS

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

PCI SLOT 6, 5.0V, SECONDARY BUS

Date:	7-10-2008_10:19	Ver:	C
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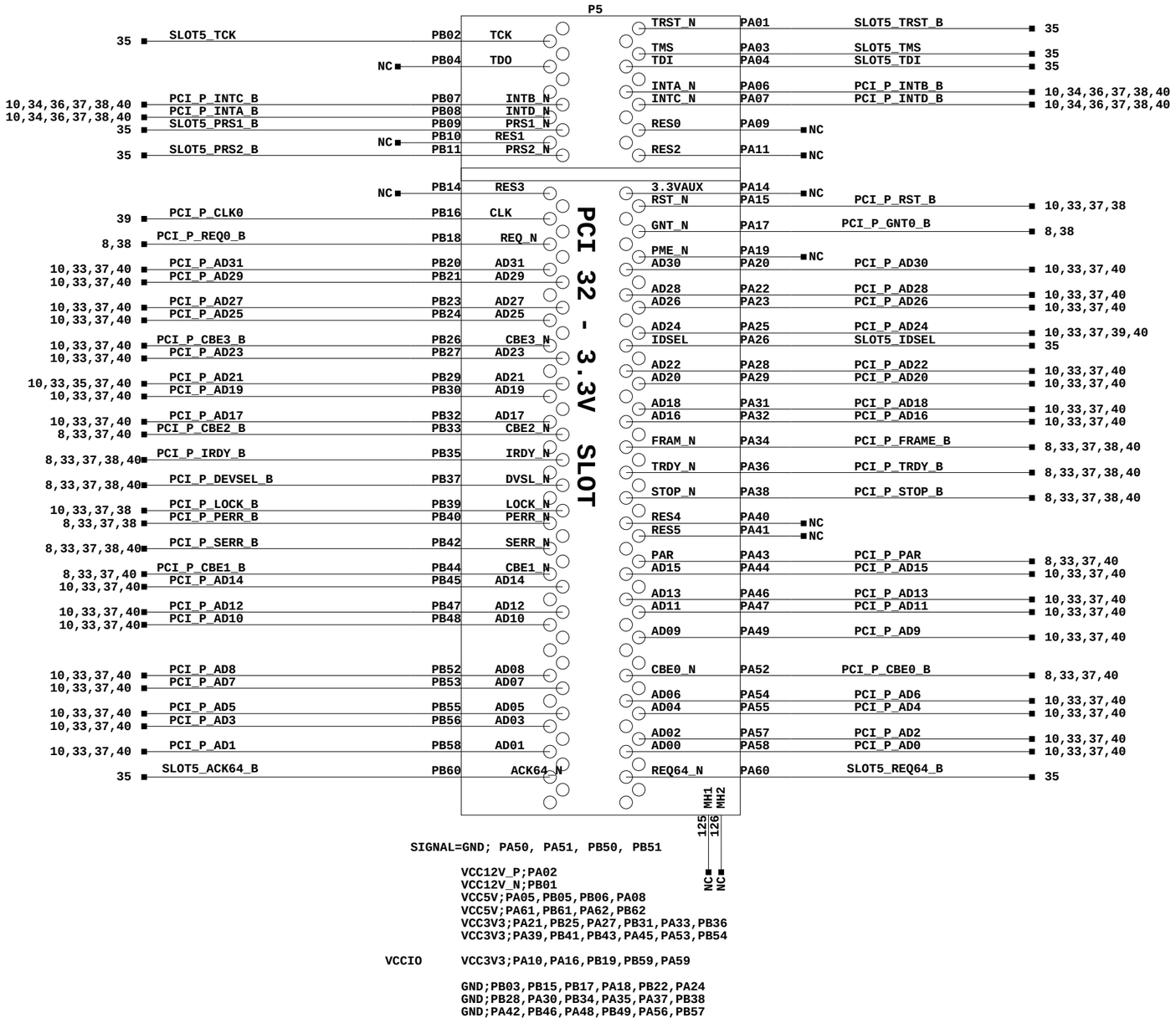

PCI SLOT 5, 3.3V, PRIMARY BUS

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

PCI SLOT 5, 3.3V, PRIMARY BUS

Date:	7-10-2008_10:19	Ver:	C
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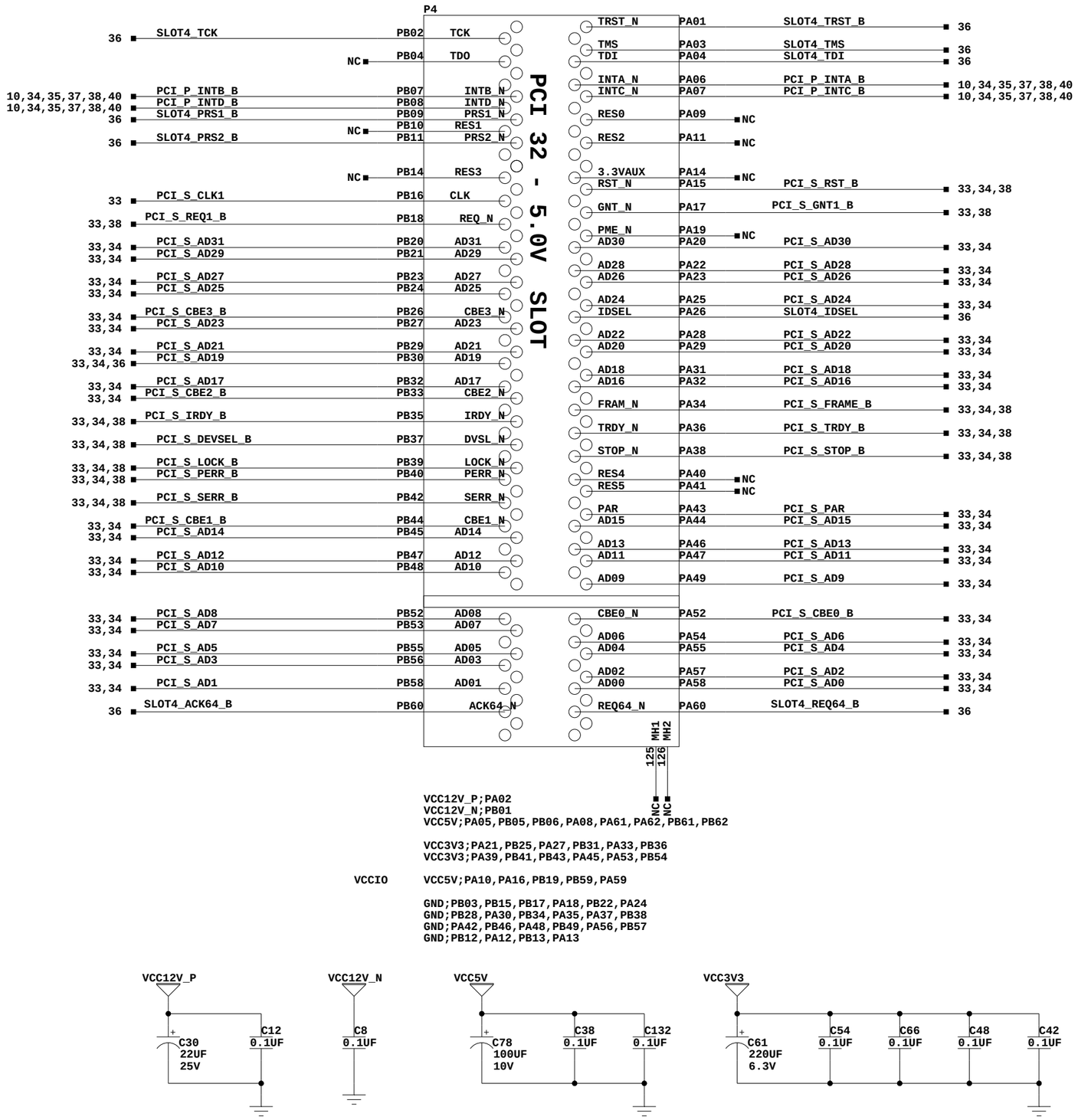

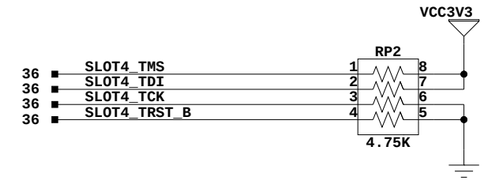

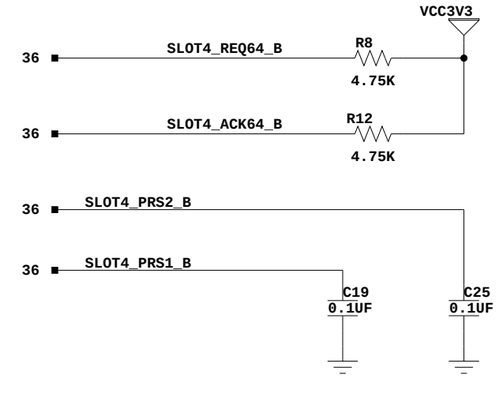

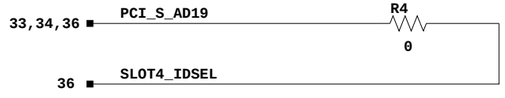

PCI SLOT 4, 5.0V, SECONDARY BUS

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

PCI SLOT 4, 5.0V, SECONDARY BUS

Date:	7-10-2008_10:19	Ver:	C
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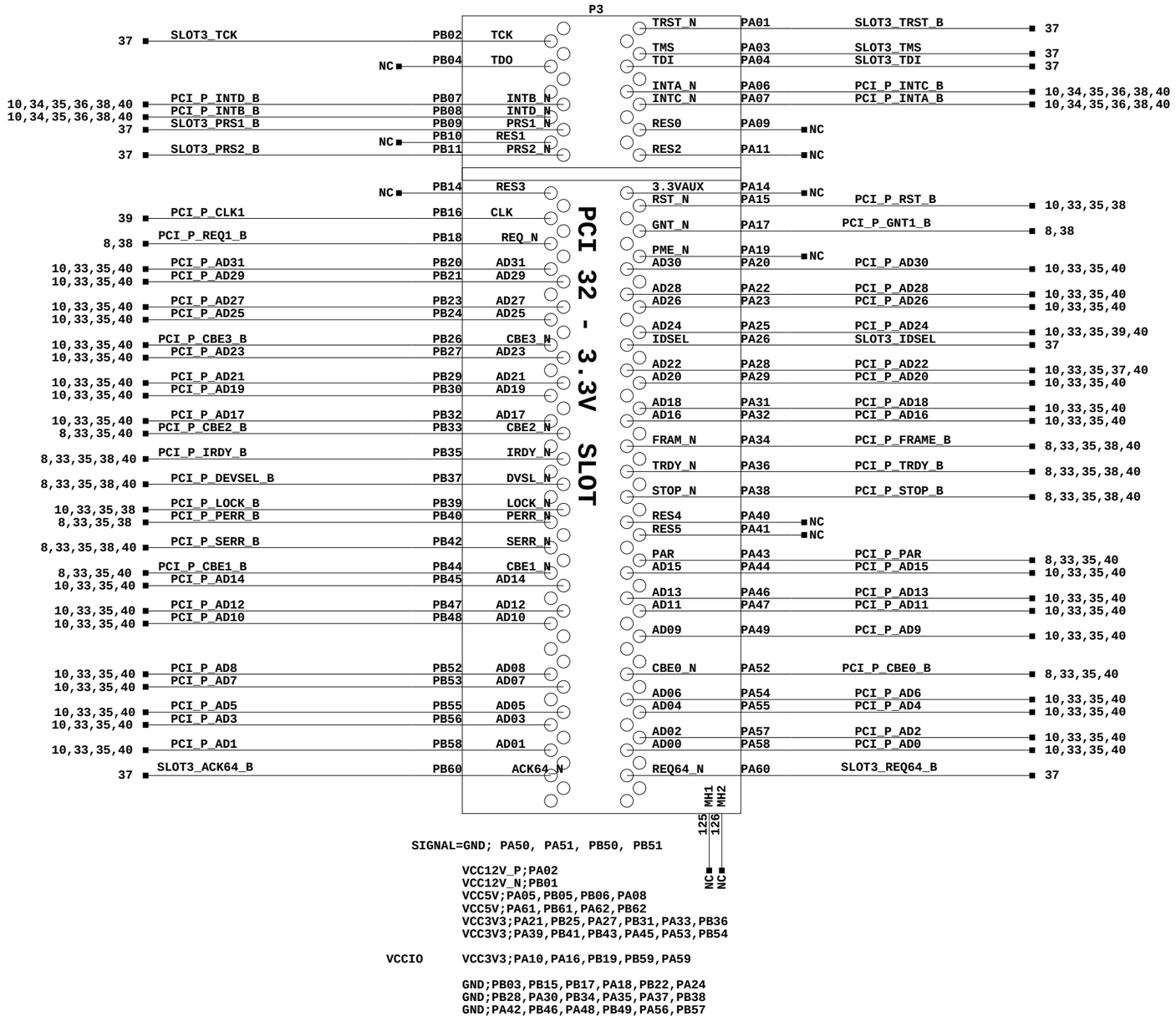

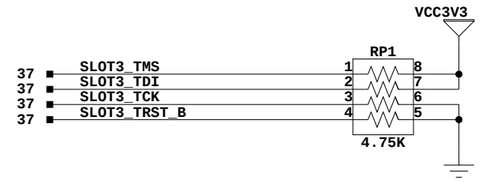

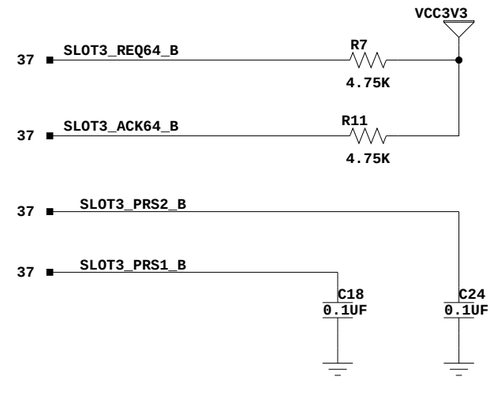

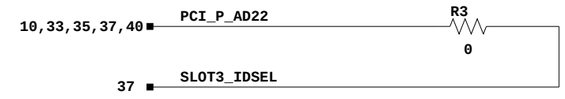

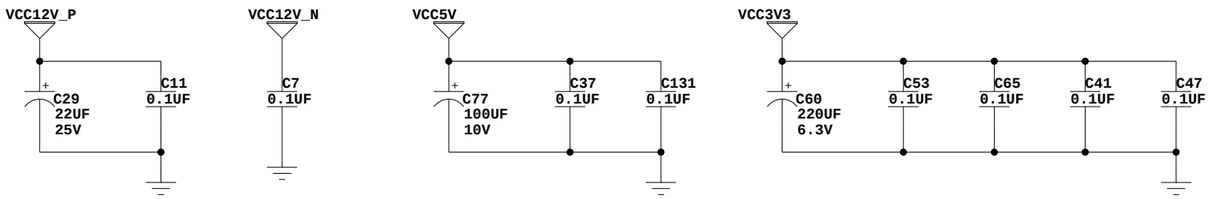

PCI SLOT 3, 3.3V, PRIMARY BUS

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

PCI SLOT 3, 3.3V, PRIMARY BUS

Date:	7-10-2008_10:19	Ver:	C
Sheet Size: B		Rev:	01
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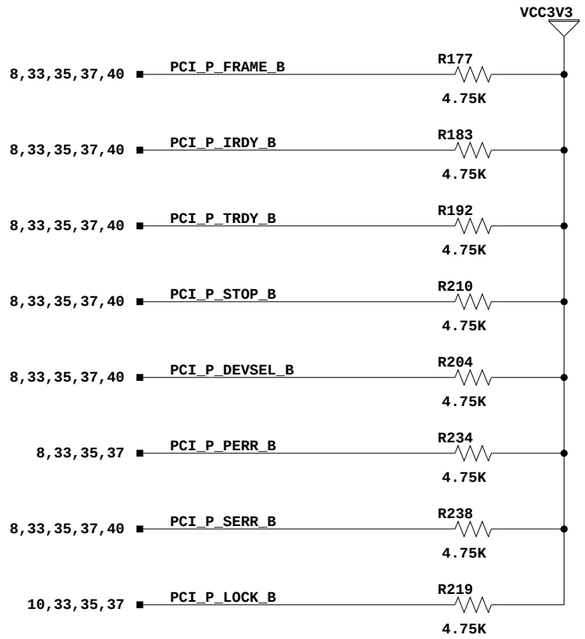

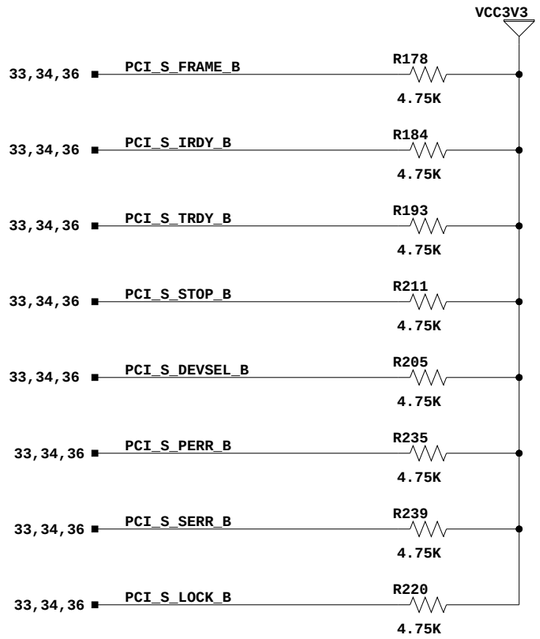

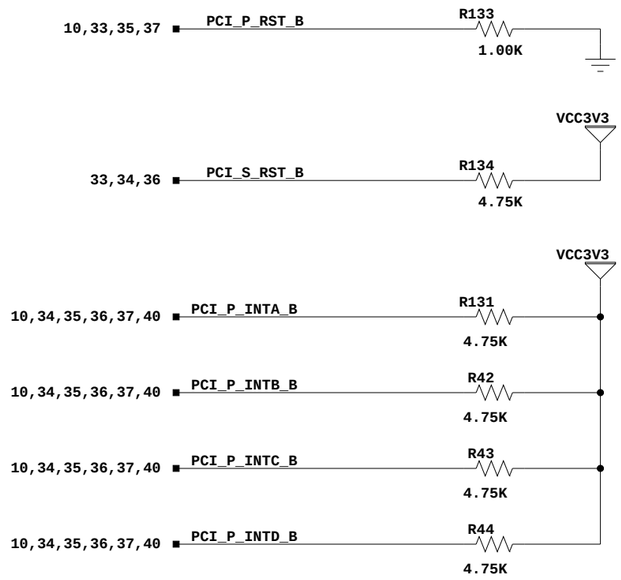

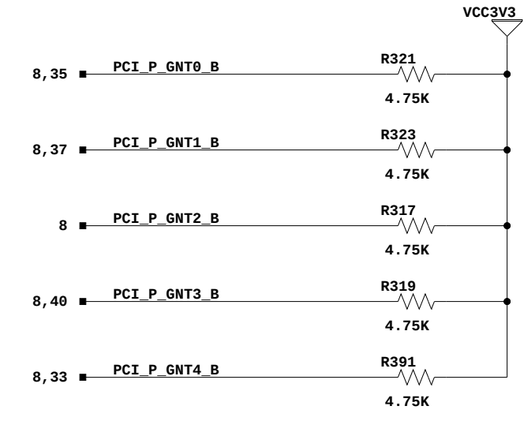

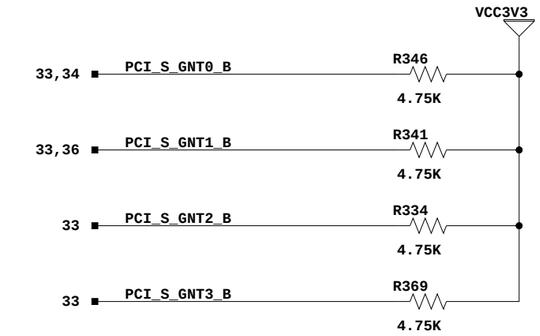

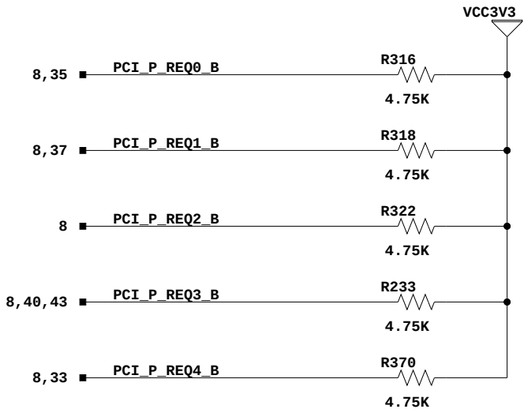

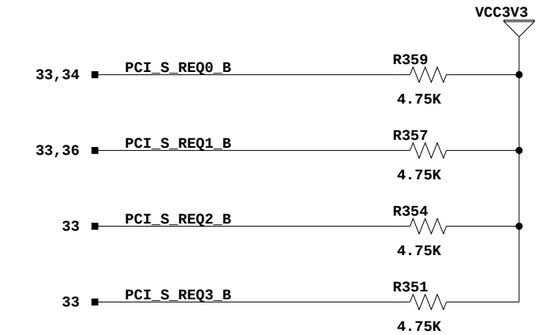

PCI BUS PULLUPS

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

PCI BUS PULLUPS

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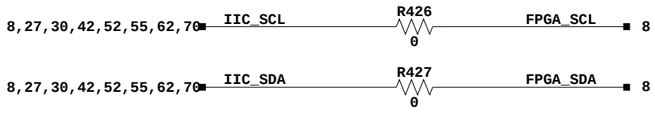
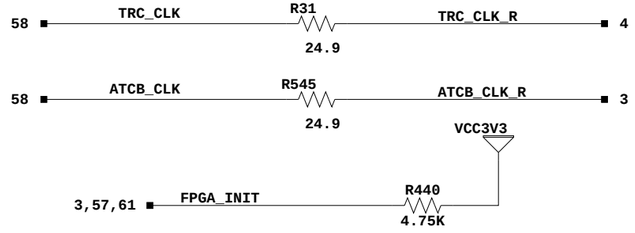
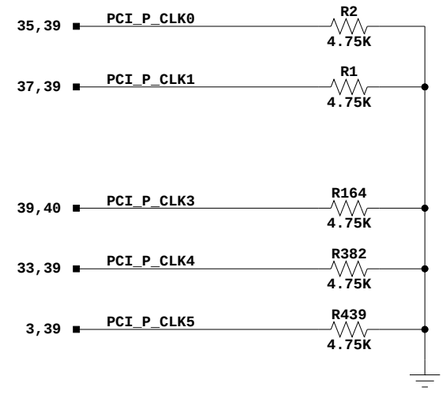
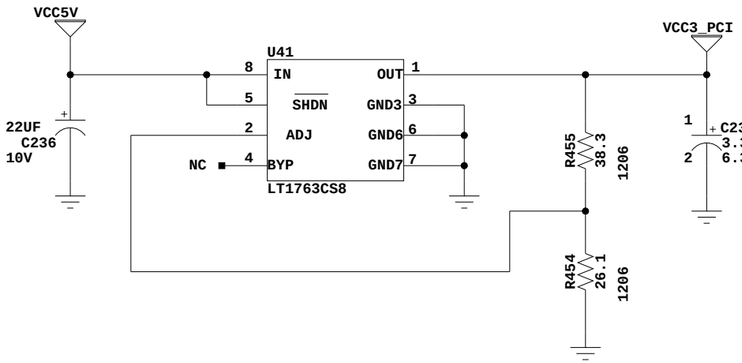


NOTE: TRC_CLK RESISTOR ALLOWS CLOCK TERMINATION
TO BE ADJUSTED INDEPENDENTLY OF OTHER I/O.





NOTE: THE PCI SPEC RECOMMENDS THAT
CLOCKS BE PULLED LOW WHEN THE
BUS IS NOT ACTIVELY CLOCKED.



NOTE: THE COMPONENT VALUES FOR THIS REGULATOR ARE TAKEN
FROM XAPP653. THIS DESIGN IS INTENDED TO SINK CURRENT
THROUGH THE 1206 RESISTORS WHEN THE CLAMP DIODES ON
THE FPGA ARE CONDUCTING DURING OVERSHOOT. THIS IS WHY
THE VALUES ARE UNUSUAL RELATIVE TO THE LT1763 DATASHEET.

NOTE: PCI_CLK RESISTORS ALLOW CLOCK TERMINATION
TO BE ADJUSTED INDEPENDENTLY OF OTHER I/O.

PCI SUPPLY AND TERMINATION

XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
PCI SUPPLY AND TERMINATION

Date:	7-10-2008_10:19	Ver:	C
Sheet Size: B		Rev:	01
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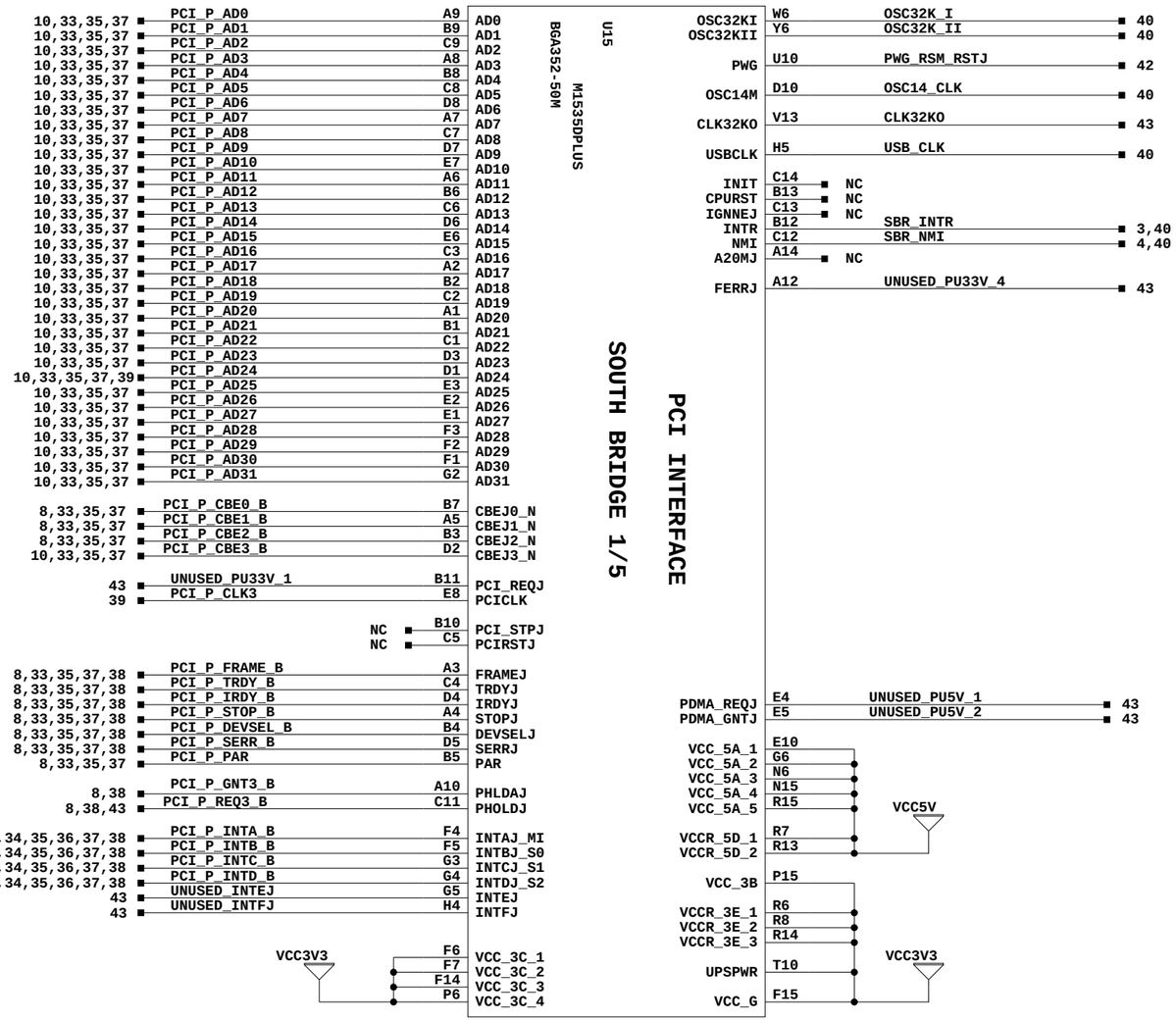

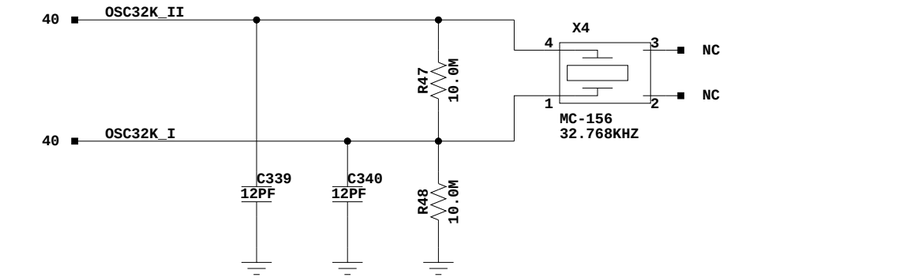

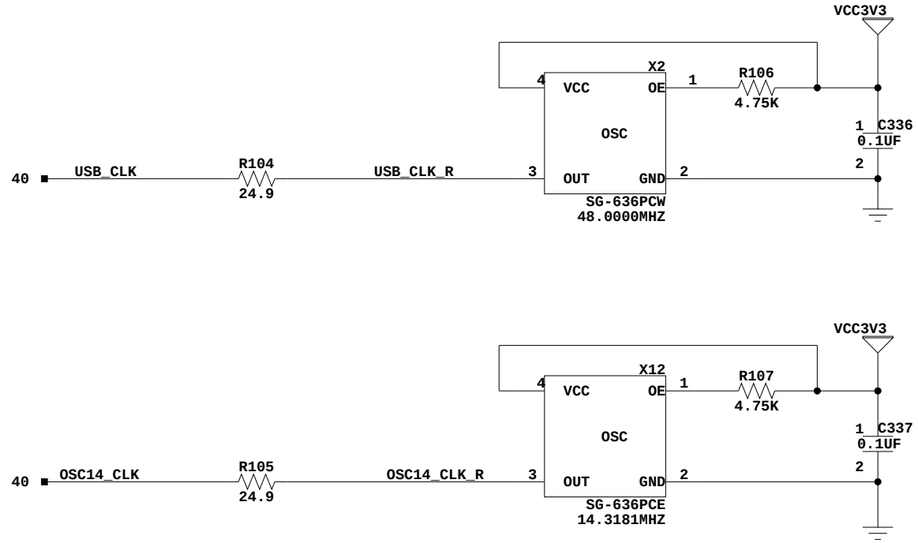

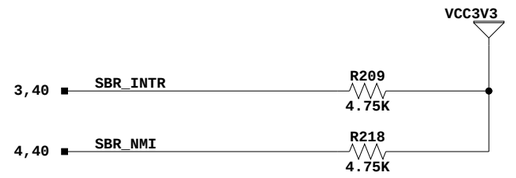

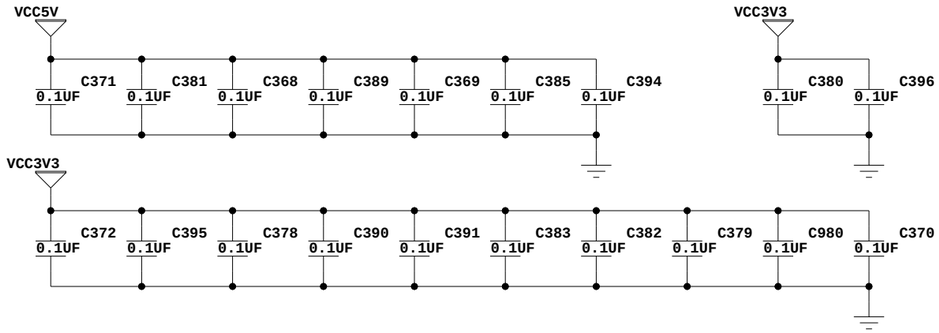

PCI SOUTH BRIDGE, PART 1

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

PCI SOUTH BRIDGE, PART 1

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M1535D+

U15 — B6A352-50M — M1535DPLUS

SOUTH BRIDGE 2/5

PARALLEL PORT	STROBJ	P1	NC
	AUTOFDJ	R1	NC
	PD0	P2	NC
	ERRORJ	T1	NC
	PD1	P3	NC
	PRINITJ	R2	NC
	PD2	N1	NC
	SLCTINJ	R3	NC
	PD3	N2	NC
	PD4	N3	NC
	PD5	N4	NC
	PD6	N5	NC
	PD7	M2	NC
	PRNACKJ	M3	NC
	BUSY	M4	NC
	PE	M5	NC
	SLCT	L5	NC
SERIAL PORT1	SIN1	H2	
	SOUT1	J5	
	RTS1J	H1	
	DTR1J	J3	NC
	CTS1J	J4	
	DSR1J	H3	NC
	DCD1J	G1	NC
	RI1J	J2	NC
SERIAL PORT2	SIN2	K4	
	SOUT2	K2	
	RTS2J	K3	
	DTR2J	L2	NC
	CTS2J	K1	
	DSR2J	K5	NC
	DCD2J	J1	NC
	RI2J	L1	NC
USB PORTS	OVCRJ1	T6	USB1_OVCR_B — 45
	OVCRJ0	T5	USB0_OVCR_B — 45
	USB_PWENJ	V9	USB_POWEN_B — 45
	GPIO22	U5	NC
	GPIO23	U6	NC
	USBP0+	W8	USB0_D_P_R — 45
	USBP0-	V8	USB0_D_N_R — 45
	USBP1+	U9	USB1_D_P_R — 45
	USBP1-	Y7	USB1_D_N_R — 45
	USBP2+	W7	NC
	USBP2-	V7	UNUSED_PD_1 — 43
	USBP3+	U8	NC
	USBP3-	T8	UNUSED_PD_2 — 43
IrDA	IRRXH	L4	UNUSED_PD_3 — 43
	IRRX	L3	UNUSED_PD_4 — 43
	IRTX	M1	NC
KEYBRD MOUSE	KBCLK	U11	KBCLK_R — 45
	KBDATA	U12	KBDATA_R — 45
	KBINH	V12	KBINH — 41,62
	MSCLK	T11	MSCLK_R — 45
	MSDATA	T12	MSDATA_R — 45

M1535D+

U15 — B6A352-50M — M1535DPLUS

SOUTH BRIDGE 3/5

IDE INTERFACE

GROUP F
VCC=3.3V

	PIDED0	G17	PIDE_D0_R — 46
	PIDED1	F20	PIDE_D1_R — 46
	PIDED2	F18	PIDE_D2_R — 46
	PIDED3	F16	PIDE_D3_R — 46
	PIDED4	E19	PIDE_D4_R — 46
	PIDED5	D20	PIDE_D5_R — 46
	PIDED6	D18	PIDE_D6_R — 46
	PIDED7	B20	PIDE_D7_R — 46
	PIDED8	C20	PIDE_D8_R — 46
	PIDED9	D19	PIDE_D9_R — 46
	PIDED10	E18	PIDE_D10_R — 46
	PIDED11	E20	PIDE_D11_R — 46
	PIDED12	F17	PIDE_D12_R — 46
	PIDED13	F19	PIDE_D13_R — 46
	PIDED14	G16	PIDE_D14_R — 46
	PIDED15	G18	PIDE_D15_R — 46
	PIDEA0	H20	PIDE_A0_R — 46
	PIDEA1	H19	PIDE_A1_R — 46
	PIDEA2	J16	PIDE_A2_R — 46
	SIRQI	N16	PIDE_INTRQ_R — 46
	PIDEDRQ	G19	PIDE_DMARQ_R — 46
	PIDEDAKJ	H18	PIDE_DMACK_B_R — 46
	PIDERDY	H17	PIDE_IORDY_R — 46
	PIDEIORJ	H16	PIDE_DIOR_B_R — 46
	PIDEIOWJ	G20	PIDE_DIOW_B_R — 46
	PIDECS1J	J17	PIDE_CS1_B_R — 46
	PIDECS3J	J18	PIDE_CS3_B_R — 46
	CBLID_P	D11	PIDE_PDIAG_B_R — 46
	SIDED0	A17	SIDE_D0_R — 46
	SIDED1	D16	SIDE_D1_R — 46
	SIDED2	B16	SIDE_D2_R — 46
	SIDED3	E15	SIDE_D3_R — 46
	SIDED4	C15	SIDE_D4_R — 46
	SIDED5	A15	SIDE_D5_R — 46
	SIDED6	D14	SIDE_D6_R — 46
	SIDED7	E13	SIDE_D7_R — 46
	SIDED8	D13	SIDE_D8_R — 46
	SIDED9	E14	SIDE_D9_R — 46
	SIDED10	B15	SIDE_D10_R — 46
	SIDED11	D15	SIDE_D11_R — 46
	SIDED12	A16	SIDE_D12_R — 46
	SIDED13	C16	SIDE_D13_R — 46
	SIDED14	E16	SIDE_D14_R — 46
	SIDED15	B17	SIDE_D15_R — 46
	SIDEA0	A19	SIDE_A0_R — 46
	SIDEA1	C18	SIDE_A1_R — 46
	SIDEA2	B19	SIDE_A2_R — 46
	SIRQII	P16	SIDE_INTRQ_R — 46
	SIDEDRQ	C17	SIDE_DMARQ_R — 46
	SIDEDAKJ	B18	SIDE_DMACK_B_R — 46
	SIDERDY	A18	SIDE_IORDY_R — 46
	SIDEIORJ	E17	SIDE_DIOR_B_R — 46
	SIDEIOWJ	D17	SIDE_DIOW_B_R — 46
	SIDECS1J	C19	SIDE_CS1_B_R — 46
	SIDECS3J	A20	SIDE_CS3_B_R — 46
	CBLID_S	E11	SIDE_PDIAG_B_R — 46
	VCC_F1	G15	VCC3V3
	VCC_F2	K16	VCC3V3

VCC5V

41,62 — KBINH — R202 — 4.75K

PCI SOUTH BRIDGE, PART 2-3

XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

PCI SOUTH BRIDGE, PART 2-3

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M1535D+

U15 — M1535DPLUS — BGA352-50M

POWER MANAGEMENT UNIT1

RSM_RSTJ	W10	PWG_RSM_RSTJ	40,42
SUSPENDJ	W13	NC	
PWRBTNJ	Y15	UNUSED_PU33V_5	43
SLPBTNJ	V10	UNUSED_PU33V_6	43
OFF_PWR0	V14	NC	
OFF_PWR1	W14	NC	
OFF_PWR2	Y14	NC	
SPLED	Y13	SPLED	43
RSM_ENT0	W11	RSM_ENT0	43
RSM_ENT1	Y11	UNUSED_PU5V_3	43
RSM_ENT8	Y10	UNUSED_PD_5	43
PMEJ	W12	UNUSED_PU33V_7	43
RI	V11	UNUSED_PD_6	43
IRQ8J	Y12	UNUSED_PU5V_4	43
RSM_ENT3	T9	UNUSED_PD_7	43

POWER MANAGEMENT UNIT2

SMIJ	A13	NC	
STPCLKJ	B14	NC	
SLEEPJ	D12	NC	
ZZ	E12	UNUSED_PU5V_5	43
NUINP1	A11	UNUSED_PD_8	43
CPU_STPJ	C10	NC	
THRMJ	T18	IIC_THERM_B	4,55
SQWO	V6	SQWO	43
SMBCLK	T7	SMB_SCL	42
SMBDATA	U7	SMB_SDA	42
SMBALERTJ	T2	IIC_ALERT_B	4,55
GPI25	E9	NC	
GPO34	P18	GPO_34	43
GPO35	P19	GPO_35	43

AC97 INTERFACE

ACRESETJ	Y9	AC_RESET_B	47
ACSDATA_IN0	W9	AC_SDATA_IN0	47
ACSDATA_IN1	Y8	UNUSED_PD_9	43
ACSDATA_OUT	U1	AC_SDATA_OUT	47
ACSYNC	P4	AC_SYNC	47
ACBIT_CLK	P5	AC_BIT_CLK	47
ACMIDI_TXD	R4	NC	
ACMIDI_RXD	T4	UNUSED_PD_10	43

SOUND CNTRL

ACGAME0	V1	NC	
ACGAME1	V2	NC	
ACGAME2	V3	NC	
ACGAME3	W1	NC	
ACGAME4	W2	NC	
ACGAME5	W3	NC	
ACGAME6	Y1	NC	
ACGAME7	Y2	NC	
ACGP_UPJ	U3	UNUSED_PU5V_7	43
ACGP_MUTEJ	U2	UNUSED_PU5V_8	43
ACGP_DOWNJ	R5	UNUSED_PU5V_9	43
FANOUT1	W5	NC	
FANOUT2	V5	NC	
FANIN2	Y5	UNUSED_PU5V_6	43
SPDIF_OUT	D9	NC	
SPDIF_IN	U4	UNUSED_PU5V_10	43

SOUTH BRIDGE 4/5

M1535D+

U15 — M1535DPLUS — BGA352-50M

XD(ISA) BUS

XD0	U20	NC	
XD1	U19	NC	
XD2	U18	NC	
XD3	Y20	NC	
XD4	W20	NC	
XD5	V20	NC	
XD6	Y19	NC	
XD7	W19	NC	
SA0	V19	NC	
SA1	Y18	NC	
SA2	W18	NC	
SA3	V18	NC	
SA4	Y17	NC	
SA5	W17	NC	
SA6	V17	NC	
SA7	U17	NC	
SA8	T17	NC	
SA9	R17	NC	
SA10	Y16	NC	
SA11	W16	NC	
SA12	V16	NC	
SA13	U16	NC	
SA14	T16	NC	
SA15	W15	NC	
BIOSA16	V15	NC	
BIOSA17	U15	NC	
BIOSA18	T15	NC	
MEMRJ	T14	UNUSED_PU5V_19	43
MEMWJ	U14	UNUSED_PU5V_20	43
IORJ	T13	NC	
IOWJ	U13	NC	

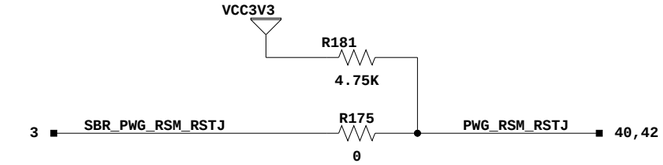
FLOPPY DISK

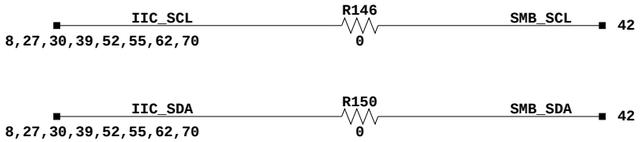
RDATAJ	M18	UNUSED_PU5V_11	43
WGATEJ	L19	NC	
WDATAJ	L18	NC	
HDSELJ	M19	NC	
FD_DIRJ	L16	NC	
STEPJ	L17	NC	
DSKCHGJ	M20	UNUSED_PU5V_12	43
DRV0J	K19	NC	
DRV1J	K20	NC	
MOT0J	K17	NC	
MOT1J	K18	NC	
WPROTJ	M16	UNUSED_PU5V_13	43
TRK0J	L20	UNUSED_PU5V_14	43
INDEXJ	J20	UNUSED_PU5V_15	43
DENSEL	J19	NC	

MISCELLANEOUS LOGIC

SPKR	T19	SPKR	47,62
RTCAS	R20	NC	
RTCRW	R19	NC	
RTCDS	R18	NC	
ROMKBCSJ	T20	ROMKBCSJ	43
IRQSER	N19	UNUSED_PU5V_16	43
GPI24	M17	NC	
GPO29	N17	GPO_29	43
GPO30	N18	GPO_30	43
PCSOJ	P20	PCS0J	43
PCS1J	R16	PCS1J	43
RUN_ENT0	Y3	NC	
RUN_ENT1	V4	NC	
RUN_ENT2	W4	NC	
RUN_ENT3	Y4	NC	
GPO10	T3	NC	
LFRAMEJ	N20	UNUSED_PU5V_17	43
LDRQJ	P17	UNUSED_PU5V_18	43

SOUTH BRIDGE 5/5





PCI SOUTH BRIDGE, PART 4-5

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

PCI SOUTH BRIDGE, PART 4-5

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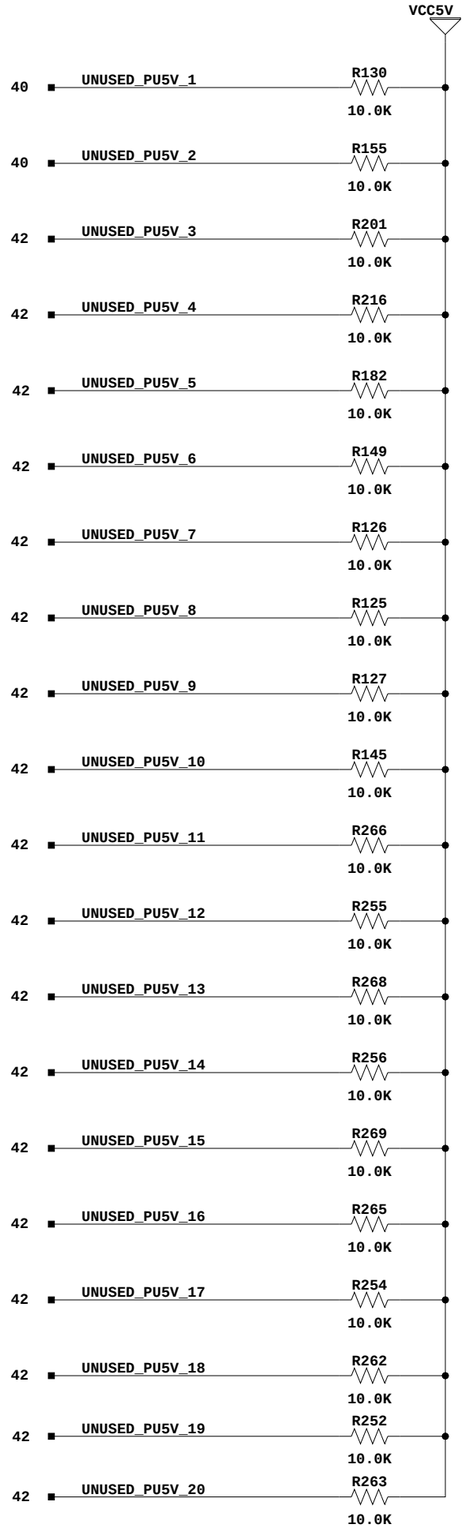

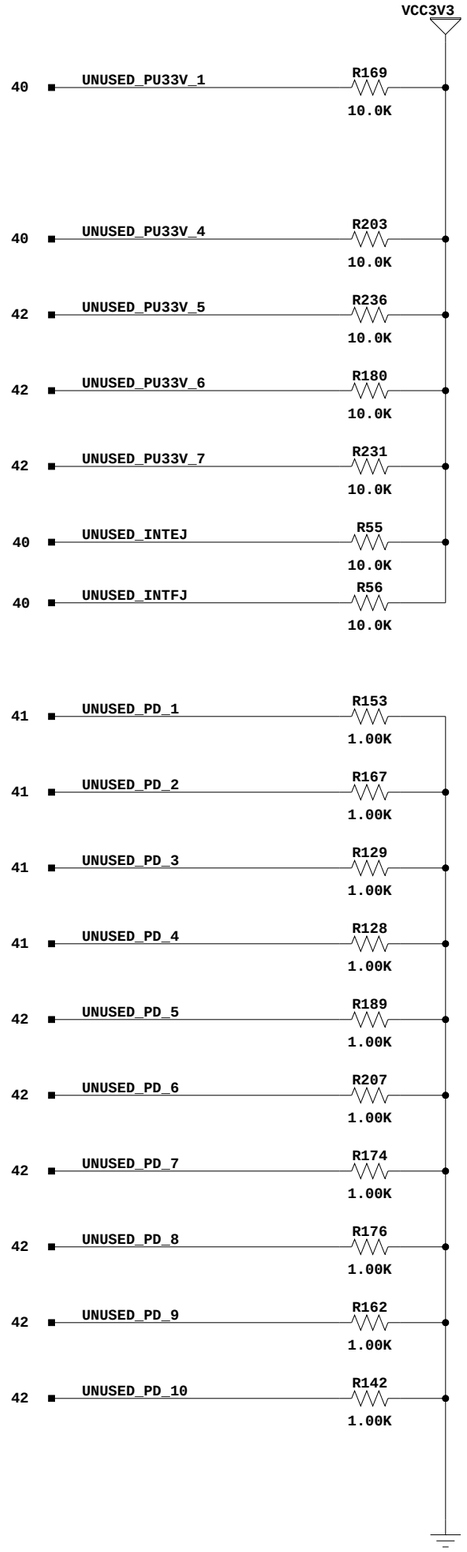

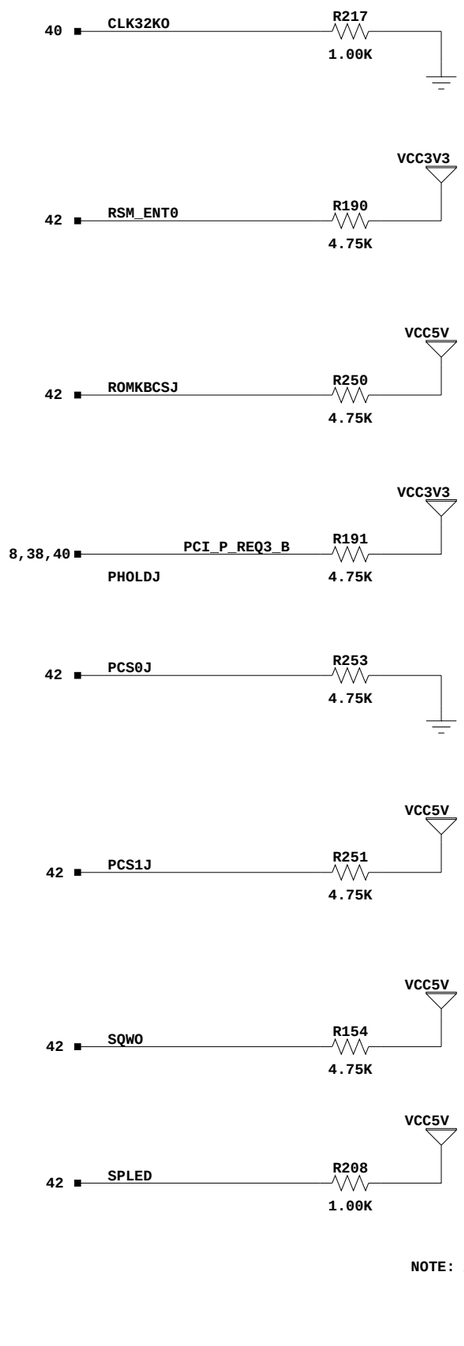

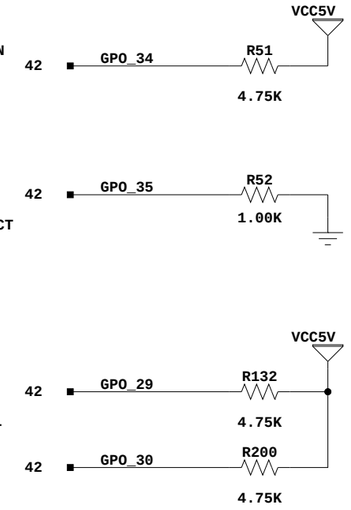

NOTE: AT MODE IS USED HERE TO DISABLE THE SOFT-POWER FUNCTIONALITY OF THE SOUTH BRIDGE

PCI SOUTH BRIDGE, CONFIG and UNUSED

XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
PCI SOUTH BRIDGE, UNUSED PIN RESISTORS

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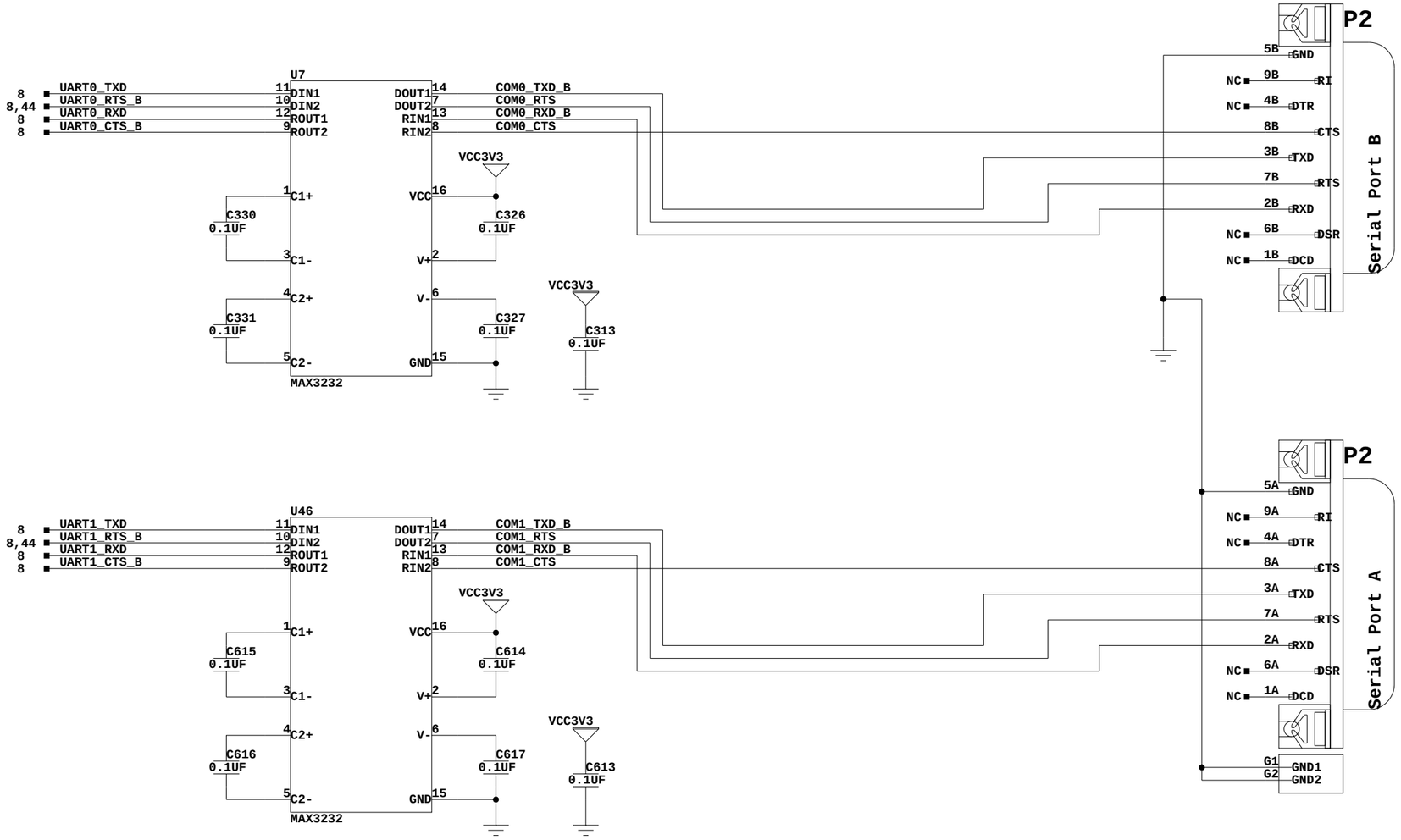

Silkscreen:
"COM 1"

Silkscreen:
"COM 2"

RS232 SERIAL PORT INTERFACE

XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
RS232 SERIAL PORT INTERFACE

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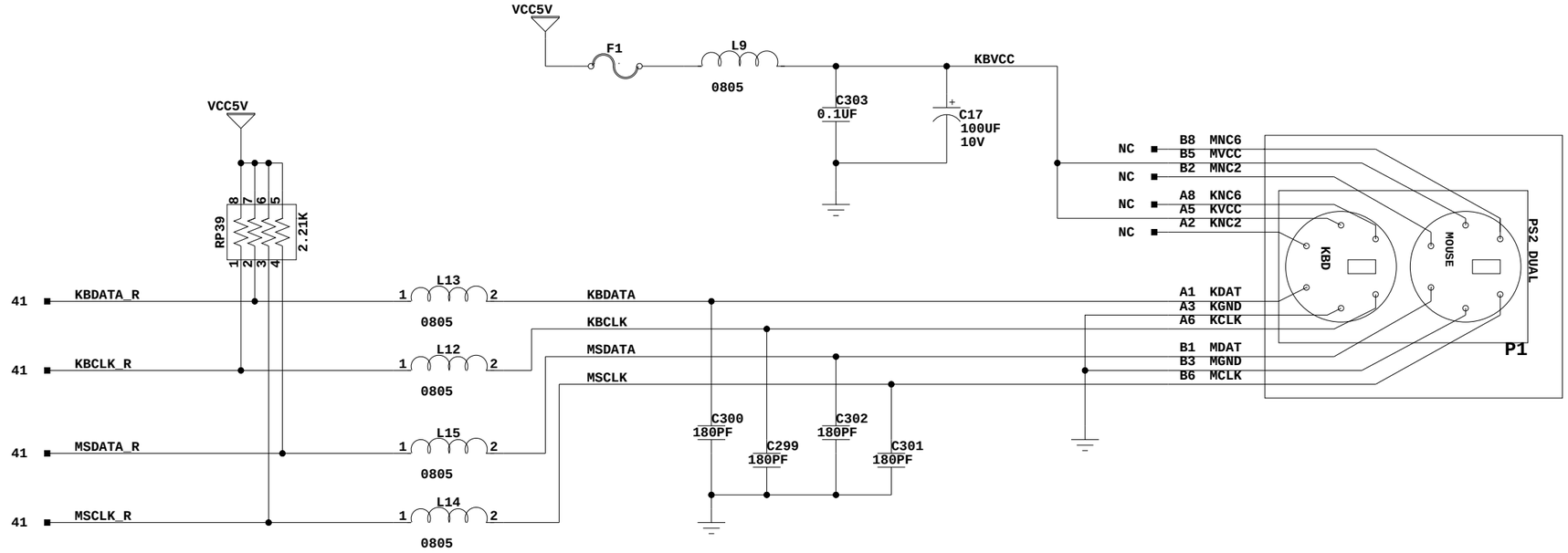

KBD/MOUSE AND USB INTERFACES

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

KBD/MOUSE AND USB INTERFACES

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Pin 20 must be removed.
Silkscreen:
"IDE PRIMARY"

RP51
41 PIDE_D7_R 8 PIDE_D7 46
41 PIDE_D8_R 7 PIDE_D8 46
41 PIDE_D6_R 6 PIDE_D6 46
41 PIDE_D9_R 5 PIDE_D9 46
47.5

RP50
41 PIDE_D5_R 8 PIDE_D5 46
41 PIDE_D10_R 7 PIDE_D10 46
41 PIDE_D4_R 6 PIDE_D4 46
41 PIDE_D11_R 5 PIDE_D11 46
47.5

RP49
41 PIDE_D3_R 8 PIDE_D3 46
41 PIDE_D12_R 7 PIDE_D12 46
41 PIDE_D2_R 6 PIDE_D2 46
41 PIDE_D13_R 5 PIDE_D13 46
47.5

RP48
41 PIDE_D1_R 8 PIDE_D1 46
41 PIDE_D14_R 7 PIDE_D14 46
41 PIDE_D0_R 6 PIDE_D0 46
41 PIDE_D15_R 5 PIDE_D15 46
47.5

41 PIDE_DMARQ_R 1 R303 2 PIDE_DMARQ 46
82.0

RP47
41 PIDE_DIOW_B_R 8 PIDE_DIOW_B 46
41 PIDE_DIOR_B_R 7 PIDE_DIOR_B 46
41 PIDE_IORDY_R 6 PIDE_IORDY 46
41 PIDE_DMACK_B_R 5 PIDE_DMACK_B 46
33.2

41 PIDE_INTRQ_R 1 R301 2 PIDE_INTRQ 46
82.0

RP46
41 PIDE_A1_R 8 PIDE_A1 46
41 PIDE_A0_R 7 PIDE_A0 46
41 PIDE_A2_R 6 PIDE_A2 46
41 PIDE_CS1_B_R 5 PIDE_CS1_B 46
33.2

41 PIDE_CS3_B_R R302 PIDE_CS3_B 46
33.2

41 PIDE_PDIAG_B_R R304 PIDE_PDIAG_B 46
0

VCC3V3
46 PIDE_IORDY R311 10.0K
46 PIDE_INTRQ R306 4.75K
46 PIDE_D7 R313 10.0K
46 PIDE_DMARQ R309 5.62K
46 PIDE_CSEL R299 475
46 PIDE_PDIAG_B R314 100K
C425
0.047UF

Mark Pin 1
Pin20=Key
J16

46 PIDE_RESET_B 1
2
46 PIDE_D7 3
46 PIDE_D8 4
46 PIDE_D6 5
46 PIDE_D9 6
46 PIDE_D5 7
46 PIDE_D10 8
46 PIDE_D4 9
46 PIDE_D11 10
46 PIDE_D3 11
46 PIDE_D12 12
46 PIDE_D2 13
46 PIDE_D13 14
46 PIDE_D1 15
46 PIDE_D14 16
46 PIDE_D0 17
46 PIDE_D15 18
19
46 PIDE_DMARQ 21
22
46 PIDE_DIOW_B 23
24
46 PIDE_DIOR_B 25
26
46 PIDE_IORDY 27
46 PIDE_CSEL 28
46 PIDE_DMACK_B 29
30
46 PIDE_INTRQ 31
NC 32
PIDE_A1 33
46 PIDE_PDIAG_B 34
46 PIDE_A0 35
46 PIDE_A2 36
46 PIDE_CS1_B 37
46 PIDE_CS3_B 38
46,62 PIDE_DASP_B 39
40
CON_IDE40

IDE PRIMARY CONN

VCC3V3
R305 180Z
GREEN
DS22
46,62 PIDE_DASP_B

Silkscreen:
"IDE P LED"

4,46 SBR_IDE_RST_B R288 SIDE_RESET_B 46
0
4,46 SBR_IDE_RST_B R300 PIDE_RESET_B 46
0

Pin 20 must be removed.
Silkscreen:
"IDE SECONDARY"

RP40
41 SIDE_D7_R 8 SIDE_D7 46
41 SIDE_D8_R 7 SIDE_D8 46
41 SIDE_D6_R 6 SIDE_D6 46
41 SIDE_D9_R 5 SIDE_D9 46
47.5

RP41
41 SIDE_D5_R 8 SIDE_D5 46
41 SIDE_D10_R 7 SIDE_D10 46
41 SIDE_D4_R 6 SIDE_D4 46
41 SIDE_D11_R 5 SIDE_D11 46
47.5

RP42
41 SIDE_D3_R 8 SIDE_D3 46
41 SIDE_D12_R 7 SIDE_D12 46
41 SIDE_D2_R 6 SIDE_D2 46
41 SIDE_D13_R 5 SIDE_D13 46
47.5

RP44
41 SIDE_D1_R 8 SIDE_D1 46
41 SIDE_D14_R 7 SIDE_D14 46
41 SIDE_D0_R 6 SIDE_D0 46
41 SIDE_D15_R 5 SIDE_D15 46
47.5

41 SIDE_DMARQ_R 1 R291 2 SIDE_DMARQ 46
82.0

RP43
41 SIDE_DIOW_B_R 8 SIDE_DIOW_B 46
41 SIDE_DIOR_B_R 7 SIDE_DIOR_B 46
41 SIDE_IORDY_R 6 SIDE_IORDY 46
41 SIDE_DMACK_B_R 5 SIDE_DMACK_B 46
33.2

41 SIDE_INTRQ_R 1 R289 2 SIDE_INTRQ 46
82.0

RP45
41 SIDE_A1_R 8 SIDE_A1 46
41 SIDE_A0_R 7 SIDE_A0 46
41 SIDE_A2_R 6 SIDE_A2 46
41 SIDE_CS1_B_R 5 SIDE_CS1_B 46
33.2

41 SIDE_CS3_B_R R292 SIDE_CS3_B 46
33.2

41 SIDE_PDIAG_B_R R290 SIDE_PDIAG_B 46
0

VCC3V3
46 SIDE_IORDY R312 10.0K
46 SIDE_INTRQ R305 4.75K
46 SIDE_D7 R307 10.0K
46 SIDE_DMARQ R310 5.62K
46 SIDE_CSEL R287 475
46 SIDE_PDIAG_B R308 100K
C424
0.047UF

Mark Pin 1
Pin20=Key
J15

46 SIDE_RESET_B 1
2
46 SIDE_D7 3
46 SIDE_D8 4
46 SIDE_D6 5
46 SIDE_D9 6
46 SIDE_D5 7
46 SIDE_D10 8
46 SIDE_D4 9
46 SIDE_D11 10
46 SIDE_D3 11
46 SIDE_D12 12
46 SIDE_D2 13
46 SIDE_D13 14
46 SIDE_D1 15
46 SIDE_D14 16
46 SIDE_D0 17
46 SIDE_D15 18
19
46 SIDE_DMARQ 21
22
46 SIDE_DIOW_B 23
24
46 SIDE_DIOR_B 25
26
46 SIDE_IORDY 27
46 SIDE_CSEL 28
46 SIDE_DMACK_B 29
30
46 SIDE_INTRQ 31
NC 32
SIDE_A1 33
46 SIDE_PDIAG_B 34
46 SIDE_A0 35
46 SIDE_A2 36
46 SIDE_CS1_B 37
46 SIDE_CS3_B 38
46,62 SIDE_DASP_B 39
40
CON_IDE40

IDE SECONDARY CONN

VCC3V3
R287 182
GREEN
DS21
46,62 SIDE_DASP_B

Silkscreen:
"IDE S LED"

IDE INTERFACES

XILINX

SCH P/N 0381255
ART P/N 0532059
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Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
IDE INTERFACES

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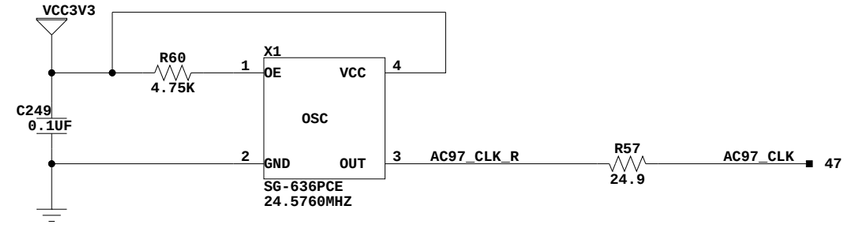
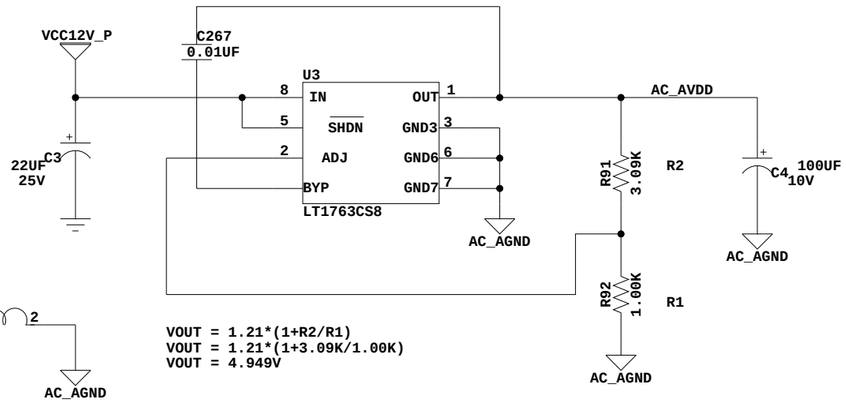
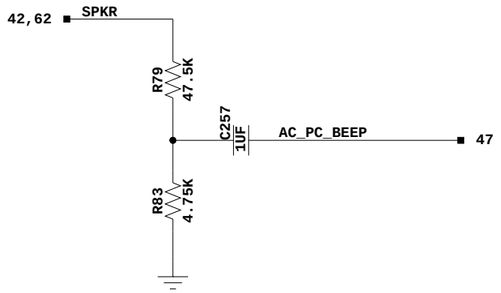
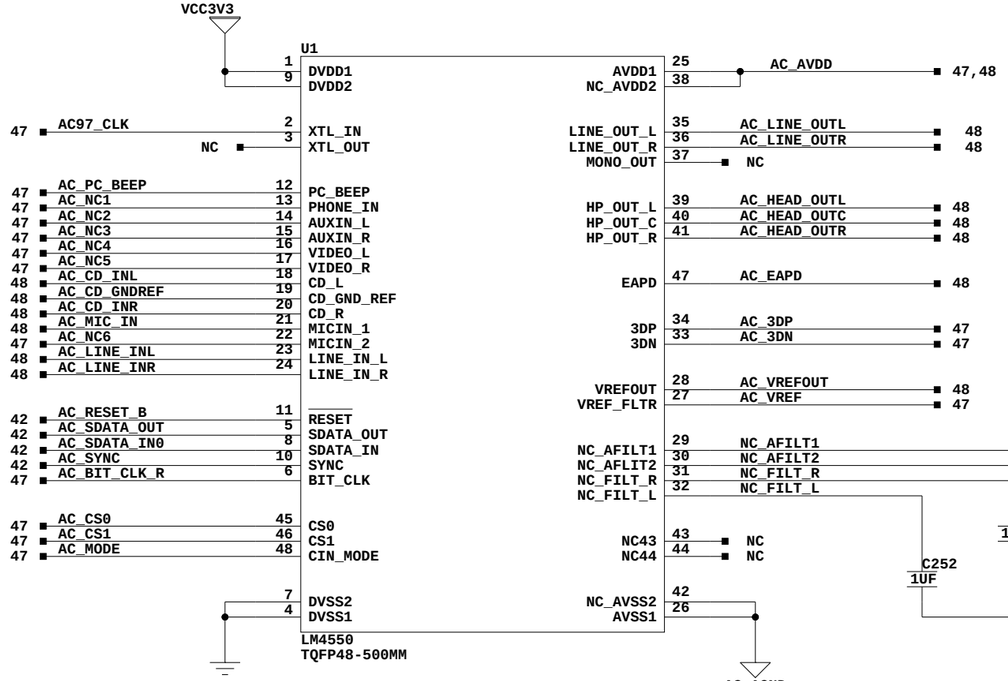
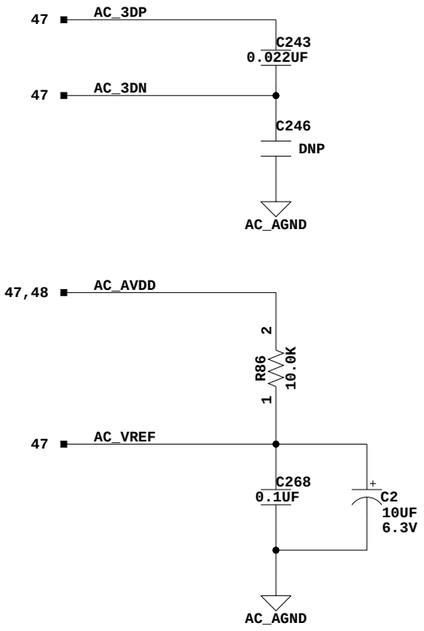
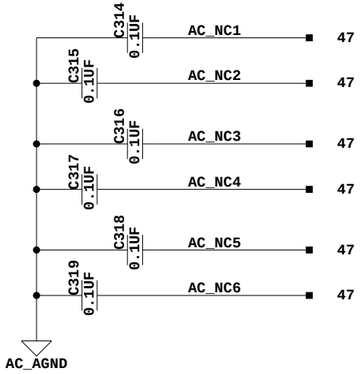


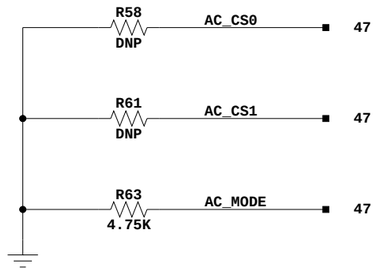


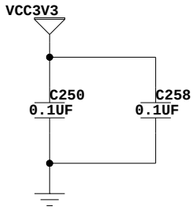


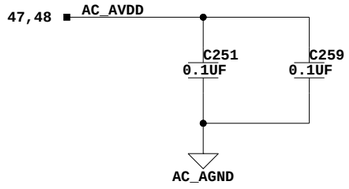












AC97 CODEC

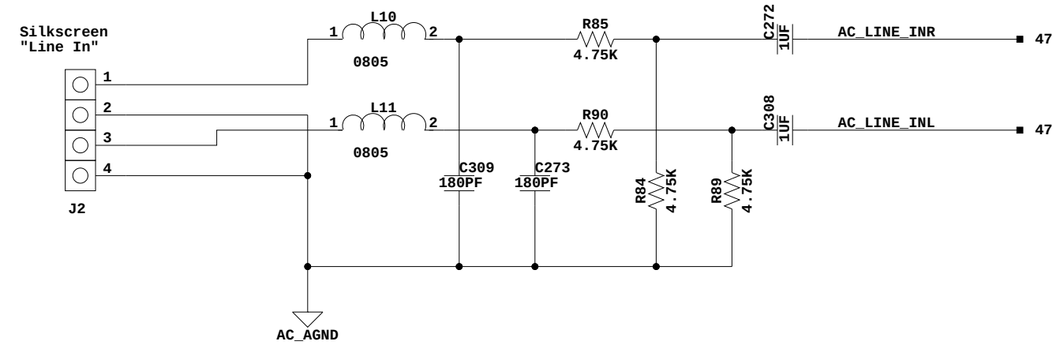
XILINX

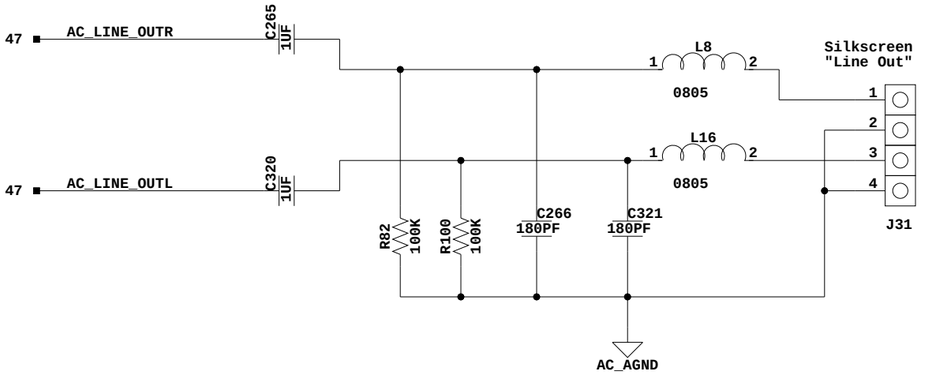
SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

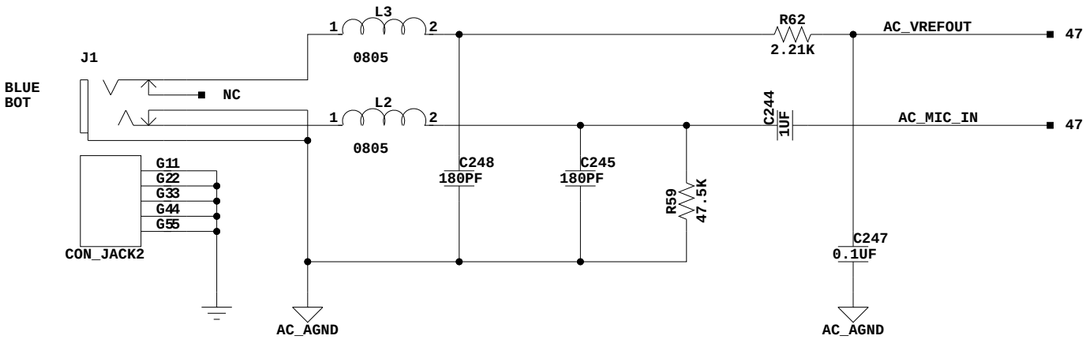
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

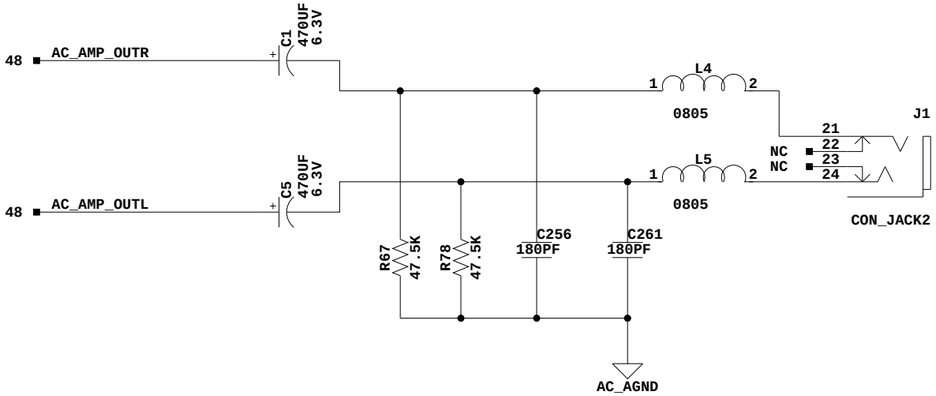
AC97 CODEC

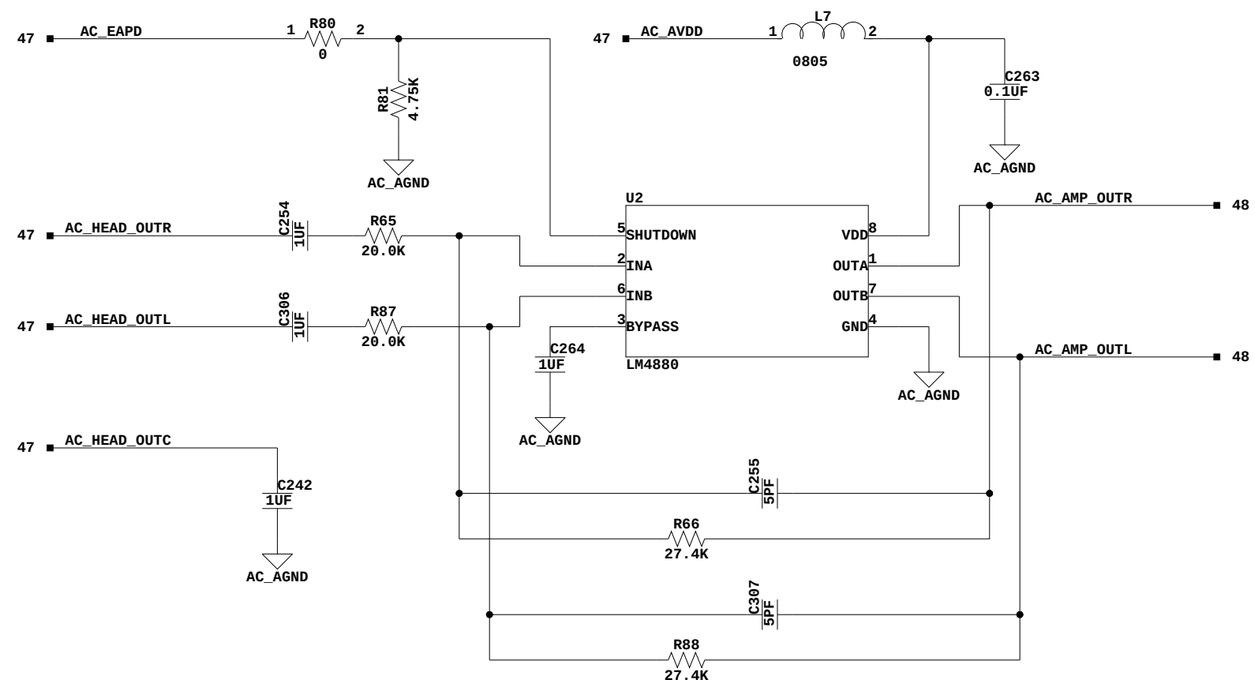
Date:	8-1-2008_15:08	Ver:	C
Sheet Size: B		Rev:	01
Sheet	47 of 70	Drawn By	BF

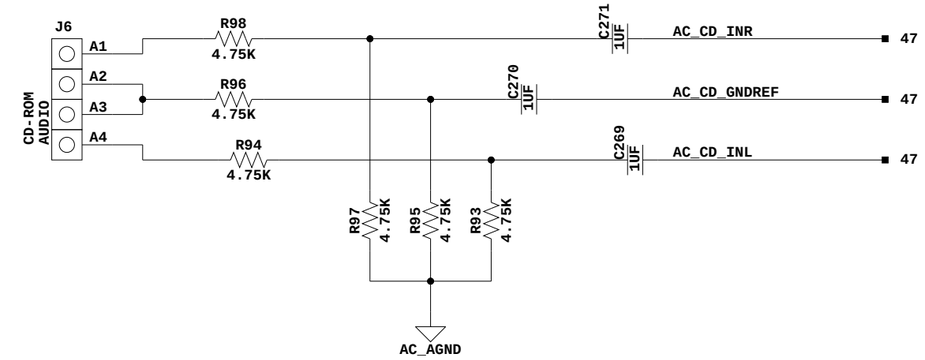












AC97 CONNECTORS

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
AC97 CONNECTORS

Date:	7-10-2008_10:19	Ver:	C
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SGMII: GTP 124_0

NOTE:
PHY ADDR = '00111'

NOTE:
BOTTOM SGMII

10/100/1000 RJ45 AND MAGNETICS

DEVICE=RJ45_JC0-0019
P7
PARTS=1
LEVEL=STD
PKG_TYPE=RJ45_JC0-0019

NC=25,26

PHY0_RX* signals must be time-of-flight matched to each other

PHY0_TX* signals must be time-of-flight matched to each other

J50, J28 1-2: GMII/MII to Cu (Default)
J50, J28 2-3: SGMII to Cu, no clk
J50 1-2, J49 ON: RGMII, modified MII in Cu

MII / RGMII / SGMII TRI-MODE ETHERNET PHY

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
MII / RGMII / SGMII TRI-MODE ETHERNET PHY

Date: 8-1-2008_15:08	Ver: C
Sheet Size: B	Rev: 01
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SGMII: GTP 124_1

NOTE:
PHY ADDR = ‘00111’

NOTE:
BOTTOM SGMII

10/100/1000 RJ45 AND MAGNETICS

DEVICE=RJ45_JC0-0019
P7
PARTS=1
LEVEL=STD
PKG_TYPE=RJ45_JC0-0019

M88E1111_PQFP128R
PQFP-128R
U53

SGMII TRI-MODE ETHERNET PHY

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

SGMII TRI-MODE ETHERNET PHY

Date:	7-10-2008_10:19	Ver:	C
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SATA Host 1

GTP 120_1

SATA Host 2

GTP 120_0

SATA INTERFACE

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

SATA INTERFACE

Date:	7-10-2008_10:19	Ver:	C
Sheet Size: B		Rev:	01
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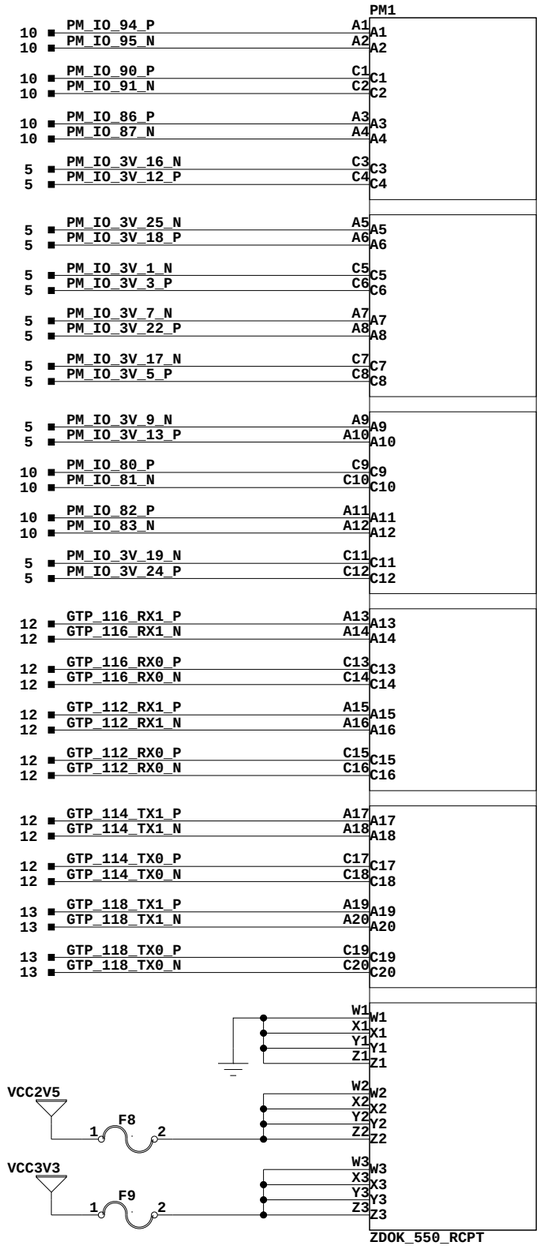

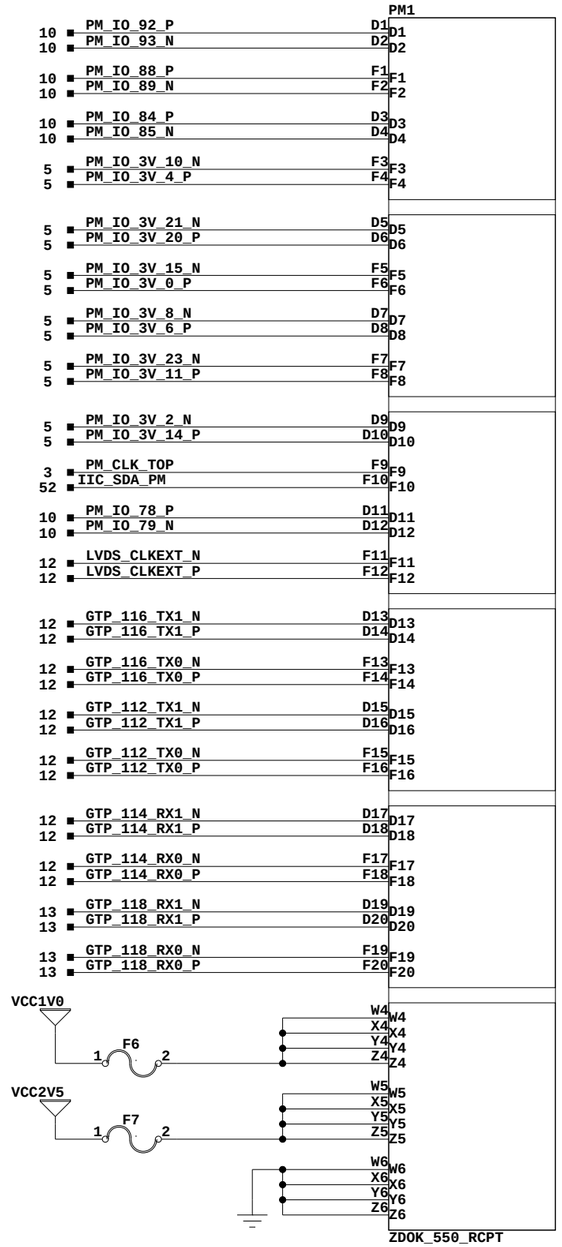

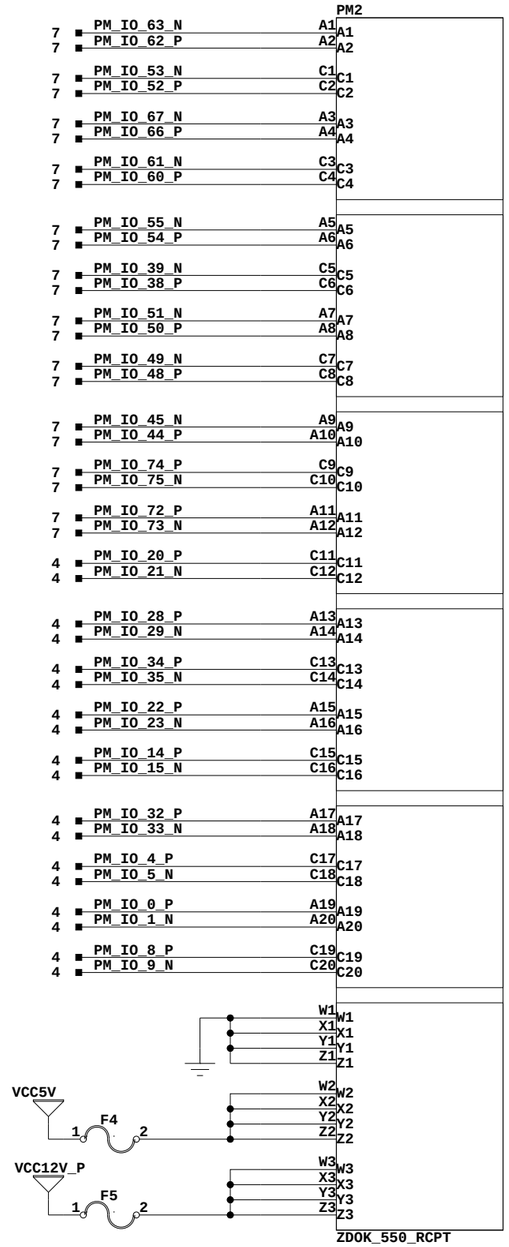

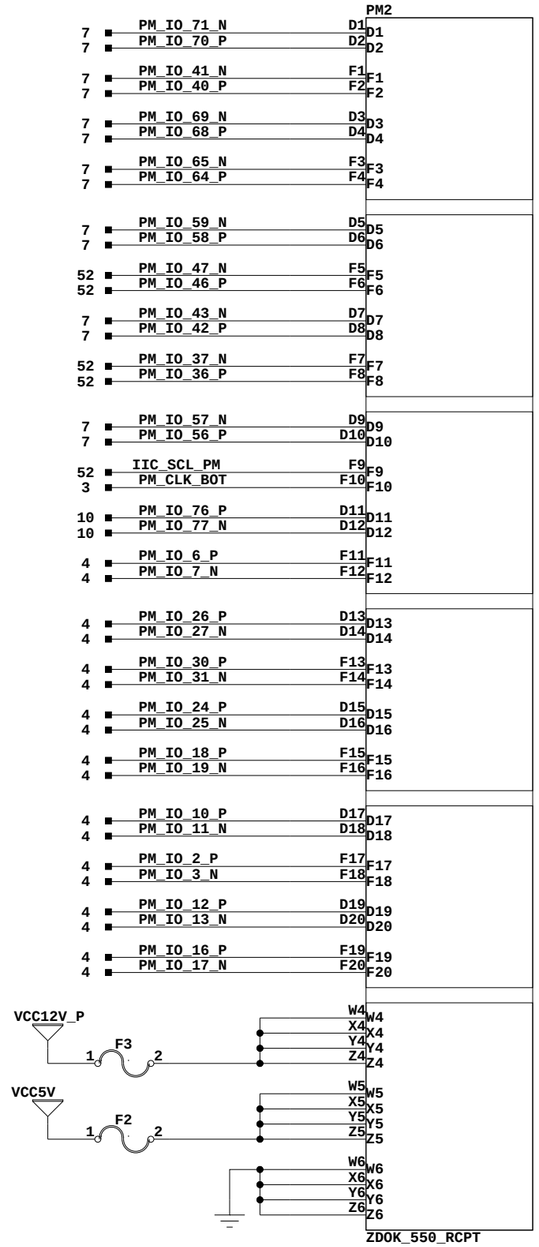

GND;B1,B2,B3,B4,B5
GND;B6,B7,B8,B9,B10
GND;B11,B12,B13,B14,B15
GND;B16,B17,B18,B19,B20
GND;E1,E2,E3,E4,E5
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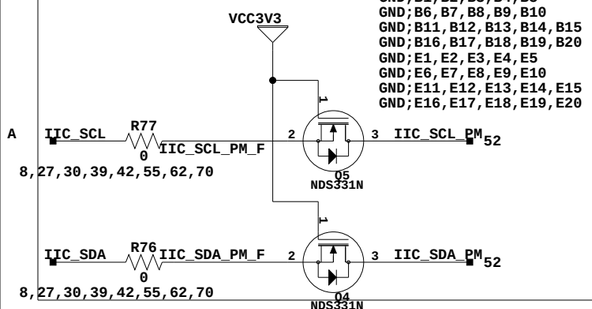
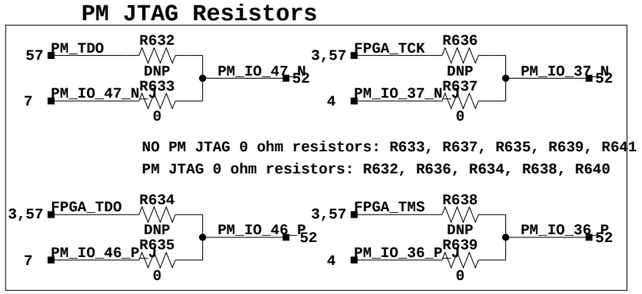
GND;E16,E17,E18,E19,E20



PM JTAG Resistors



GND;B1,B2,B3,B4,B5
GND;B6,B7,B8,B9,B10
GND;B11,B12,B13,B14,B15
GND;B16,B17,B18,B19,B20
GND;E1,E2,E3,E4,E5
GND;E6,E7,E8,E9,E10
GND;E11,E12,E13,E14,E15
GND;E16,E17,E18,E19,E20

PERSONALITY MODULE CONNECTORS

XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

PERSONALITY MODULE CONNECTORS

Date:	8-1-2008_15:08	Ver:	C
Sheet Size: B		Rev:	01
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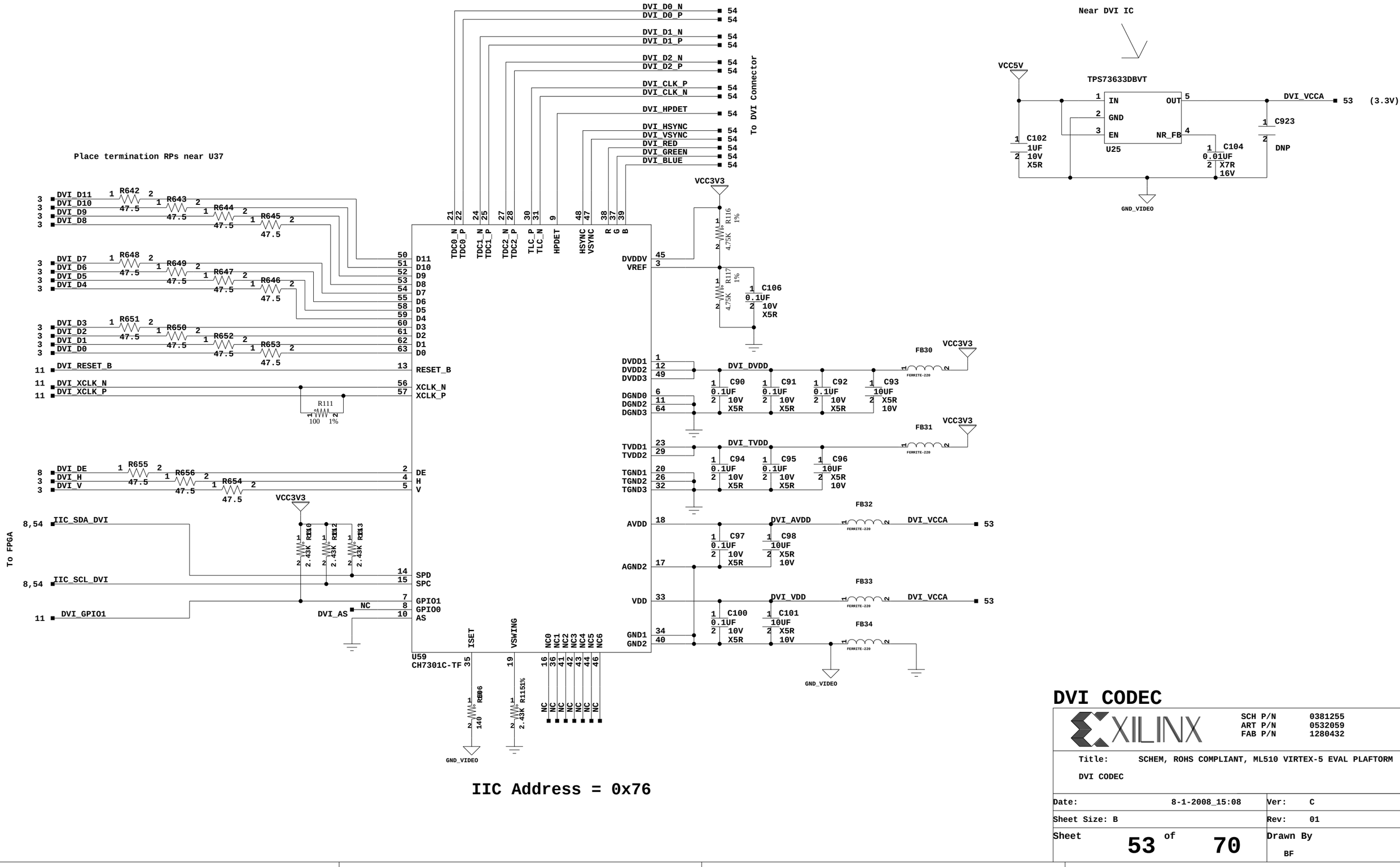


IIC Address = 0x76

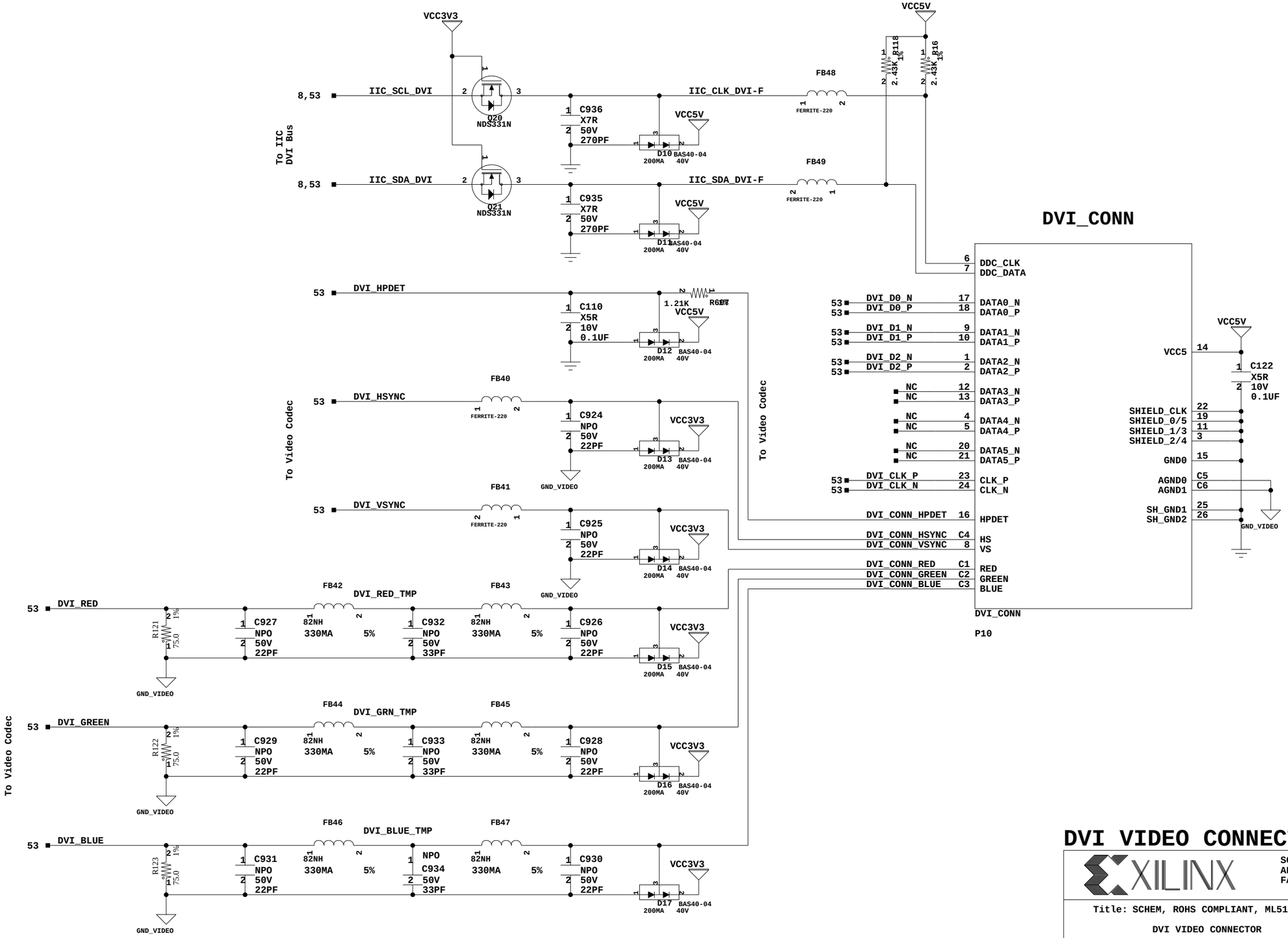
DVI CODEC

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

DVI CODEC

Date: 8-1-2008_15:08	Ver: C
Sheet Size: B	Rev: 01
Sheet 53 of 70	Drawn By BF



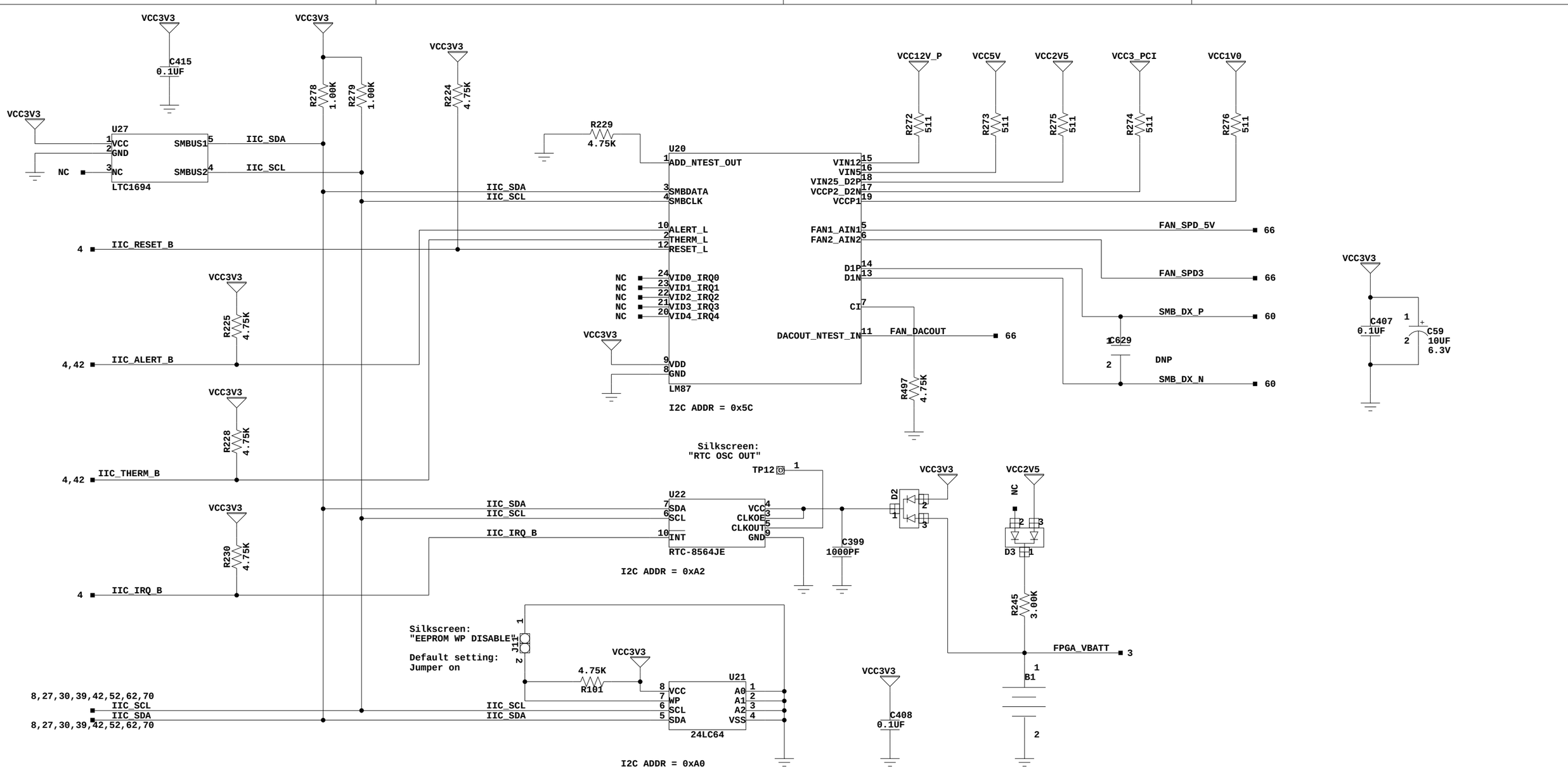
DVI VIDEO CONNECTOR

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

DVI VIDEO CONNECTOR

Date:	7-10-2008_10:19	Ver:	C
Sheet Size: B		Rev:	01
Sheet	54 of 70	Drawn By	BF



I2C AND SPI DEVICES

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

I2C AND SPI DEVICES

Date:	8-1-2008_15:08	Ver:	C
Sheet Size: B		Rev:	01
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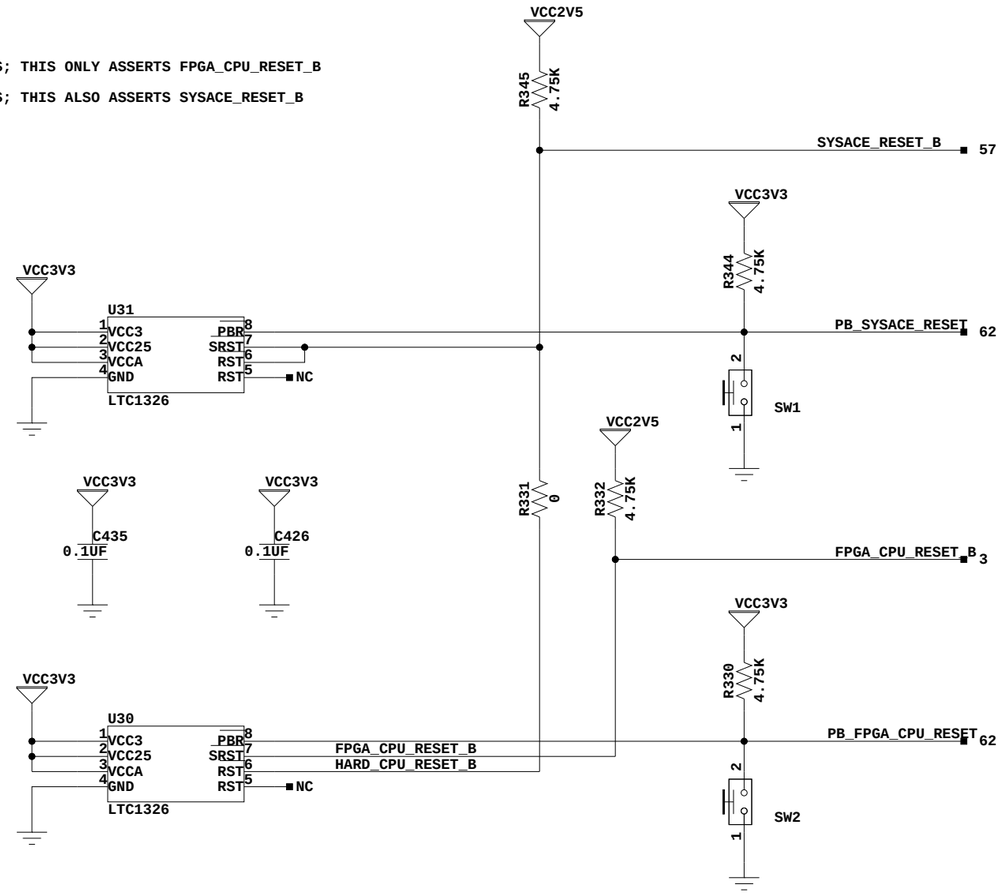
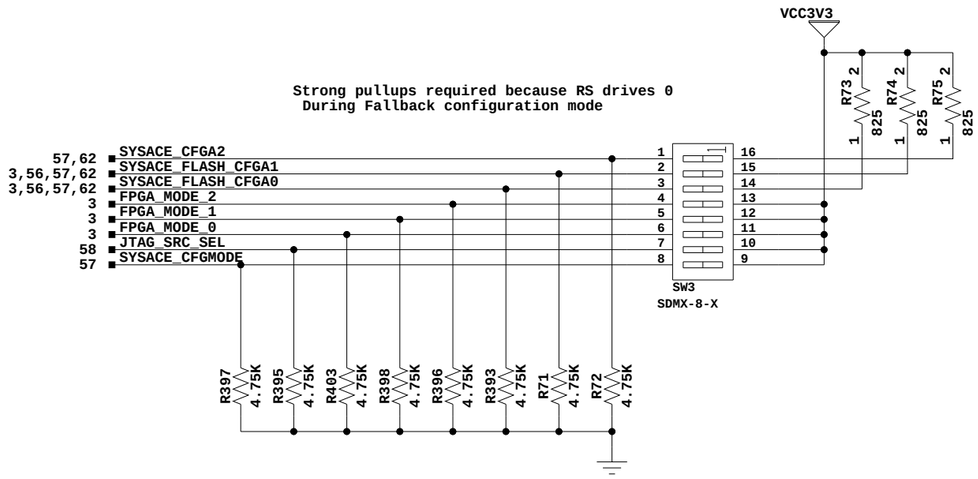
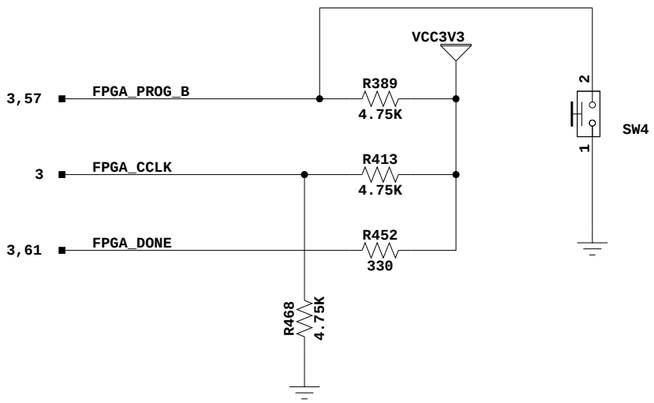


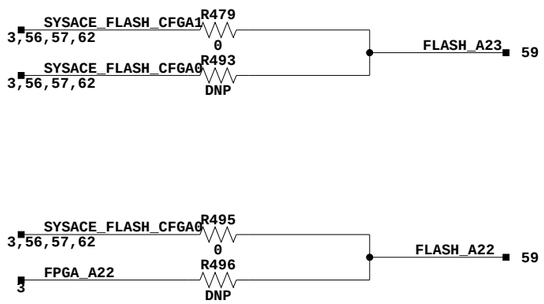


BPI Flash Addressing Scheme

	FPGA (U37) BPI Addr Pin	Schematic Net Name	Net Connection After Jumpering		Parellel Flash (U43) Addr Pin
4 x 64 Mbit Revisions	RS1 (U37.AK12)	SYSAC_FLASH_CFG1	FLASH_A23	R479-0ohm; R493-DNP	A24 (U43.26)
	RS0 (U37.AK13)	SYSAC_FLASH_CFG0	FLASH_A22	R495-0ohm; R496-DNP	A23 (U43.9)
	A22 (U37.AK14)	FPGA_A22	no connect		no connect
2 x 128 Mbit Revisions	RS1 (U37.AK12)	SYSAC_FLASH_CFG1	no connect	R479-DNP; R493-0ohm	no connect
	RS0 (U37.AK13)	SYSAC_FLASH_CFG0	FLASH_A23	R495-DNP; R496-0ohm	A24 (U43.26)
	A22 (U37.AK14)	FPGA_A22	FLASH_A22		A23 (U43.9)
Any Address Mode	A[21:0] (U37)	FLASH_A[21:0]	FLASH_A[21:0] N/A		A[22:1] (U43)

Note: See the ML510 User Guide for more details about BPI Flash





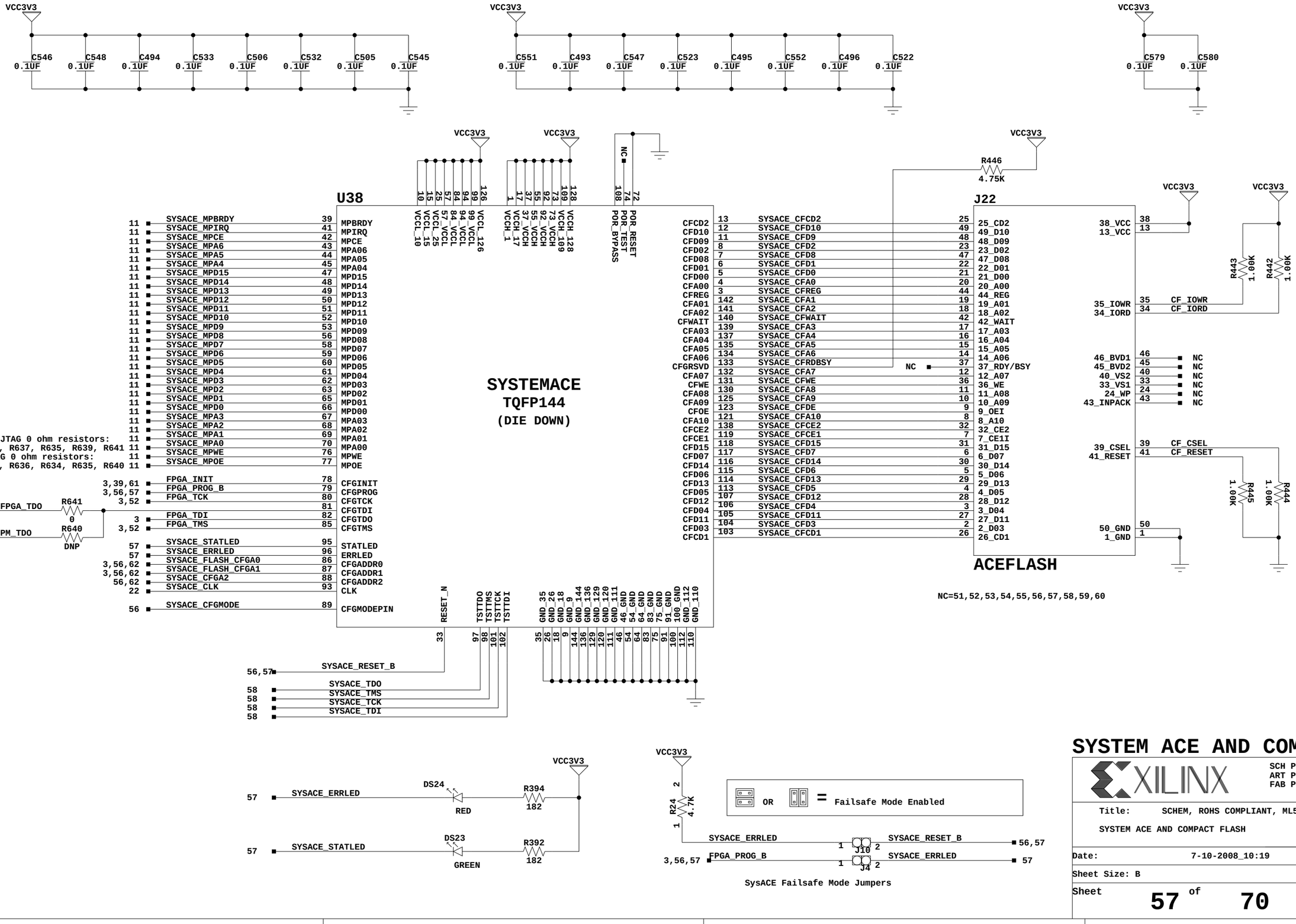
FPGA CONFIG, RESET, AND MISC I/O

XILINX

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
FPGA CONFIG, RESET, AND MISC I/O

Date: 7-10-2008_10:19	Ver: C
Sheet Size: B	Rev: 01
Sheet 56 of 70	Drawn By BF



SYSTEM ACE AND COMPACT FLASH

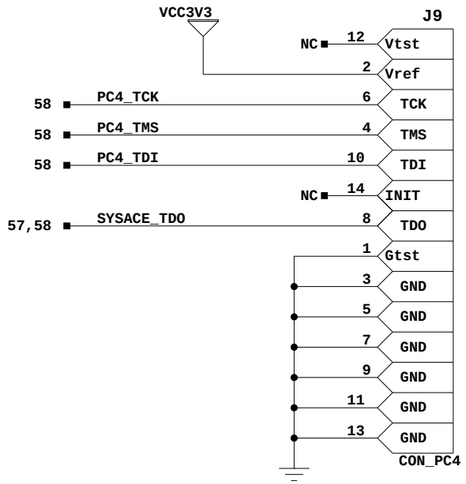
XILINX

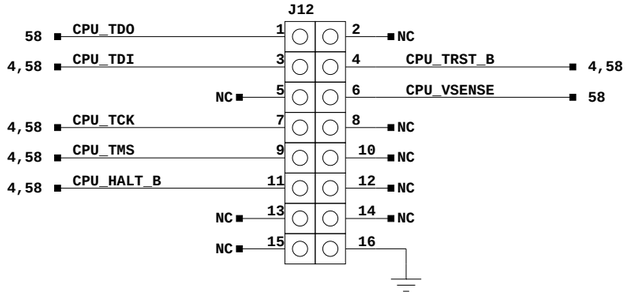
SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

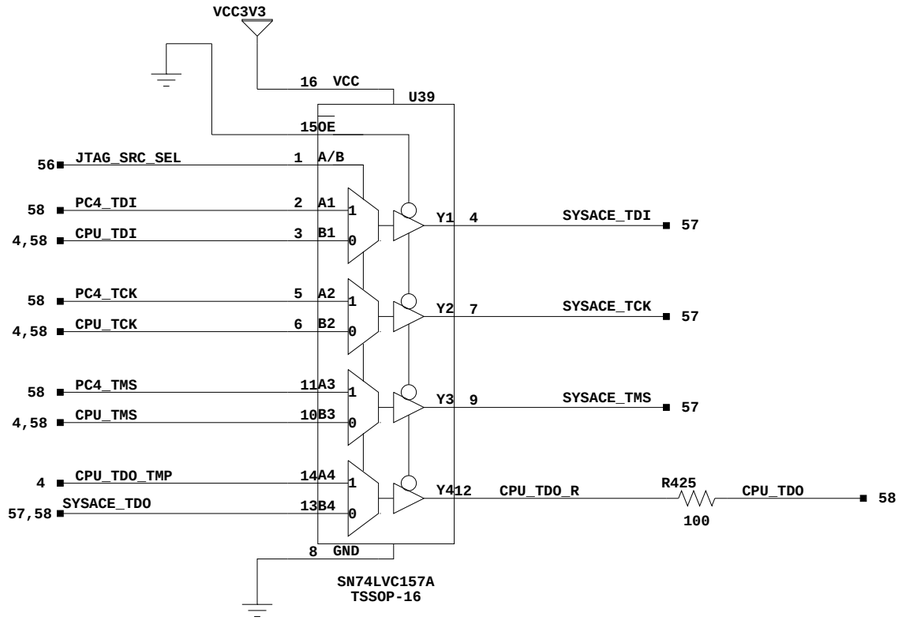
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

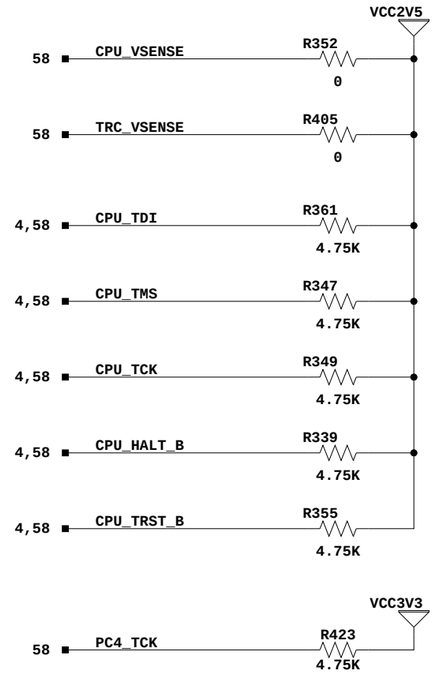
SYSTEM ACE AND COMPACT FLASH

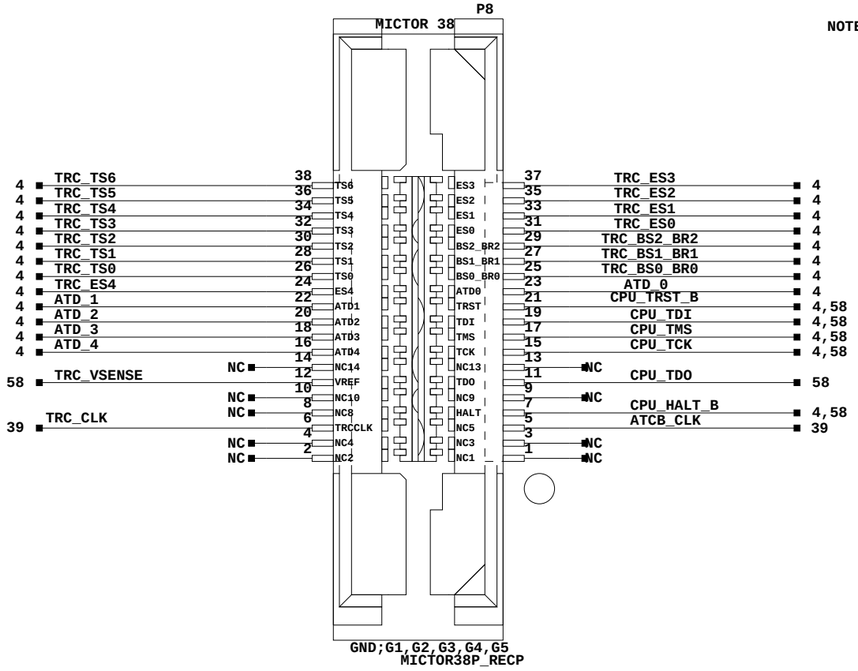
Date:	7-10-2008_10:19	Ver:	C
Sheet Size: B		Rev:	01
Sheet	57 of 70	Drawn By	BF



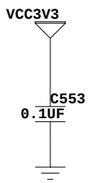








NOTE: THIS MUX INTRODUCES AN IMPLICIT 2.5V TO
3.3V LEVEL-SHIFT FOR THE CPU JTAG SIGNALS.
THE SERIES RESISTOR ON CPU_TDO IS INTENDED
TO PROVIDE PROTECTION FOR A 2.5V JTAG PROBE.



JTAG, DEBUG, TRACE CONNECTORS

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
JTAG, DEBUG, TRACE CONNECTORS

Date:	7-10-2008_10:19	Ver:	C
Sheet Size: B		Rev:	01
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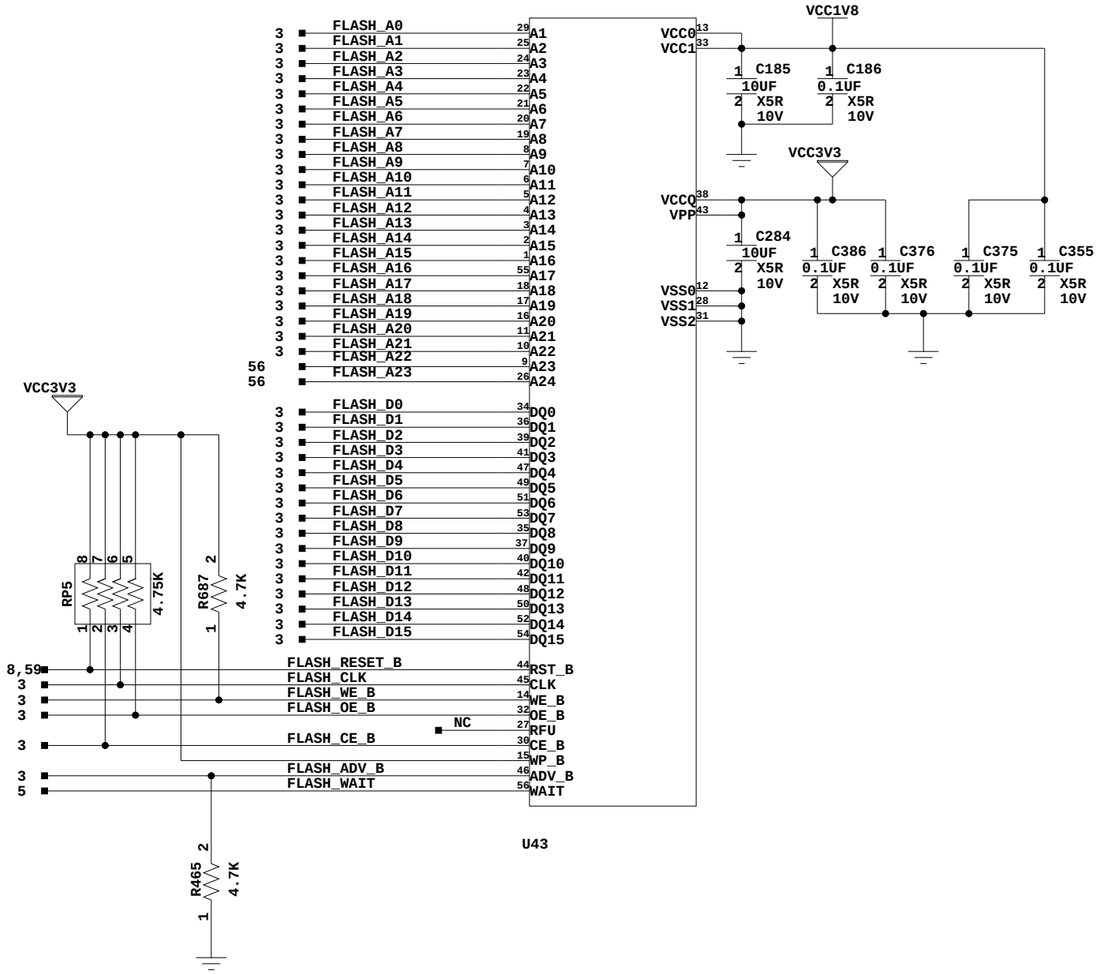
Silkscreen:
"Strata FLASH"
"256 MBit"



Programmable-Delay Supervisor Circuit

<Cap Value in nF> = (((<DELAY in S>)-(0.5*0.001)) *175)

SYNC. SRAM FLASH

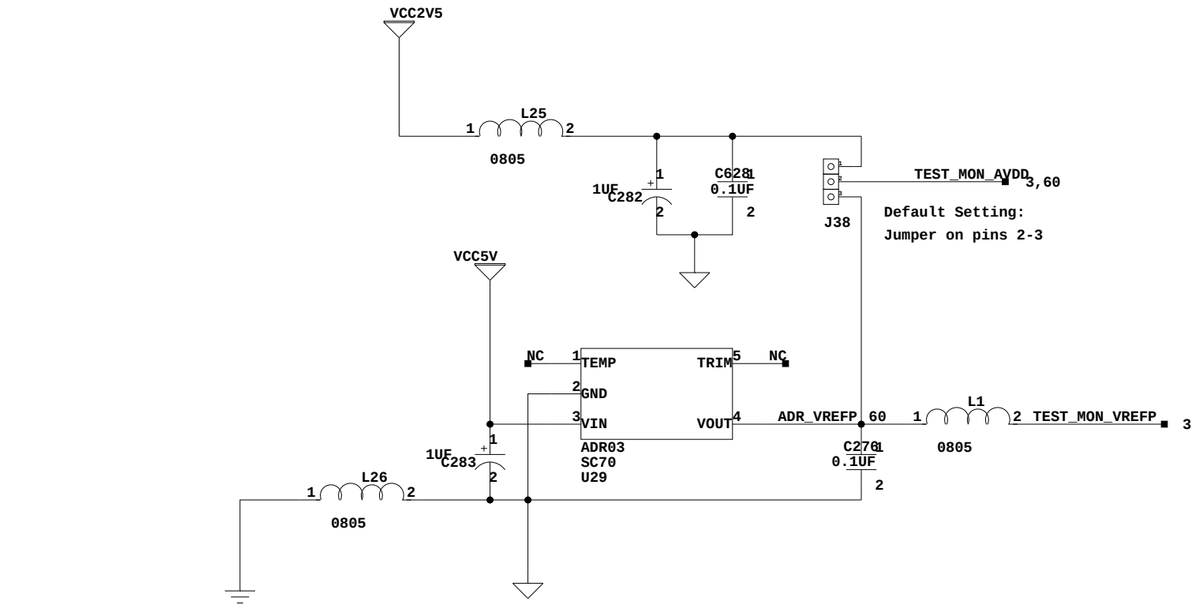
XILINX

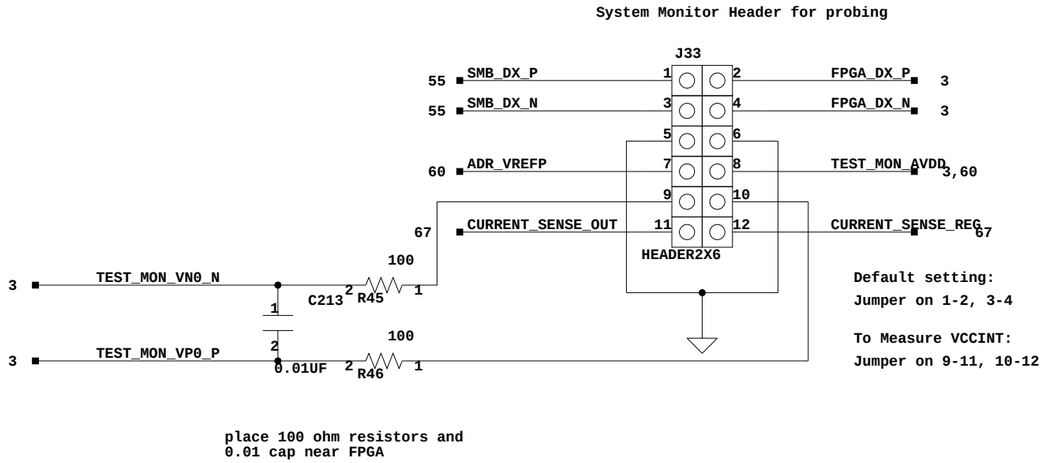
SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

SYNC. SRAM FLASH

Date:	8-1-2008_15:08	Ver:	C
Sheet Size: B		Rev:	01
Sheet	59 of 70	Drawn By	BF





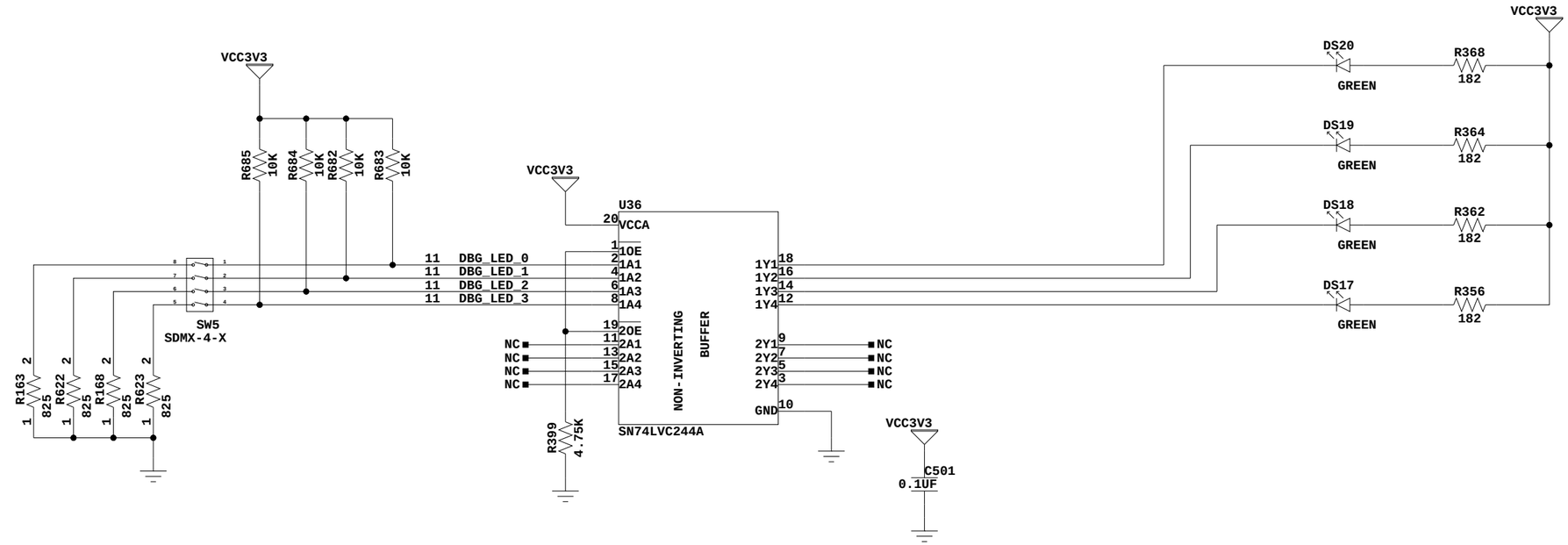
SYSMON HEADER / AVDD VREFP SUPPLY

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
SYS MONITOR HEADER / FPGA AVDD VREFP SUPPLY

Date: 8-1-2008_15:09	Ver: C
Sheet Size: B	Rev: 01
Sheet 60 of 70	Drawn By BF



DEBUG AND STATUS LEDS

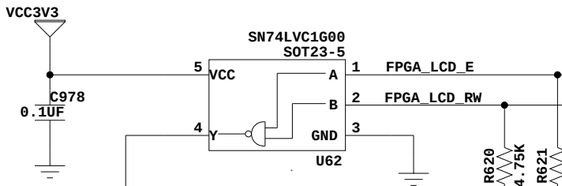
XILINX

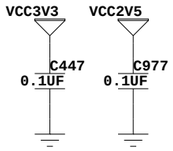
SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

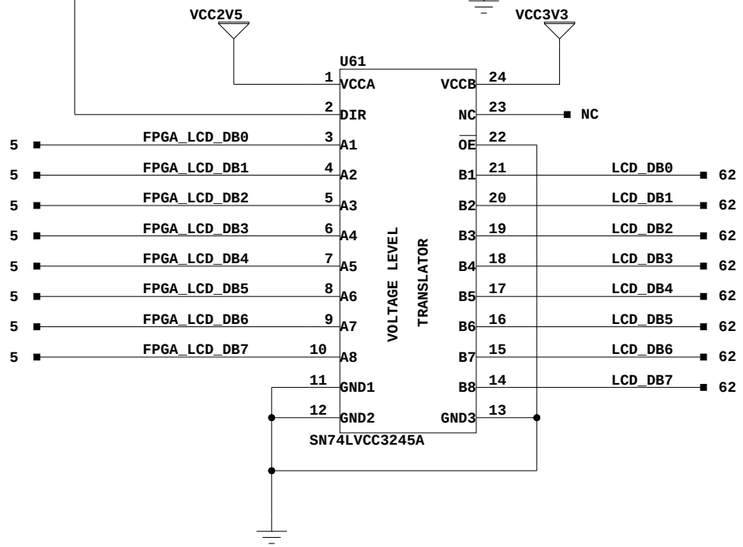
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

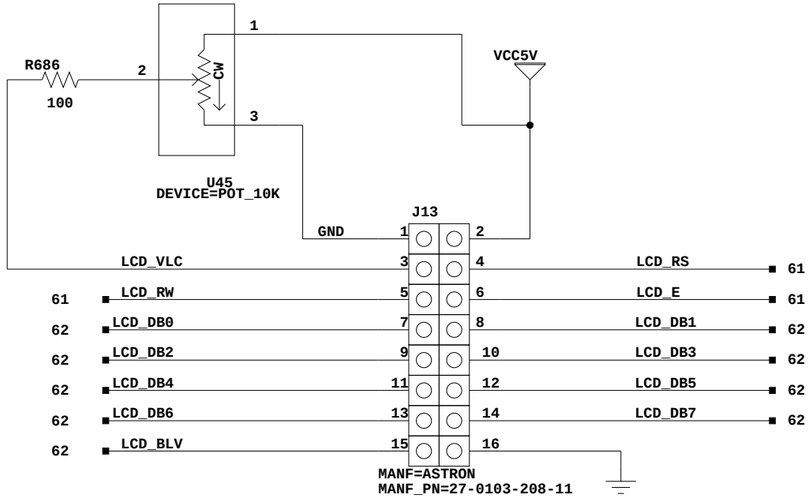
DEBUG AND STATUS LEDS

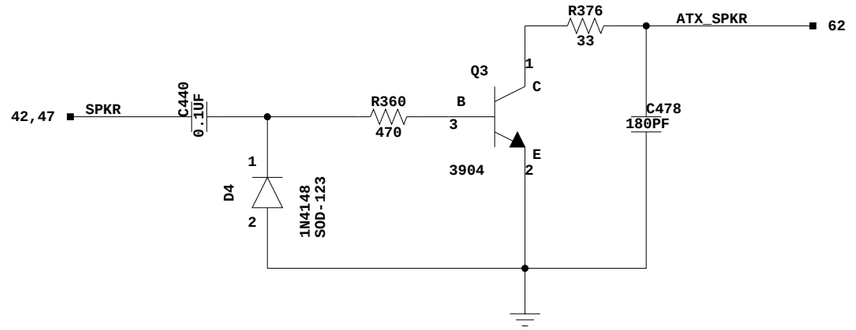
Date:	8-1-2008_15:08	Ver:	C
Sheet Size: B		Rev:	01
Sheet	61 of 70	Drawn By	BF

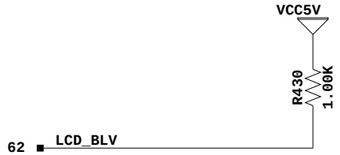


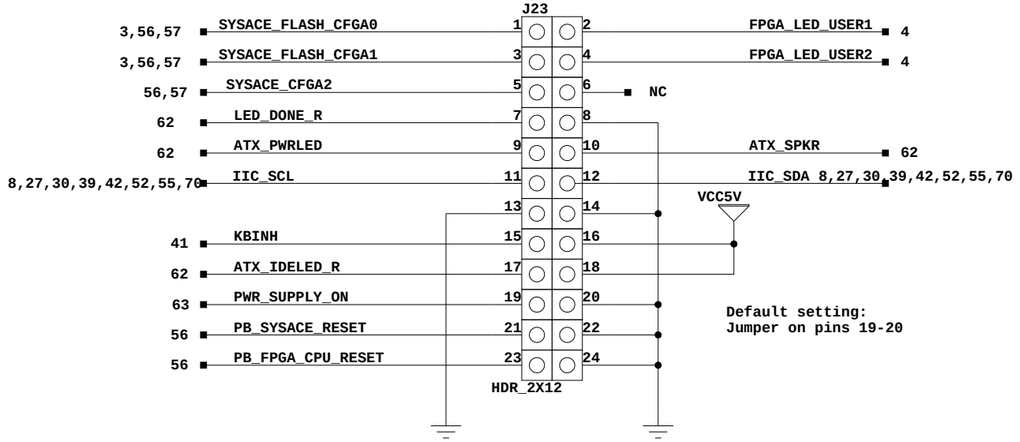


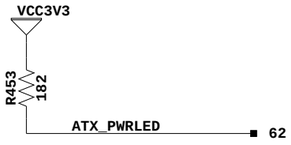


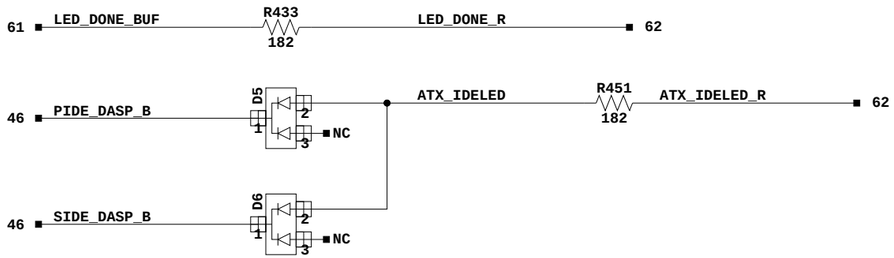


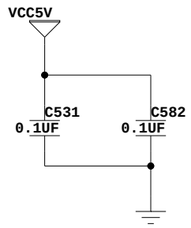












ATX AND FRONT PANEL CONNECTORS

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

ATX AND FRONT PANEL CONNECTORS

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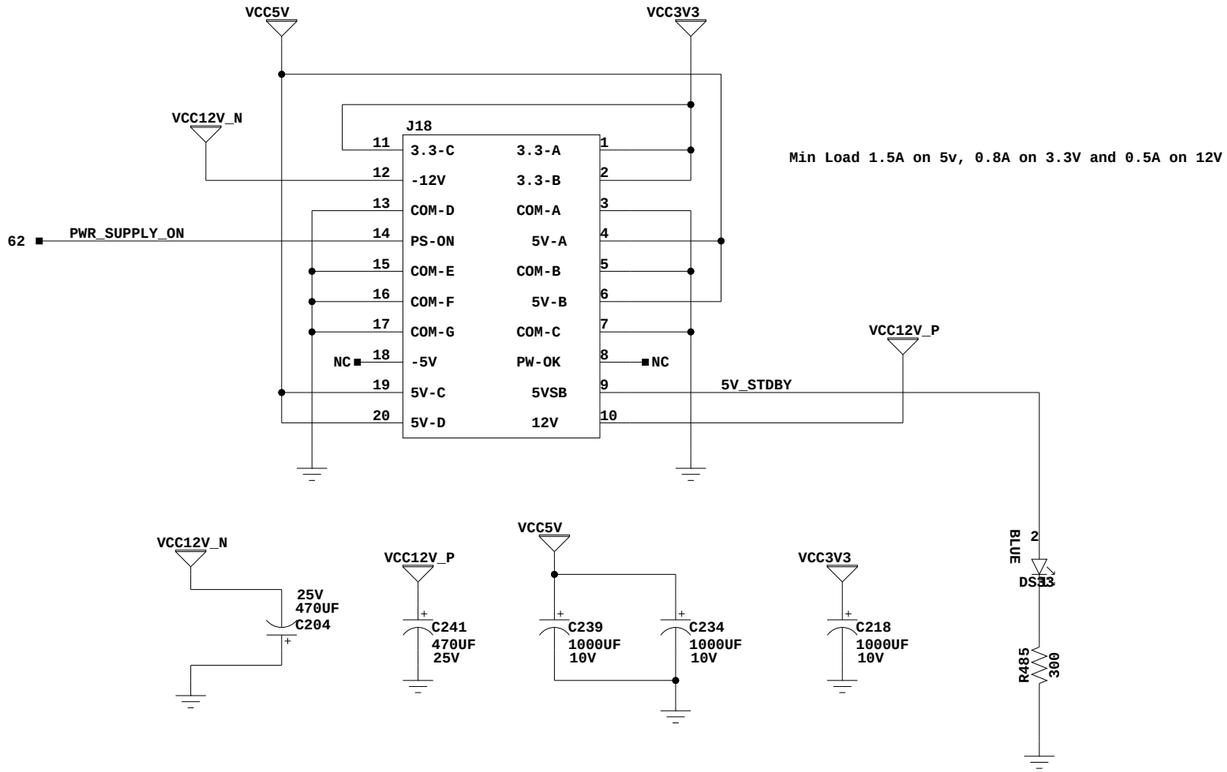
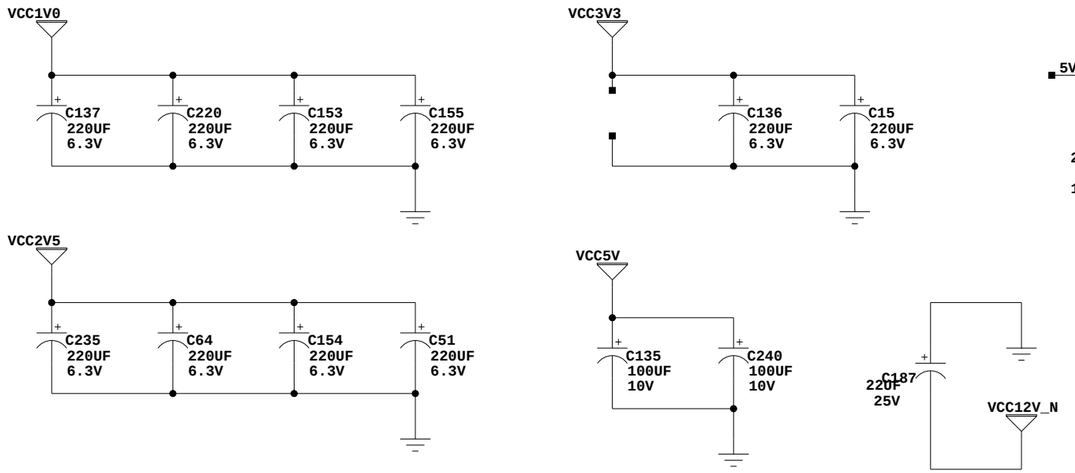
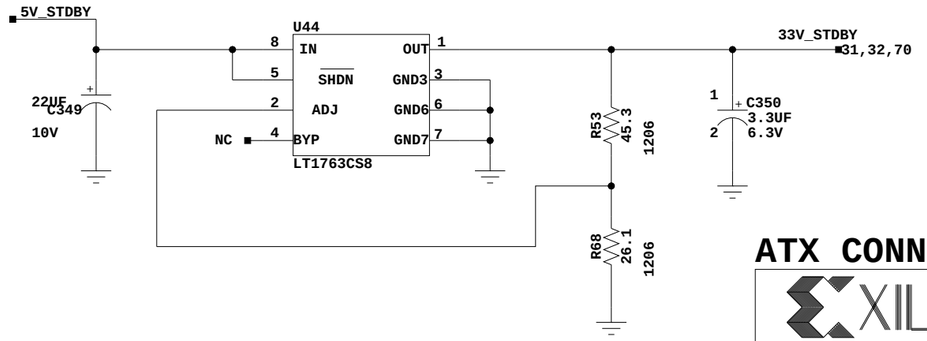


ATX Power Connector



BULK CAPS DISTRIBUTED AROUND BOARD.



ATX CONNECTOR, PWR TOGGLE

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
ATX CONNECTOR, PWR TOGGLE AND HEADER

Date:	8-1-2008_15:08	Ver:	C
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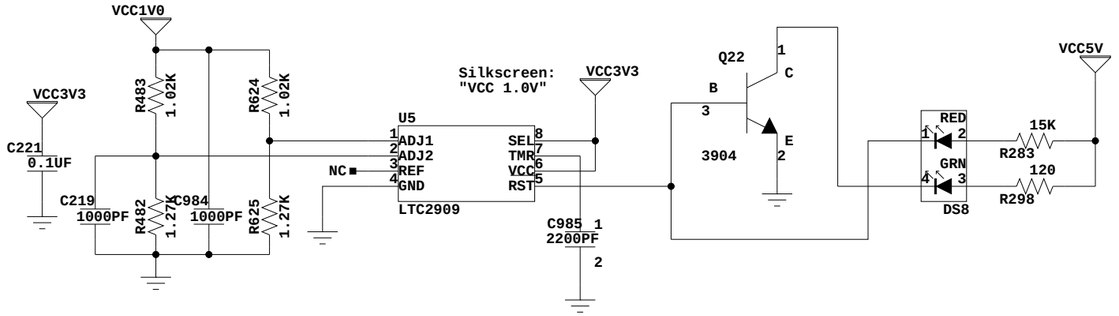

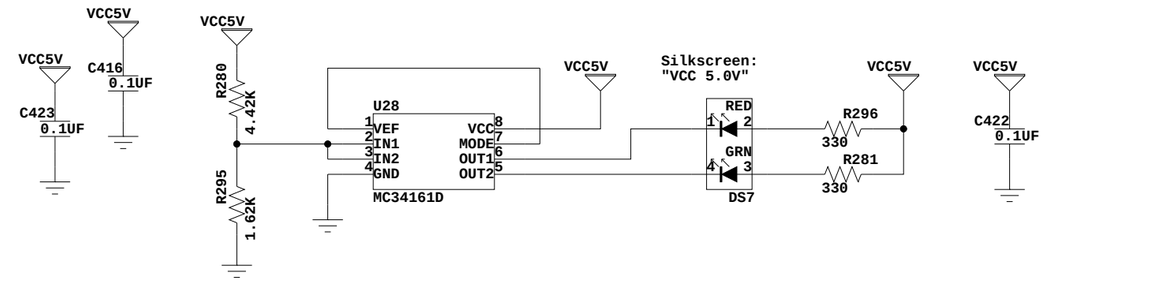

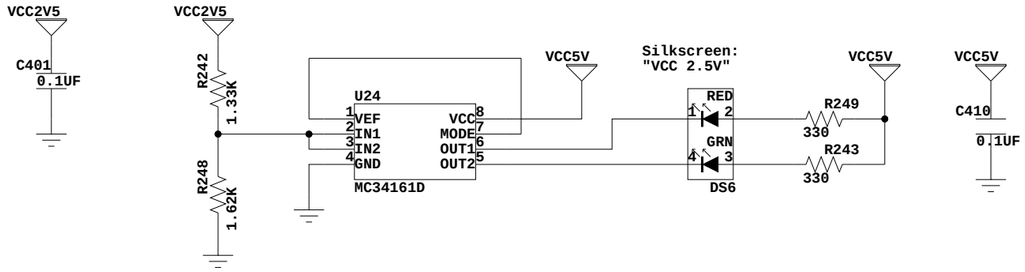

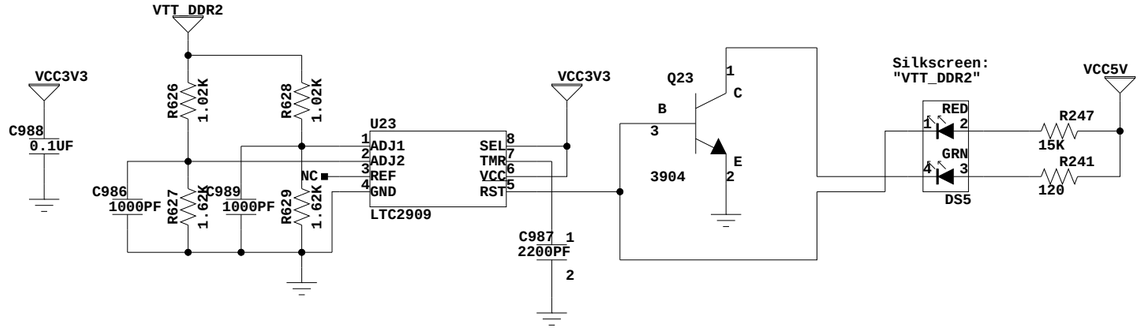

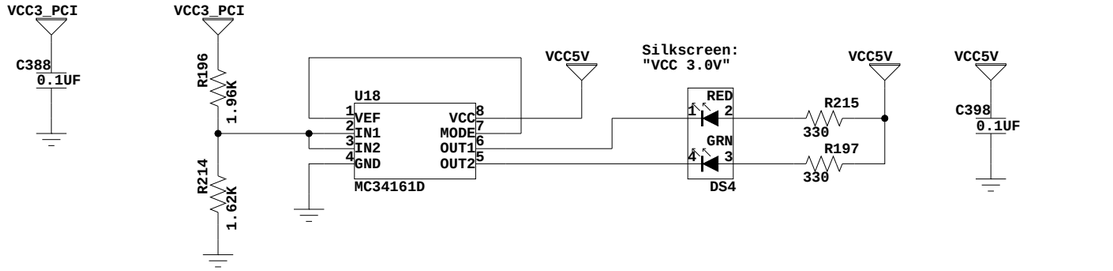

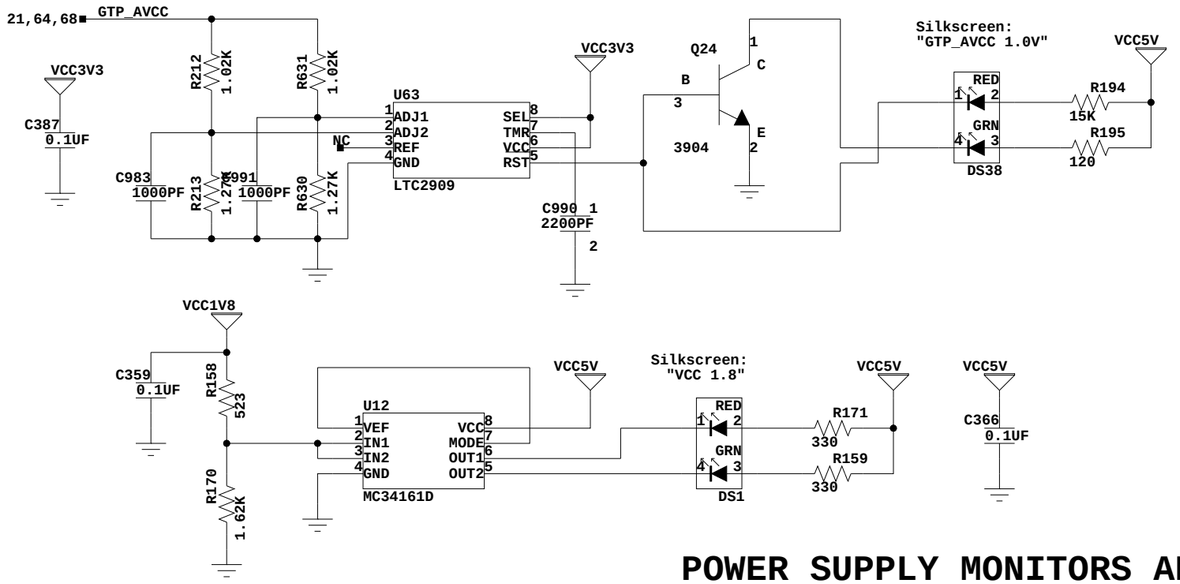

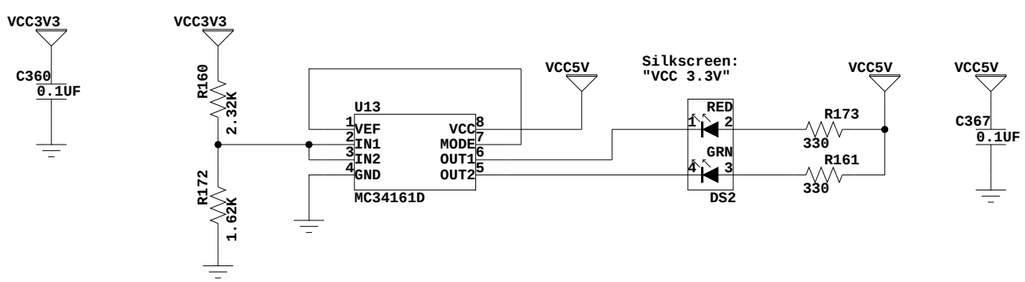

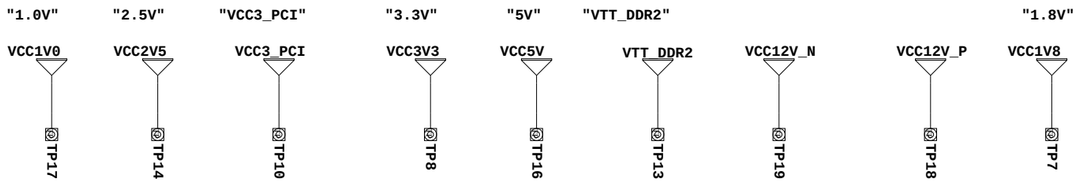

POWER SUPPLY MONITORS AND LEDS

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

POWER SUPPLY MONITORS AND LEDS

Date:	8-1-2008_15:08	Ver:	C
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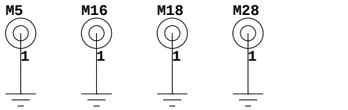
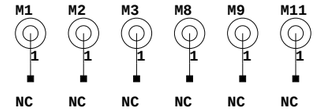
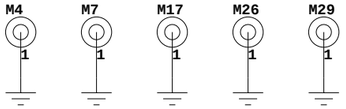
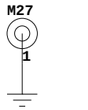
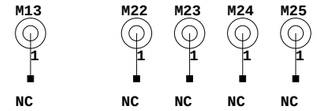
Mounting holes for ATX Form Factor



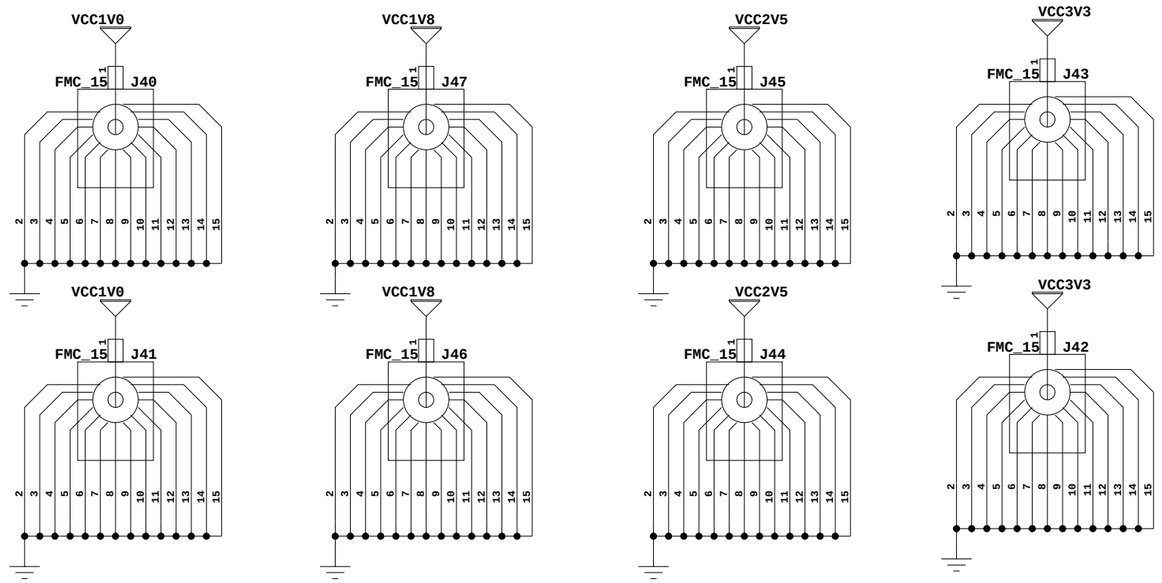




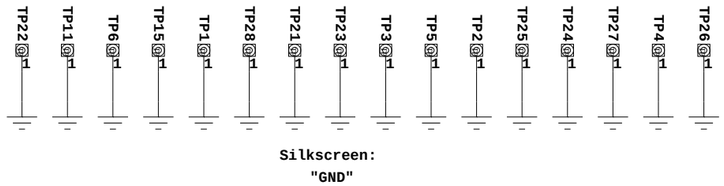




FMC connectors for power supply testing



Spread out on the board.



Silkscreen:
"GND"

ATX MOUNTING HOLES / TEST POINTS

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
ATX MOUNTING HOLES AND TEST POINTS

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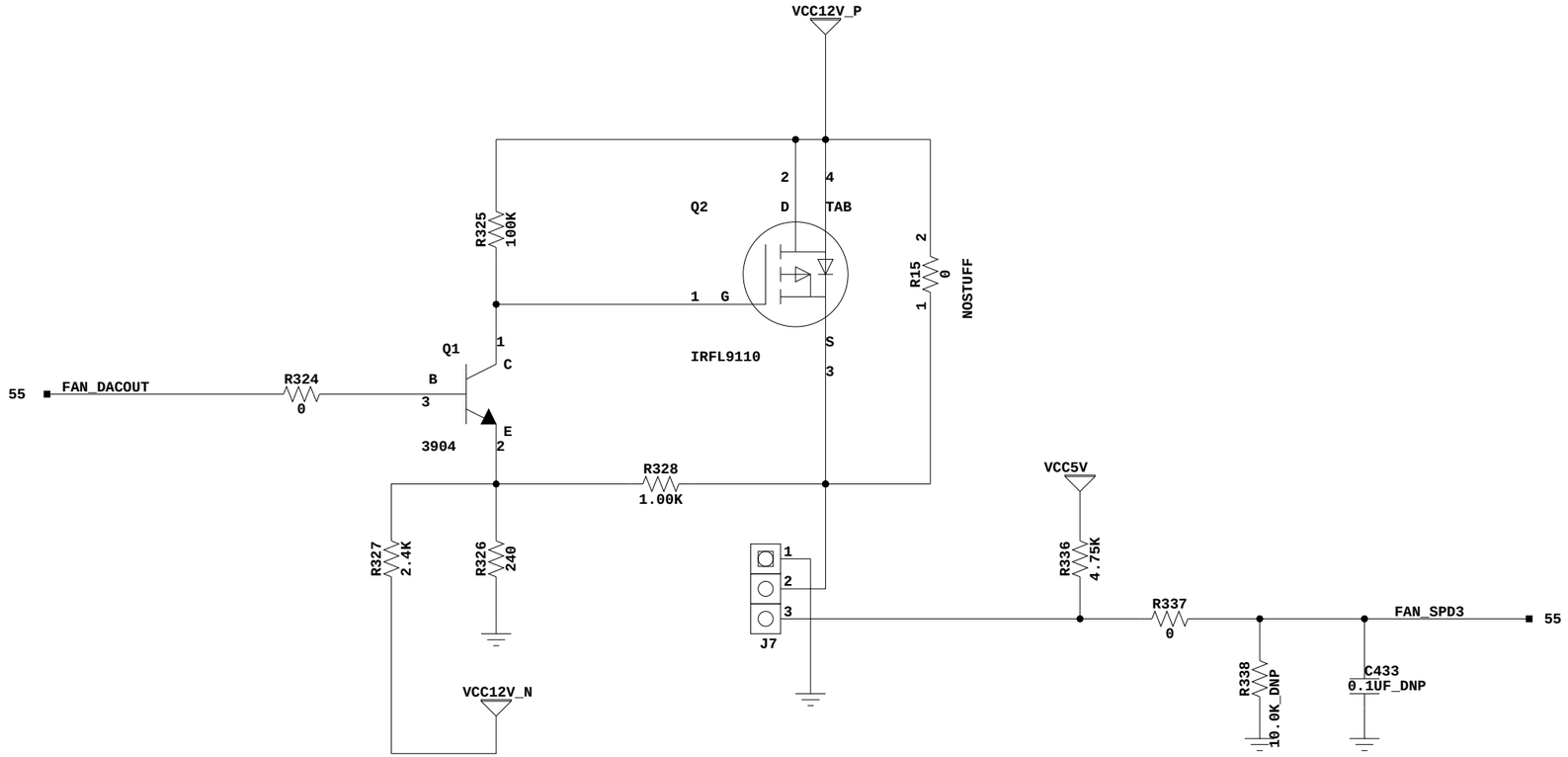

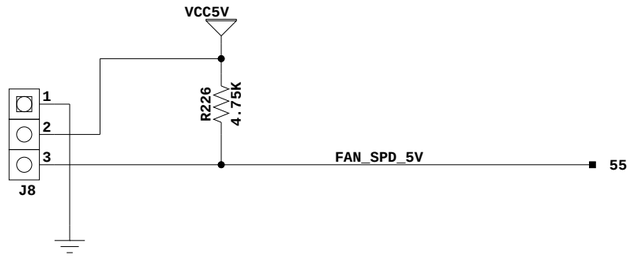

FPGA FAN SWITCH AND TACH

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA FAN SWITCH AND TACH

Date:	8-1-2008_15:08	Ver:	C
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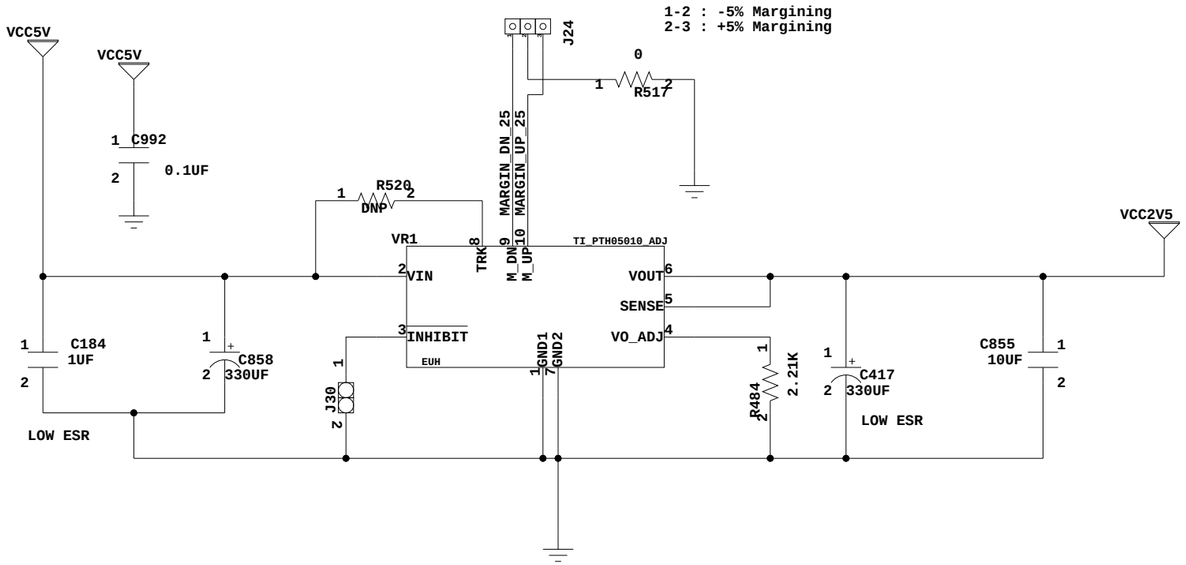
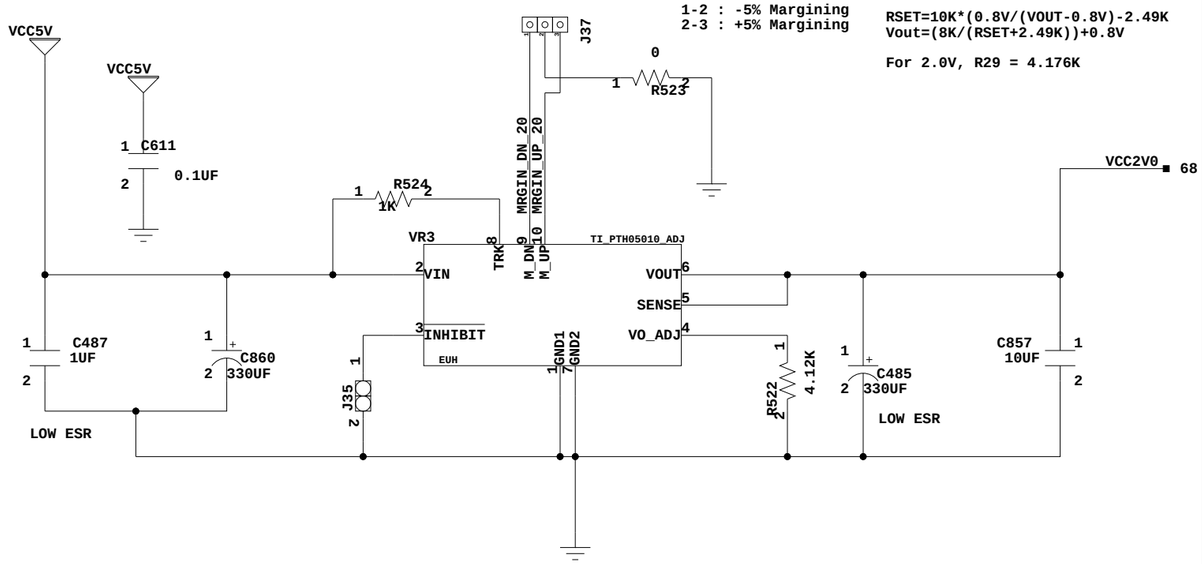
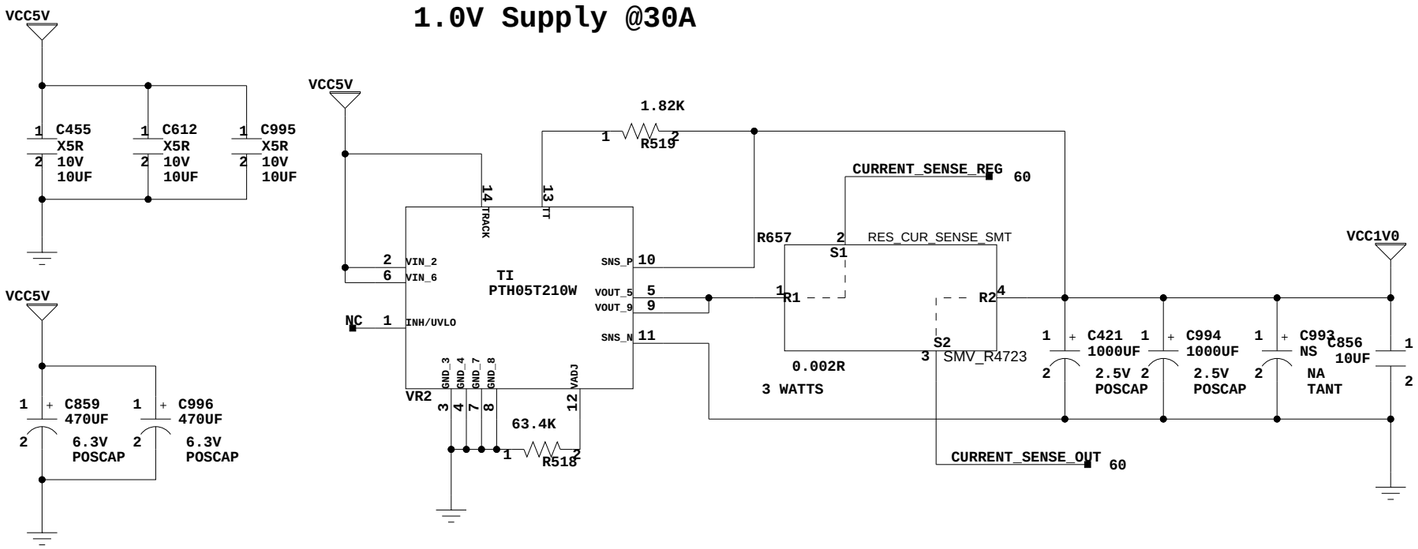
2.5V Supply @15A



2.0V Supply @15A



1.0V Supply @30A



FPGA CORE AND IO VOLTAGE

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

FPGA CORE AND IO VOLTAGE

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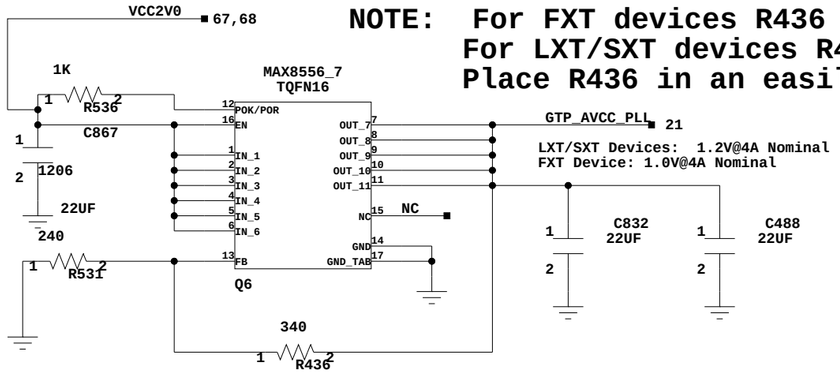
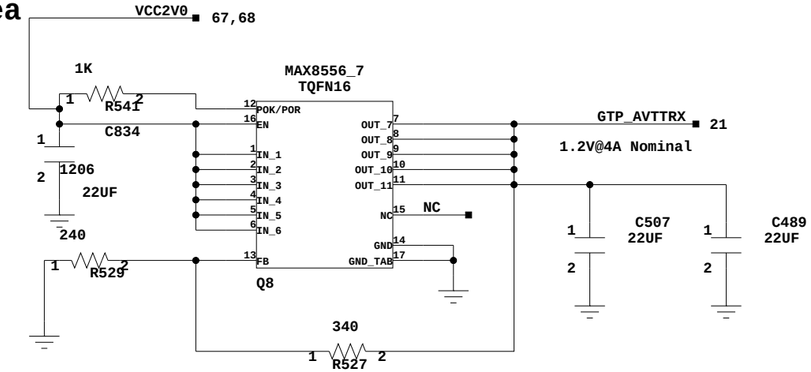
NOTE: For FXT devices R436 must be 240 ohms
For LXT/SXT devices R436 should be 340 ohms
Place R436 in an easily accessible area





R2 = R1*{(Vout/0.5)-1}

GTP POWER SUPPLIES

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
GTP POWER SUPPLIES

Date:	8-1-2008_15:08	Ver:	C
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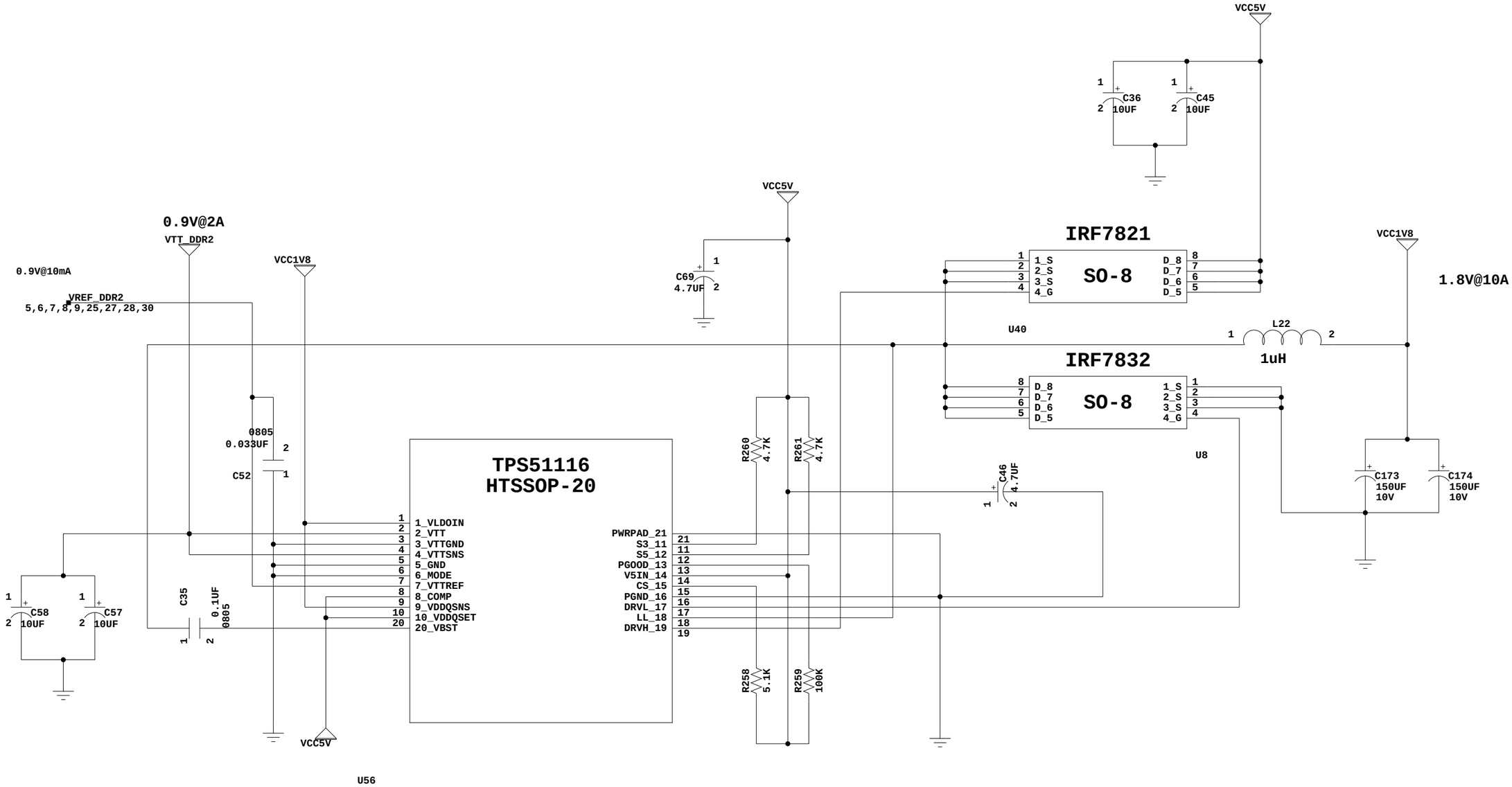

DDR2 POWER SUPPLY

XILINX

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM

DDR2 POWER SUPPLY

Date:	8-1-2008_15:08	Ver:	C
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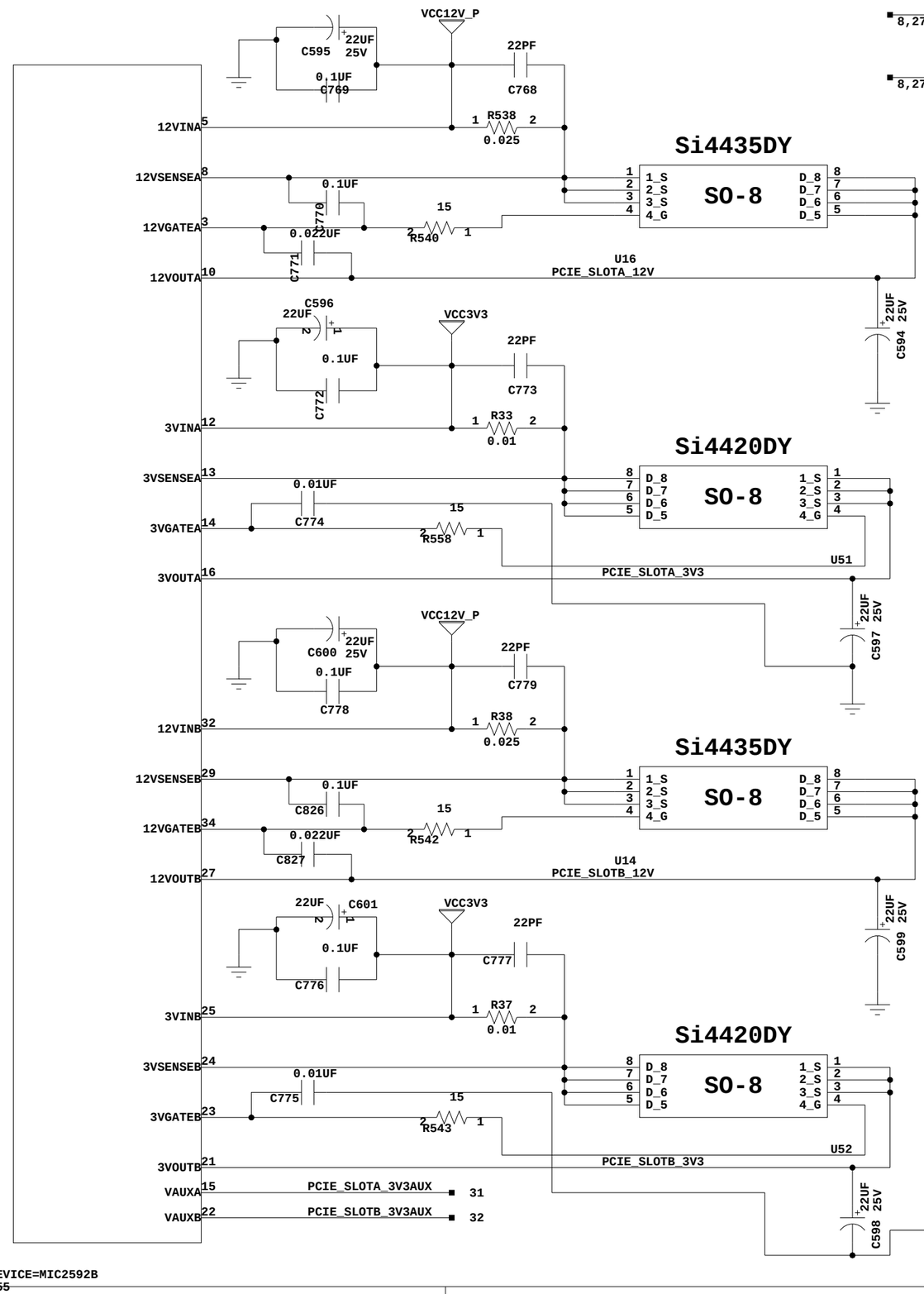
VCC12V_P
C595 22UF 25V
0.1UF C769
22PF C768
12VINA 5
R538 1 2 0.025
Si4435DY
SO-8
12VSENSEA 8
0.1UF C770
12VGATEA 3
15 R540
0.022UF C771
12VOUTA 10
U16
PCIE_SLOTA_12V
22UF 25V C594
C596 22UF
VCC3V3
0.1UF C772
22PF C773
3VINA 12
R33 1 2 0.01
Si4420DY
SO-8
3VSENSEA 13
0.01UF C774
3VGATEA 14
15 R558
3VOUTA 16
U51
PCIE_SLOTA_3V3
22UF 25V C597
VCC12V_P
C600 22UF 25V
0.1UF C778
22PF C779
12VINB 32
R38 1 2 0.025
Si4435DY
SO-8
12VSENSEB 29
0.1UF C826
12VGATEB 34
15 R542
0.022UF C827
12VOUTB 27
U14
PCIE_SLOTB_12V
22UF 25V C599
C601 22UF
VCC3V3
0.1UF C776
22PF C777
3VINB 25
R37 1 2 0.01
Si4420DY
SO-8
3VSENSEB 24
0.01UF C775
3VGATEB 23
15 R543
3VOUTB 21
U52
PCIE_SLOTB_3V3
22UF 25V C598
VAUXA 15
PCIE_SLOTA_3V3AUX 31
VAUXB 22
PCIE_SLOTB_3V3AUX 32
DEVICE=MIC2592B
U55
IIC_SCL
8,27,30,39,42,52,55,62
R428 0
IIC_SCL_PCIE 70
IIC_SDA
8,27,30,39,42,52,55,62
R431 0
IIC_SDA_PCIE 70
I2C ADDR = 0x8E
Make sure IIC Address is set correctly
33V_STDBY
31,32,63,70
47UF C602 100UF
C603
0.1UF C828
0.01UF C829
VSTBYA 11
VSTDBYB 26
IREF 33
0 R544
CFILTERA 2
0.047UF C830
CFILTERB 35
0.047UF C831
ONA 44
ONB 43
AUXENA 45
AUXENB 42
FAULT_A 1
FAULT_B 36
PWRGDA 6
PWRGDB 31
FORCE_A 9
FORCE_B 28
GPIA_0 4
100K R565
NC 7
NC
GPIB_0 38
100K R566
NC_1 30
NC
R554 R546 R547 R548 R549 R550 R551 R552 R553 R555 100K
R690 R691 DNP
A0 41
A1 40
A2 39
100K R564
100K R561
100K R557
33V_STDBY
31,32,63,70
INT 37
SCL 47
SDA 48
IIC_SCL_PCIE 70
IIC_SDA_PCIE 70
100K R556
RFILTER
GND 2
NC 19
NC 20
GND 42
NC 38
GND 17
DEVICE=MIC2592B
U55
100K-DNP R567
PCI-E PWR MGMT CONTROLLER
XILINX
SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTORM
PCI-E PWR MGMT CONTROLLER
Date: 8-1-2008_15:08
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Sheet Size: B
Rev: 01
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