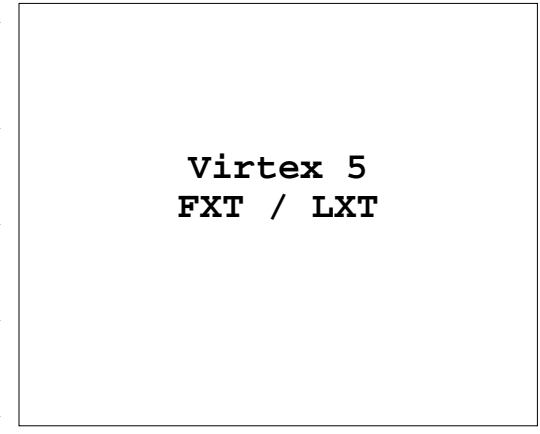


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USER Clock
SMA Clock IN/OUT
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Mictor and
CPU Debug Header
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IIC
Fan Controller
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SystemACE
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MII/RGMII/SGMII
10/100/1000 PHY
RJ45 Magnetics
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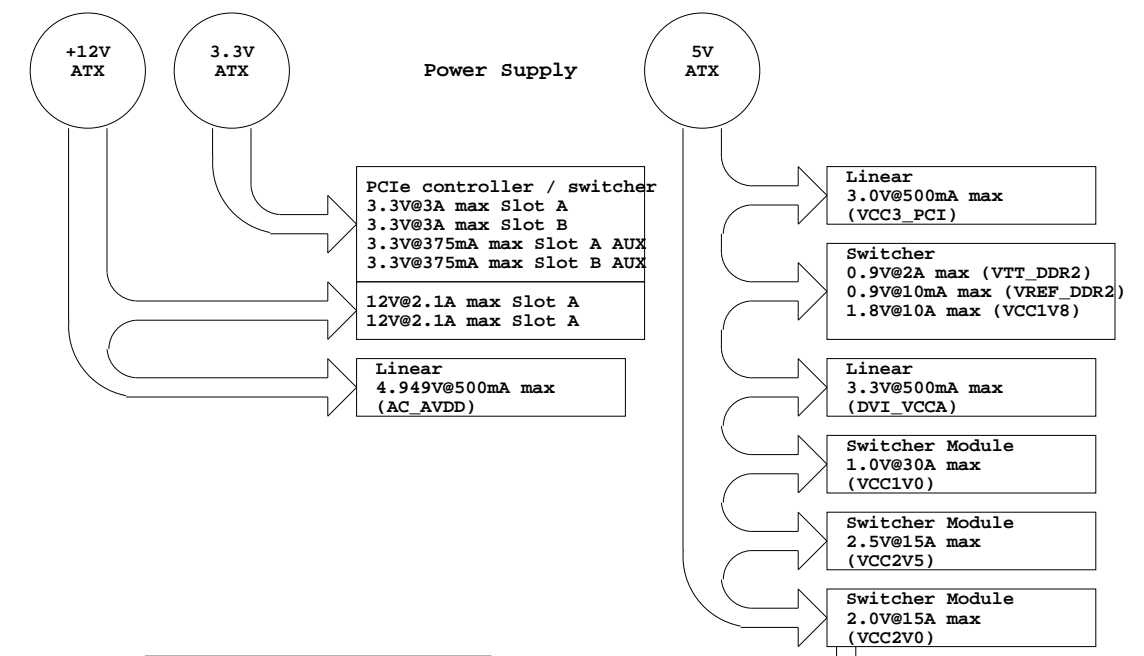
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RJ45 Magnetics
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J25, J26

2 line
Character LCD
Header
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J13



IIC Device Addresses

DEVICE	REFDES	ADDR
LM87C1MT	u20	0x5C
RTC-8564JE	u22	0xA2
24LC64-I/SN	u21	0xA0
87705-1001	p9	0xA6
87705-1001	p48	0xA8
MIC2592B-2BTQ	U55	0x8E

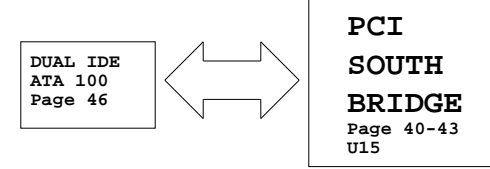
XILINX PART NUMBERS	
SCHEMATICS	0381255
PCB ARTWORK	0532059
PCB FABRICATION	1280432

NOTE: PLEASE REVIEW THE ML510 BOM FOR ITEMS DESIGNATED AS "DNP".

DNP ITEMS ARE NOT POPULATED ON THE PCB.

THE ML510 BOM CONTAINS THE MOST ACCURATE INFORMATION ABOUT

DNP DISCRETES AND COMPONENTS



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DUAL 3.3V PCI
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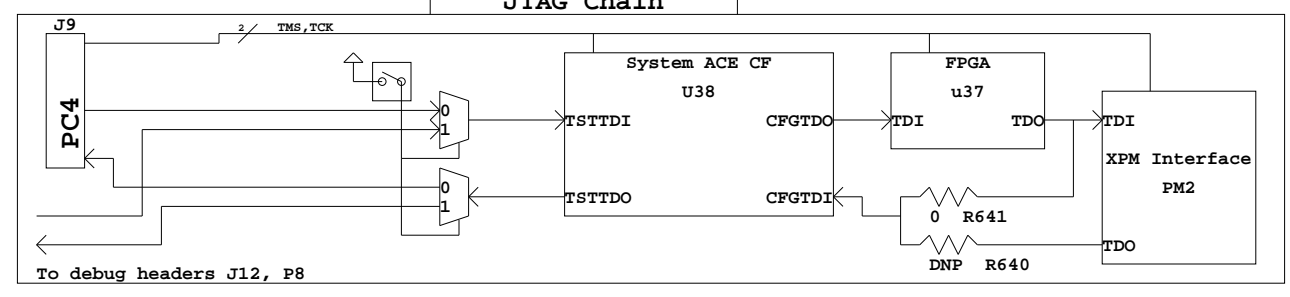
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JTAG Chain



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29	DIMM1 DDR2 SSTL-2 TERMINATION
30	DIMM1 DDR2 DECOUPLING
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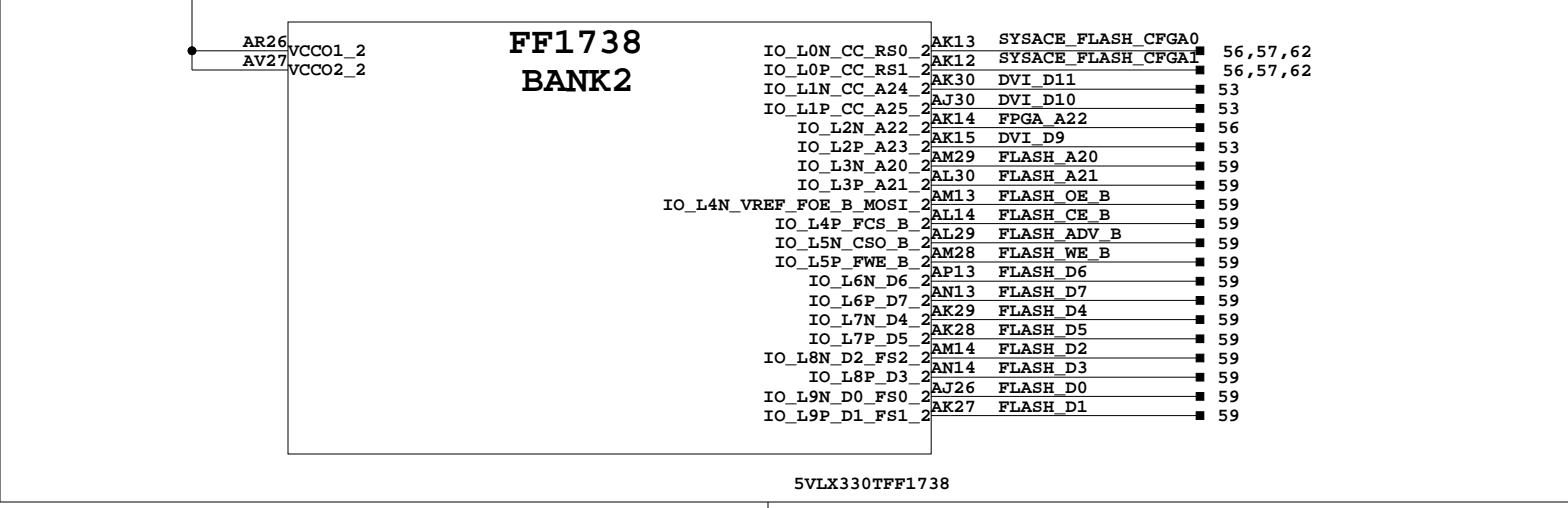
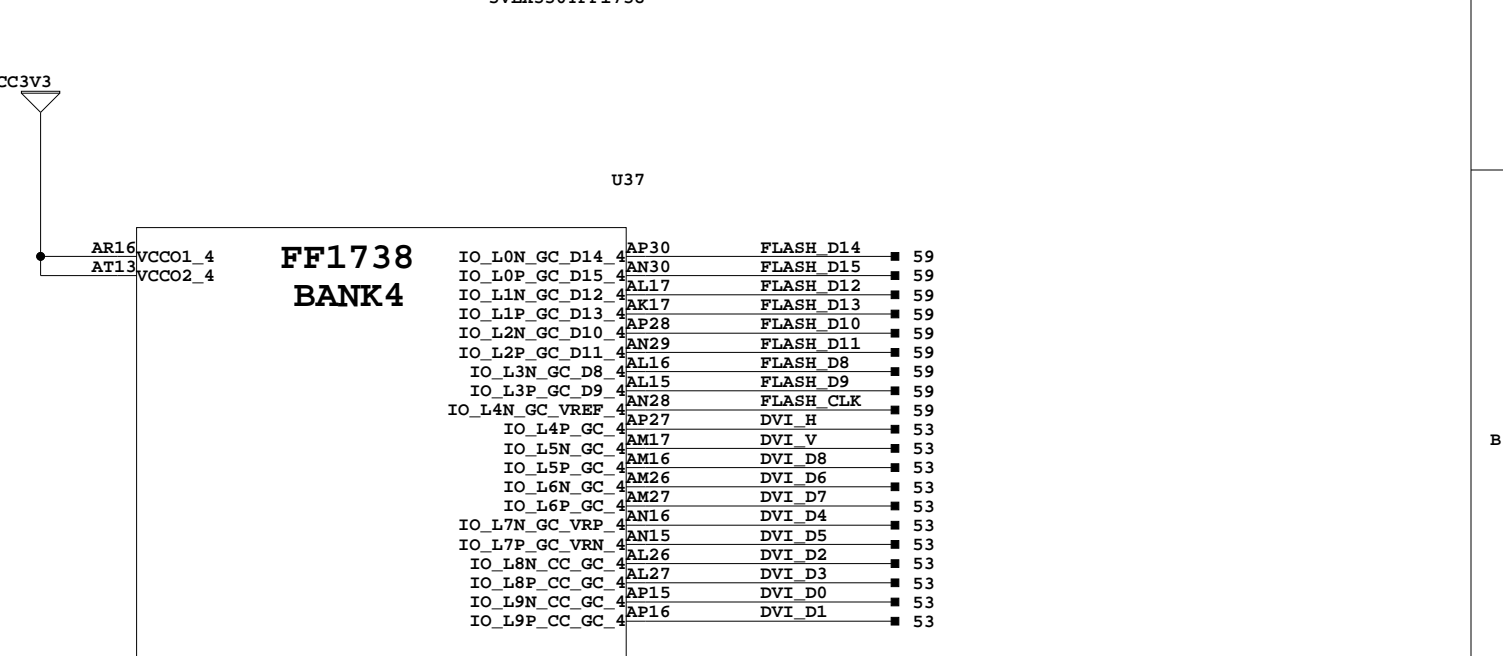
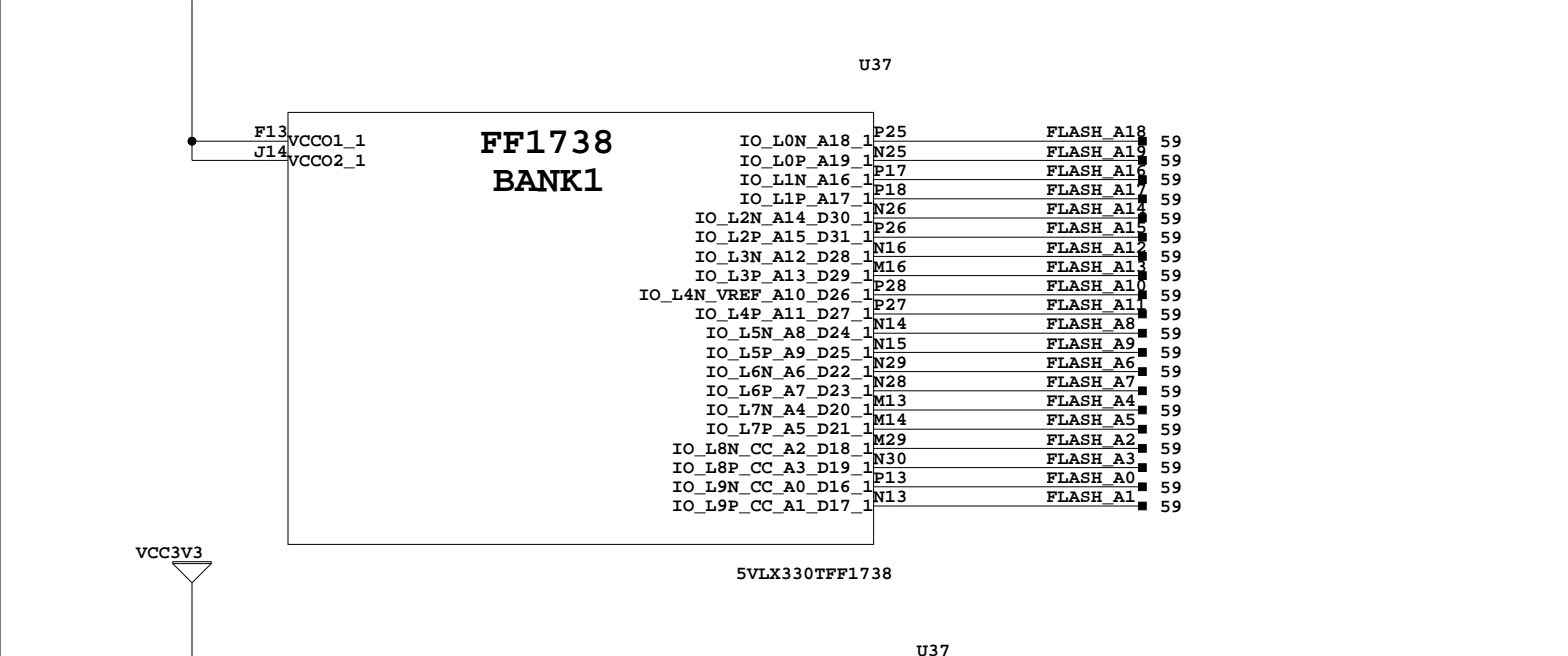
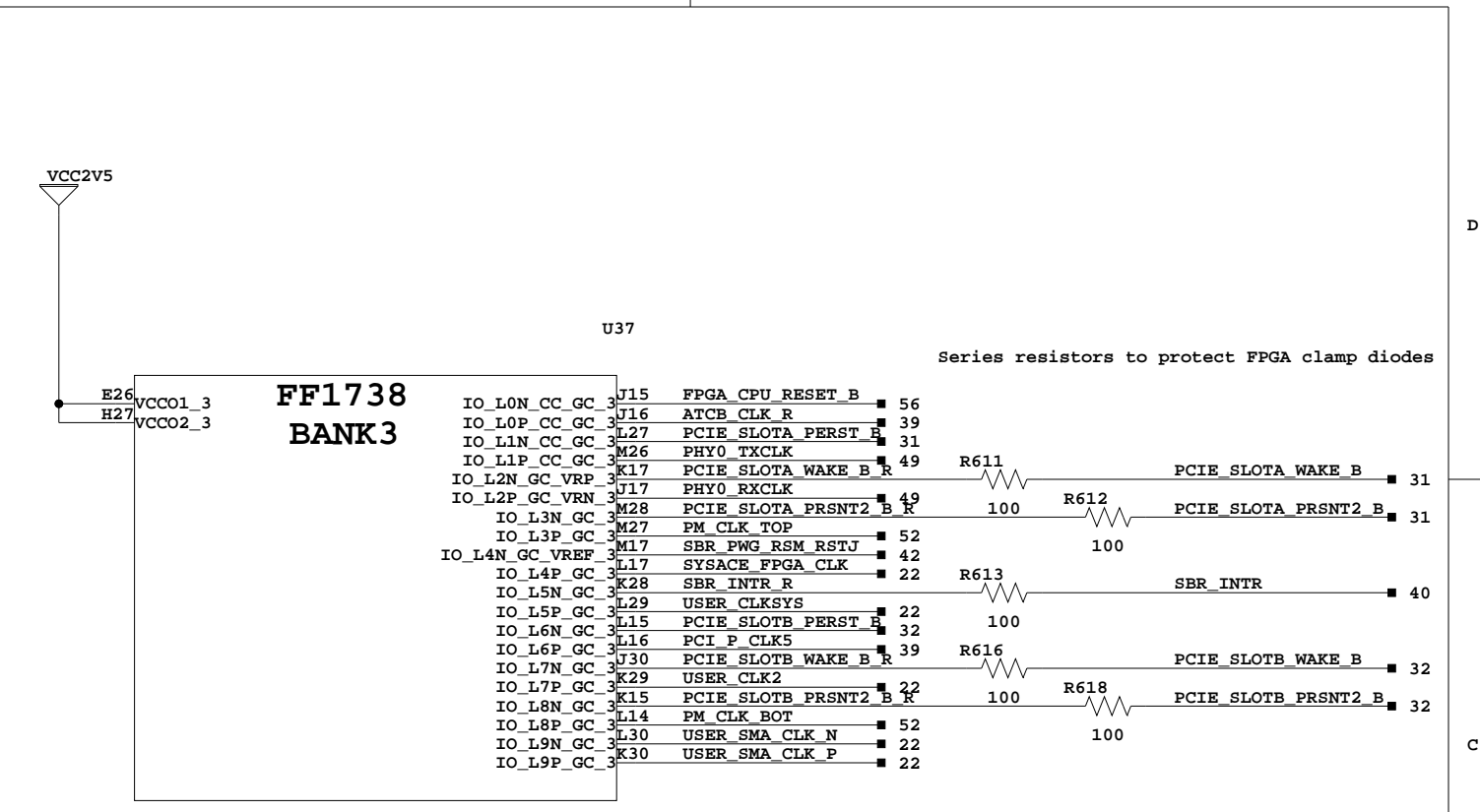
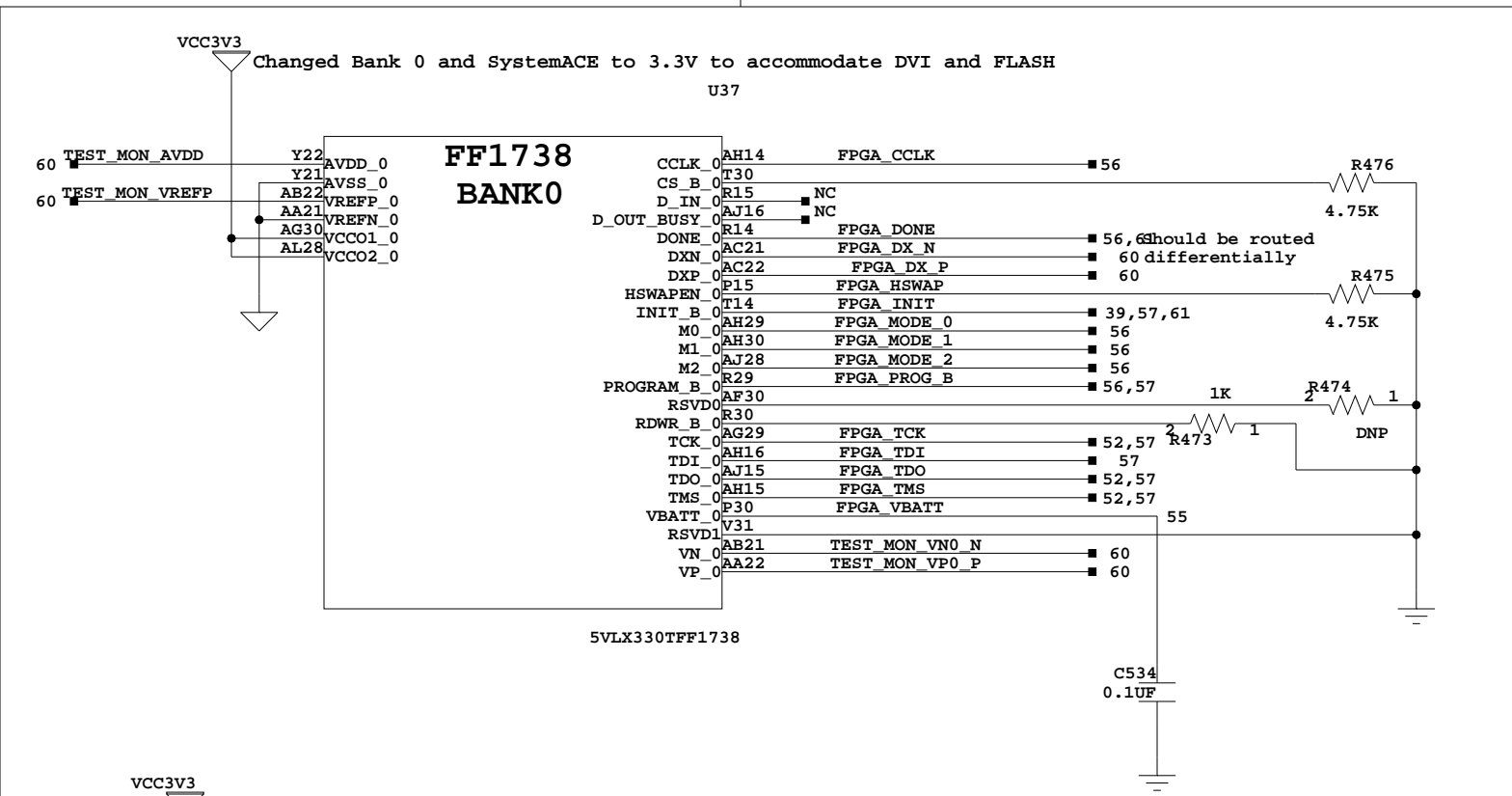
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ART P/N 0532059
FAB P/N 1280432

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FPGA - BANK 0, 1, 2, 3, 4

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FPGA - BANK 0, 1, 2, 3, 4 - CONFIG, MISC, FLASH, CLOCKS, DVI		
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VCC2V5

U37

B25 VCCO1_5
C22 VCCO2_5
F23 VCCO3_5

FF1738
BANK5

IO_L0N_5	M24	PM_IO_1_N	52
IO_L0P_5	L24	PM_IO_0_P	52
IO_L10N_CC_5	K19	PM_IO_21_N	52
IO_L10P_CC_5	K18	PM_IO_20_P	52
IO_L11N_CC_5	L26	PM_IO_23_N	52
IO_L11P_CC_5	K27	PM_IO_22_P	52
IO_L12N_VRN_5	P20	VRP_BANK5	52
IO_L12P_VRN_5	N20	VRN_BANK5	52
IO_L13N_5	F27	PM_IO_25_N	52
IO_L13P_5	G27	PM_IO_24_P	52
IO_L14N_VREF_5	N19	PM_IO_27_N	52
IO_L14P_5	M19	PM_IO_26_P	52
IO_L15N_5	H28	PM_IO_29_N	52
IO_L15P_5	G28	PM_IO_28_P	52
IO_L16N_5	N18	PM_IO_31_N	52
IO_L16P_5	M18	PM_IO_30_P	52
IO_L17N_5	F29	PM_IO_33_N	52
IO_L17P_5	G29	PM_IO_32_P	52
IO_L18N_5	L19	PM_IO_35_N	52
IO_L18P_5	L20	PM_IO_34_P	52
IO_L19N_5	H30	PM_IO_37_N	52
IO_L19P_5	H29	PM_IO_36_P	52
IO_L1N_5	E17	PM_IO_3_N	52
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IO_L2N_5	L25	PM_IO_5_N	52
IO_L2P_5	K24	PM_IO_4_P	52
IO_L3N_5	F17	PM_IO_7_N	52
IO_L3P_5	F16	PM_IO_6_P	52
IO_L4N_VREF_5	J25	PM_IO_9_N	52
IO_L4P_5	K25	PM_IO_8_P	52
IO_L5N_5	H16	PM_IO_11_N	52
IO_L5P_5	G16	PM_IO_10_P	52
IO_L6N_5	J26	PM_IO_13_N	52
IO_L6P_5	H26	PM_IO_12_P	52
IO_L7N_5	G17	PM_IO_15_N	52
IO_L7P_5	G18	PM_IO_14_P	52
IO_L8N_CC_5	J27	PM_IO_17_N	52
IO_L8P_CC_5	J28	PM_IO_16_P	52
IO_L9N_CC_5	H18	PM_IO_19_N	52
IO_L9P_CC_5	J18	PM_IO_18_P	52

5VLX330TFF1738

49.9

49.9

VCC2V5

VCC2V5

U37

AT23 VCCO1_6
AW24 VCCO2_6
AY21 VCCO3_6

FF1738
BANK6

IO_L0N_6	AR28	CPU_TDO_TMP	58
IO_L0P_6	AR29	CPU_HALT_B	58
IO_L10N_CC_6	AM18	TRC_BS1_BR1	58
IO_L10P_CC_6	AN18	TRC_BS2_BR2	58
IO_L11N_CC_6	AP26	ATD_0	58
IO_L11P_CC_6	AN26	TRC_BS0_BR0	58
IO_L12N_VRN_6	AP18	VRP_BANK6	58
IO_L12P_VRN_6	AR18	VRN_BANK6	58
IO_L13N_6	AP25	ATD_2	58
IO_L13P_6	AN25	ATD_1	58
IO_L14N_VREF_6	AR19	SBR_IDE_RST_B	46
IO_L14P_6	AT19	ATD_3	58
IO_L15N_6	AN24	IIC_THERM_B	42,55
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IO_L19P_6	AR14	CPU_TMS	50
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IO_L2P_6	AR30	CPU_TDI	58
IO_L3N_6	AR15	TRC_ES4	58
IO_L3P_6	AT15	TRC_ES2	58
IO_L4N_VREF_6	AU29	SBR_NMI_R	58
IO_L4P_6	AT29	TRC_TS0	58
IO_L5N_6	AT16	TRC_TS2	58
IO_L5P_6	AT17	TRC_TS1	58
IO_L6N_6	AT27	TRC_TS4	58
IO_L6P_6	AU28	TRC_TS3	58
IO_L7N_6	AR17	TRC_TS6	58
IO_L7P_6	AP17	TRC_TS5	58
IO_L8N_CC_6	AR27	TRC_CLK_R	39
IO_L8P_CC_6	AT26	TRC_ES3	58
IO_L9N_CC_6	AN19	TRC_ES0	58
IO_L9P_CC_6	AN20	TRC_ES1	58

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49.9

49.9

VCC2V5

Series resistor to protect
FPGA clamp diode

R619
100

SBR_NMI 40

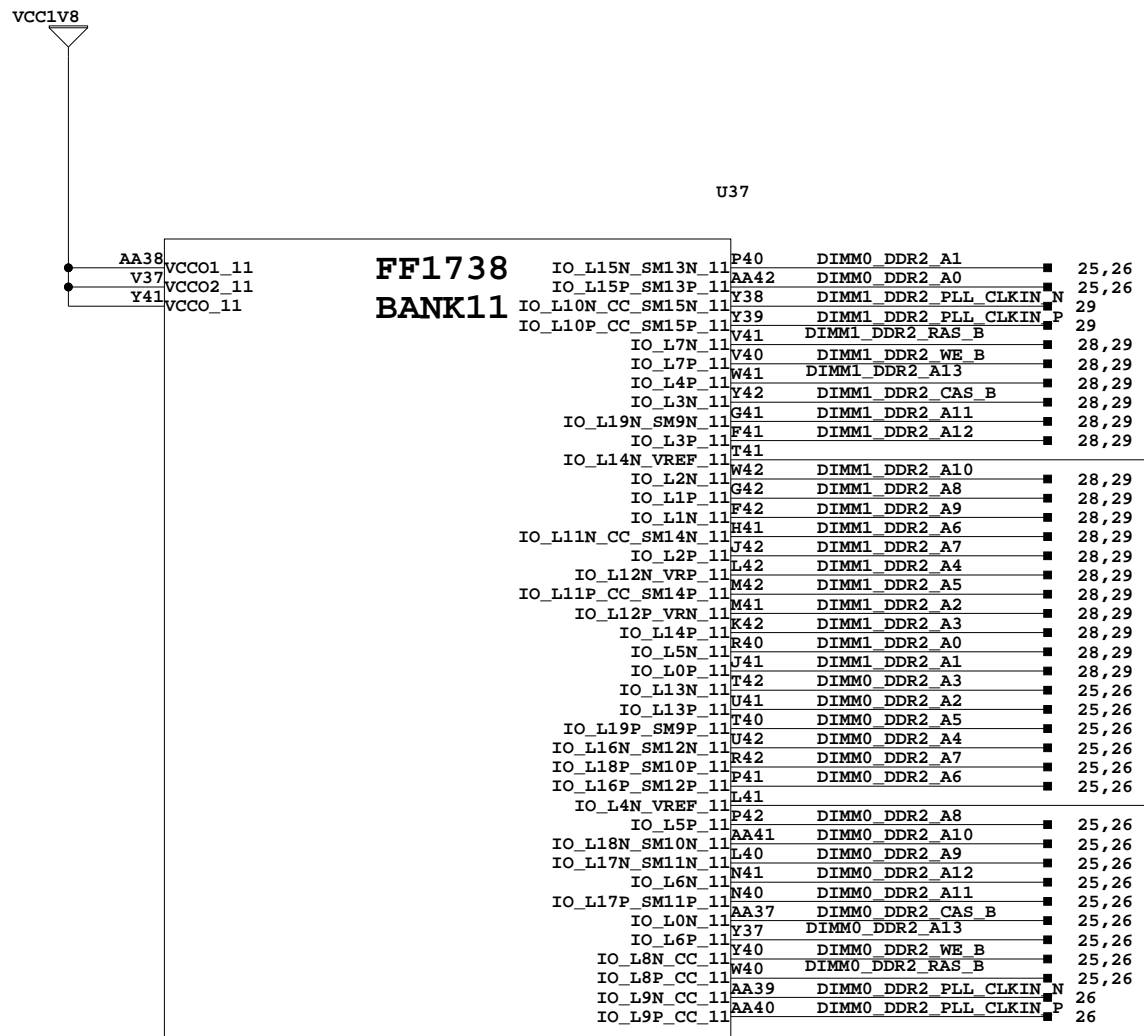
FPGA - BANK 5,6



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ART P/N 0532059
FAB P/N 1280432

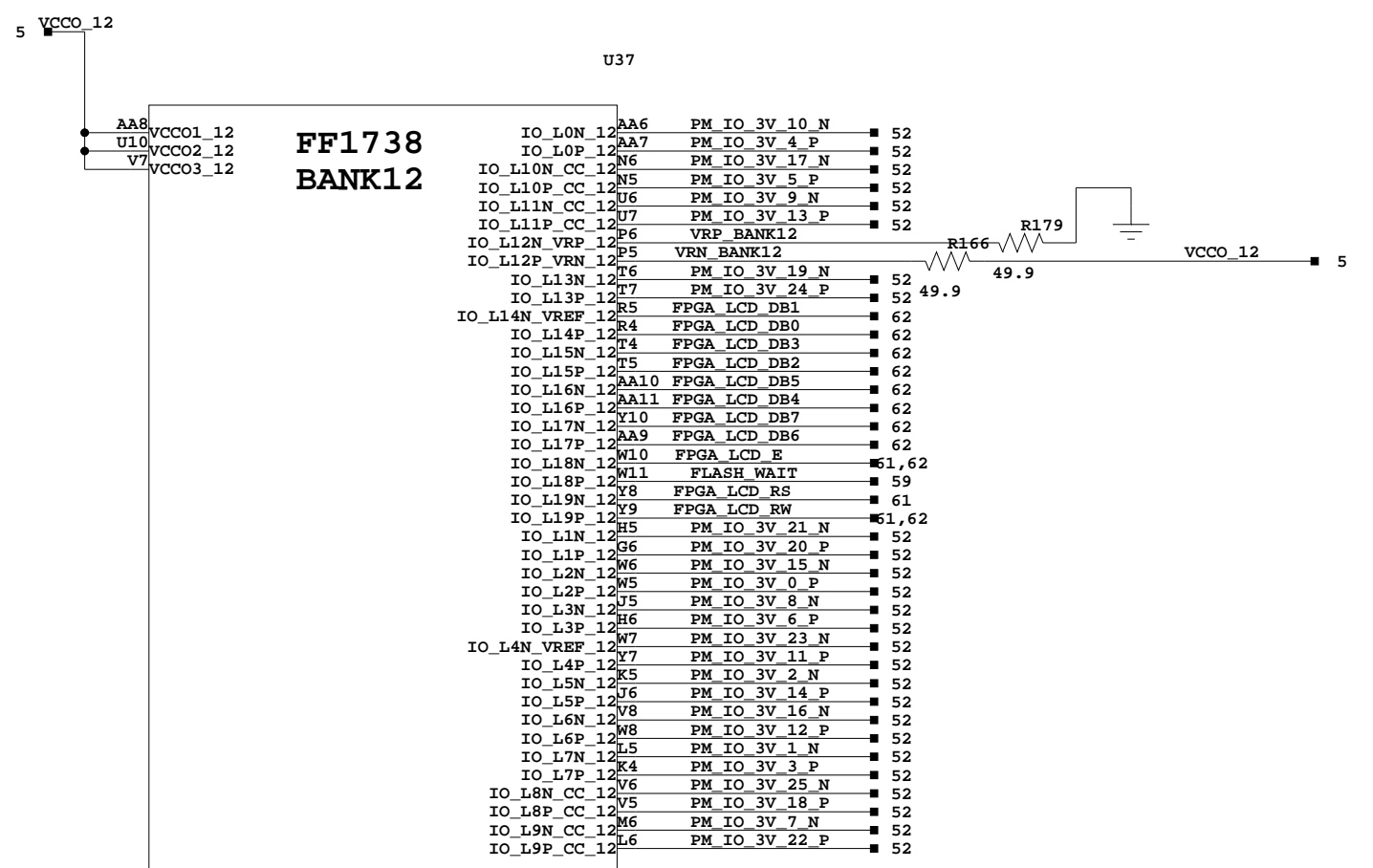
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FPGA - BANK 5,6 - PM, DEBUG

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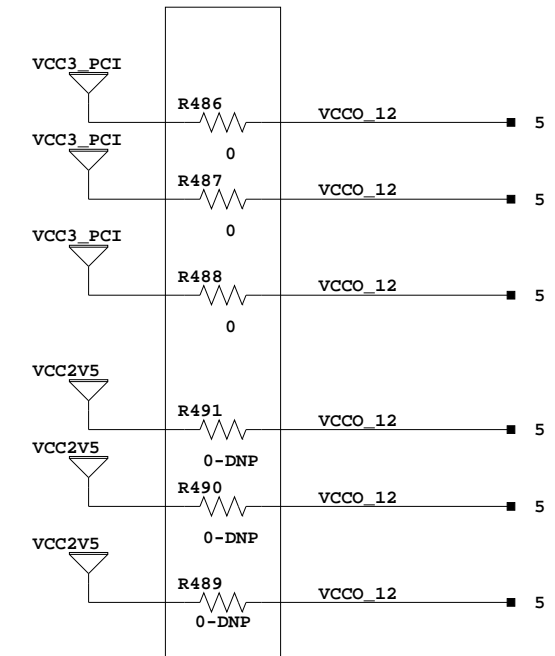
Pin	Signal	Function	Value
P40	DIMM0_DDR2_A1		25,26
AA42	DIMM0_DDR2_A0		25,26
Y38	DIMM1_DDR2_PLL_CLKIN_N		29
Y39	DIMM1_DDR2_PLL_CLKIN_P		29
Y41	DIMM1_DDR2_RAS_B		28,29
V40	DIMM1_DDR2_WE_B		28,29
W41	DIMM1_DDR2_A13		28,29
Y42	DIMM1_DDR2_CAS_B		28,29
G41	DIMM1_DDR2_A11		28,29
F41	DIMM1_DDR2_A12		28,29
T41			
W42	DIMM1_DDR2_A10		28,29
G42	DIMM1_DDR2_A8		28,29
F42	DIMM1_DDR2_A9		28,29
H41	DIMM1_DDR2_A6		28,29
J42	DIMM1_DDR2_A7		28,29
L42	DIMM1_DDR2_A4		28,29
M42	DIMM1_DDR2_A5		28,29
M41	DIMM1_DDR2_A2		28,29
K42	DIMM1_DDR2_A3		28,29
R40	DIMM1_DDR2_A0		28,29
J41	DIMM1_DDR2_A1		28,29
T42	DIMM0_DDR2_A3		25,26
U41	DIMM0_DDR2_A2		25,26
T40	DIMM0_DDR2_A5		25,26
U42	DIMM0_DDR2_A4		25,26
R42	DIMM0_DDR2_A7		25,26
P41	DIMM0_DDR2_A6		25,26
L41			
P42	DIMM0_DDR2_A8		25,26
AA41	DIMM0_DDR2_A10		25,26
L40	DIMM0_DDR2_A9		25,26
N41	DIMM0_DDR2_A12		25,26
N40	DIMM0_DDR2_A11		25,26
AA37	DIMM0_DDR2_CAS_B		25,26
Y37	DIMM0_DDR2_A13		25,26
Y40	DIMM0_DDR2_WE_B		25,26
W40	DIMM0_DDR2_RAS_B		25,26
AA39	DIMM0_DDR2_PLL_CLKIN_N		26
AA40	DIMM0_DDR2_PLL_CLKIN_P		26

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Pin	Signal	Function	Value
AA6	PM_IO_3V_10_N		52
AA7	PM_IO_3V_4_P		52
N6	PM_IO_3V_17_N		52
N5	PM_IO_3V_5_P		52
U6	PM_IO_3V_9_N		52
U7	PM_IO_3V_13_P		52
P6	VRP_BANK12		52
P5	VRN_BANK12		52
T6	PM_IO_3V_19_N		52
T7	PM_IO_3V_24_P		52
R5	FPGA_LCD_DB1		62
R4	FPGA_LCD_DB0		62
T4	FPGA_LCD_DB3		62
T5	FPGA_LCD_DB2		62
AA10	FPGA_LCD_DB5		62
AA11	FPGA_LCD_DB4		62
Y10	FPGA_LCD_DB7		62
AA9	FPGA_LCD_DB6		62
W10	FPGA_LCD_E		62
W11	FLASH_WAIT		61,62
V8	FPGA_LCD_RS		59
V8	FPGA_LCD_RW		61
Y9	FPGA_LCD_RW		61,62
H5	PM_IO_3V_21_N		52
G6	PM_IO_3V_20_P		52
W6	PM_IO_3V_15_N		52
W5	PM_IO_3V_0_P		52
J5	PM_IO_3V_8_N		52
H6	PM_IO_3V_6_P		52
W7	PM_IO_3V_23_N		52
Y7	PM_IO_3V_11_P		52
K5	PM_IO_3V_2_N		52
J6	PM_IO_3V_14_P		52
V8	PM_IO_3V_16_N		52
W8	PM_IO_3V_12_P		52
L5	PM_IO_3V_1_N		52
K4	PM_IO_3V_3_P		52
V6	PM_IO_3V_25_N		52
V5	PM_IO_3V_18_P		52
M6	PM_IO_3V_7_N		52
L6	PM_IO_3V_22_P		52

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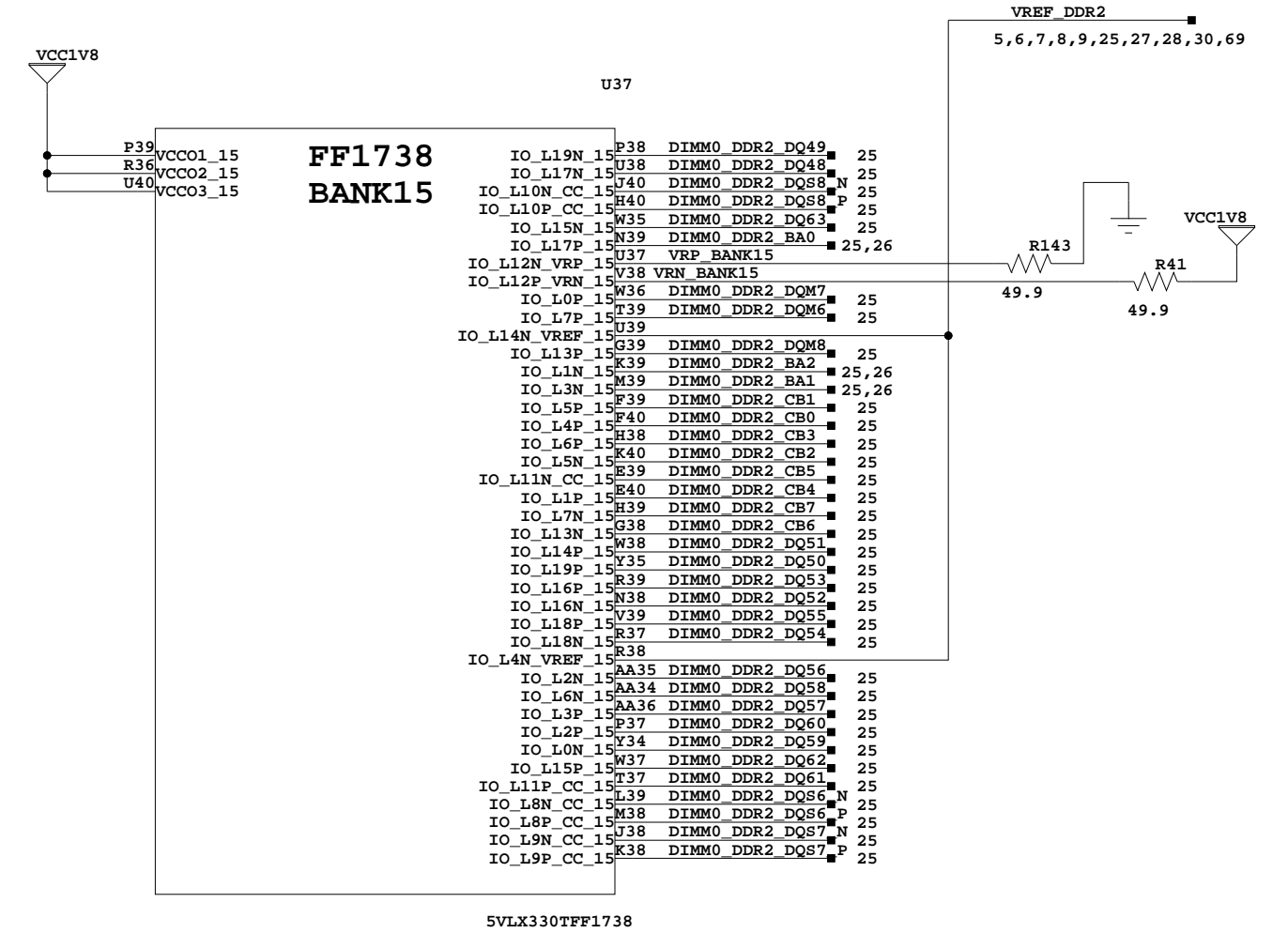
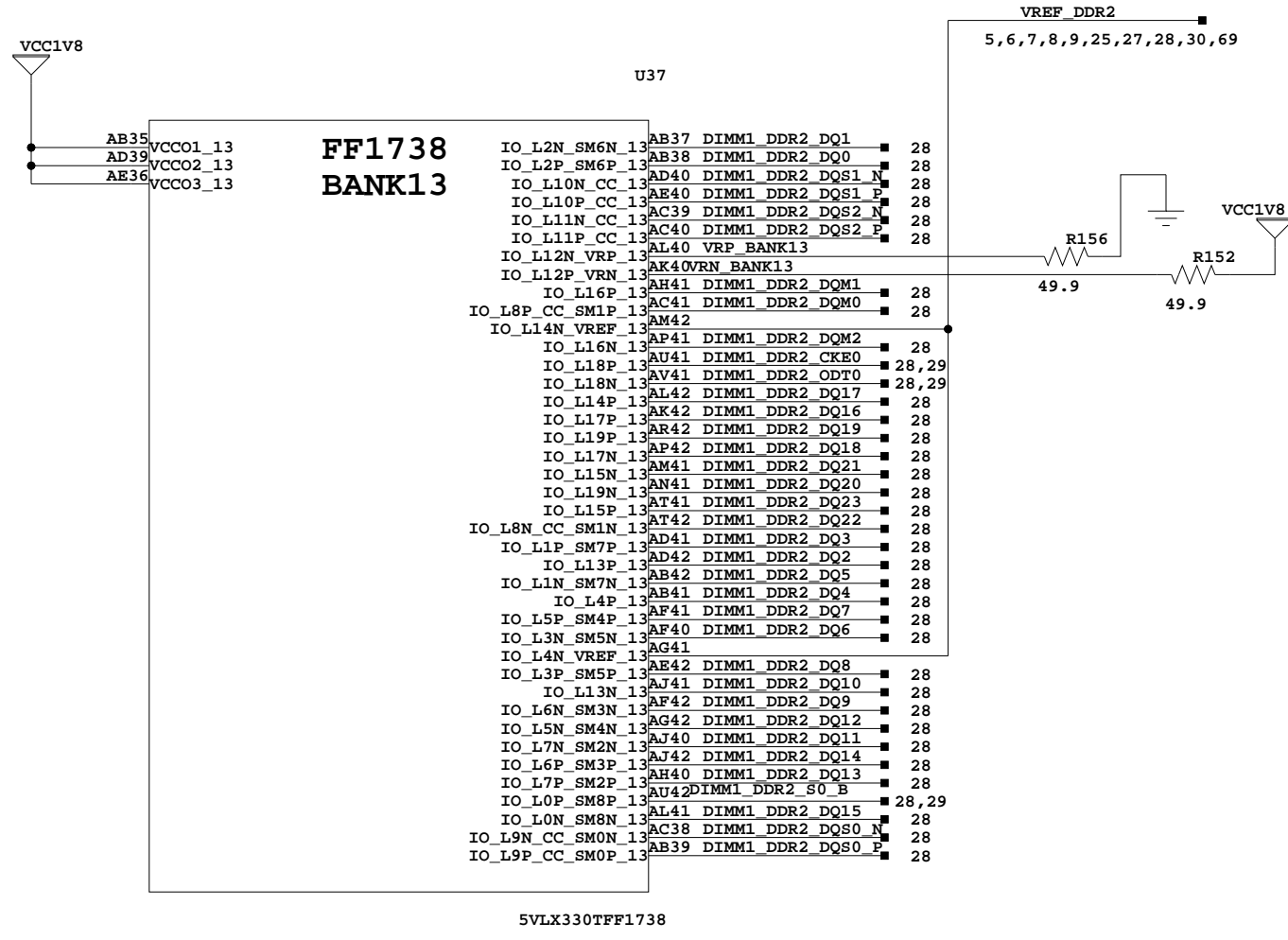
FPGA - BANK 11,12



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 FPGA - BANK 11,12 DDR2, PM, LCD

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FPGA - BANK 13,15



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FPGA - BANK 13,15 - DDR2

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VCC1V8

AG40
AH37
AK41

VCC01_17
VCC02_17
VCC03_17

FF1738
BANK17

IO_L0N_17	AC34	DIMM1_DDR2_DQ25	28
IO_L2P_17	AB36	DIMM1_DDR2_DQ24	28
IO_L10N_CC_17	AU39	DIMM1_DDR2_DQ84_N	28
IO_L10P_CC_17	AV40	DIMM1_DDR2_DQ84_P	28
IO_L11N_CC_17	AR39	DIMM1_DDR2_DQ85_N	28
IO_L11P_CC_17	AT39	DIMM1_DDR2_DQ85_P	28
IO_L12N_VRN_17	AH39	VRN_BANK17	28
IO_L12P_VRN_17	AG39	VRN_BANK17	28
IO_L7N_17	AG37	DIMM1_DDR2_DQ4	28
IO_L4P_17	AC36	DIMM1_DDR2_DQ3	28
IO_L14N_VREF_17	AK37		28
IO_L18N_17	AN40	DIMM1_DDR2_DQ5	28
IO_L5P_17	AE39	DIMM1_DDR2_CKE1	28,29
IO_L8P_CC_17	AF37	DIMM1_DDR2_ODT1	28,29
IO_L6P_17	AP40	DIMM1_DDR2_DQ41	28
IO_L18P_17	AM38	DIMM1_DDR2_DQ40	28
IO_L17N_17	AP38	DIMM1_DDR2_DQ43	28
IO_L19N_17	AM37	DIMM1_DDR2_DQ42	28
IO_L16P_17	AK38	DIMM1_DDR2_DQ45	28
IO_L19P_17	AL39	DIMM1_DDR2_DQ44	28
IO_L5N_17	AN39	DIMM1_DDR2_DQ47	28
IO_L17P_17	AN38	DIMM1_DDR2_DQ46	28
IO_L0P_17	AE38	DIMM1_DDR2_DQ27	28
IO_L2N_17	AD36	DIMM1_DDR2_DQ26	28
IO_L3P_17	AC35	DIMM1_DDR2_DQ29	28
IO_L13P_17	AB34	DIMM1_DDR2_DQ28	28
IO_L3N_17	AD37	DIMM1_DDR2_DQ31	28
IO_L1P_17	AD35	DIMM1_DDR2_DQ30	28
IO_L4N_VREF_17	AD38		28
IO_L8N_CC_17	AJ38	DIMM1_DDR2_DQ32	28
IO_L1N_17	AL37	DIMM1_DDR2_DQ34	28
IO_L15N_17	AH38	DIMM1_DDR2_DQ33	28
IO_L7P_17	AF39	DIMM1_DDR2_DQ36	28
IO_L6N_17	AM39	DIMM1_DDR2_DQ35	28
IO_L15P_17	AK39	DIMM1_DDR2_DQ38	28
IO_L13N_17	AG38	DIMM1_DDR2_DQ37	28
IO_L16N_17	AE37	DIMM1_DDR2_S1_B	28,29
IO_L14P_17	AJ37	DIMM1_DDR2_DQ39	28
IO_L9N_CC_17	AT40	DIMM1_DDR2_DQ83_N	28
IO_L9P_CC_17	AR40	DIMM1_DDR2_DQ83_P	28

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VREF_DDR2
5,6,8,9,25,27,28,30,69

R244
49.9

R206
49.9

VCC1V8

VCC2V5

AD9
AE6
AG10

VCC01_18
VCC02_18
VCC03_18

FF1738
BANK18

IO_L0N_18	AK7	PM_IO_39_N	52
IO_L0P_18	AJ7	PM_IO_38_P	52
IO_L10N_CC_18	AC6	PM_IO_59_N	52
IO_L10P_CC_18	AC5	PM_IO_58_P	52
IO_L11N_CC_18	AF6	PM_IO_61_N	52
IO_L11P_CC_18	AF5	PM_IO_60_P	52
IO_L12N_VRN_18	AD7	VRN_BANK18	52
IO_L12P_VRN_18	AD6	VRN_BANK18	52
IO_L13N_18	AG7	PM_IO_63_N	52
IO_L13P_18	AG6	PM_IO_62_P	52
IO_L14N_VREF_18	AD5	PM_IO_65_N	52
IO_L14P_18	AE5	PM_IO_64_P	52
IO_L15N_18	AF7	PM_IO_66_N	52
IO_L15P_18	AE8	PM_IO_69_P	52
IO_L16N_18	AE8	PM_IO_69_N	52
IO_L16P_18	AD8	PM_IO_68_P	52
IO_L17N_18	AF10	PM_IO_71_N	52
IO_L17P_18	AF9	PM_IO_70_P	52
IO_L18N_18	AE10	PM_IO_73_N	52
IO_L18P_18	AE9	PM_IO_72_P	52
IO_L19N_18	AF12	PM_IO_75_N	52
IO_L19P_18	AF11	PM_IO_74_P	52
IO_L1N_18	AC10	PM_IO_41_N	52
IO_L1P_18	AB11	PM_IO_40_P	52
IO_L2N_18	AK5	PM_IO_43_N	52
IO_L2P_18	AL5	PM_IO_42_P	52
IO_L3N_18	AB8	PM_IO_45_N	52
IO_L3P_18	AB9	PM_IO_44_P	52
IO_L4N_VREF_18	AJ5	PM_IO_47_N	52
IO_L4P_18	AJ6	PM_IO_46_P	52
IO_L5N_18	AC9	PM_IO_49_N	52
IO_L5P_18	AC8	PM_IO_48_P	52
IO_L6N_18	AH5	PM_IO_51_N	52
IO_L6P_18	AH6	PM_IO_50_P	52
IO_L7N_18	AD11	PM_IO_53_N	52
IO_L7P_18	AD10	PM_IO_52_P	52
IO_L8N_CC_18	AH4	PM_IO_55_N	52
IO_L8P_CC_18	AG4	PM_IO_54_P	52
IO_L9N_CC_18	AB6	PM_IO_57_N	52
IO_L9P_CC_18	AB7	PM_IO_56_P	52

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R199
49.9

R198
49.9

VCC2V5

FPGA - BANK 17,18



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
FPGA - BANK 17,18 - DDR2, PM

Date:	8-1-2008_15:03	Ver:	C
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VCC1V8

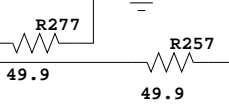
G40 VCC01_19
K41 VCC02_19
L38 VCC03_19

FF1738 BANK19

IO_L8P_CC_19	G36	DIMM0_DDR2_DQ25	25
IO_L18P_19	F37	DIMM0_DDR2_DQ24	25
IO_L10N_CC_19	F36	DIMM0_DDR2_DQS4_N	25
IO_L10P_CC_19	R35	DIMM0_DDR2_DQS4_P	25
IO_L11N_CC_19	V36	DIMM0_DDR2_DQS5_N	25
IO_L11P_CC_19	U36	DIMM0_DDR2_DQS5_P	25
IO_L12N_VRP_19	G37	VRP_BANK19	25
IO_L12P_VRN_19	H36	VRN_BANK19	25
IO_L0N_19	M36	DIMM0_DDR2_DQM4	25
IO_L13P_19	F36	DIMM0_DDR2_DQM3	25
IO_L14N_VREF_19	E37		25
IO_L0P_19	V35	DIMM0_DDR2_DQM5	25
IO_L2P_19	L37	DIMM0_DDR2_CKE1	25,26
IO_L2N_19	K35	DIMM0_DDR2_ODT1	25,26
IO_L5N_19	W32	DIMM0_DDR2_DQ41	25
IO_L14P_19	V33	DIMM0_DDR2_DQ40	25
IO_L19N_19	AA32	DIMM0_DDR2_DQ43	25
IO_L16P_19	Y32	DIMM0_DDR2_DQ42	25
IO_L16N_19	T35	DIMM0_DDR2_DQ45	25
IO_L19P_19	R34	DIMM0_DDR2_DQ44	25
IO_L17N_19	W33	DIMM0_DDR2_DQ47	25
IO_L17P_19	Y33	DIMM0_DDR2_DQ46	25
IO_L13N_19	K37	DIMM0_DDR2_DQ27	25
IO_L4P_19	J36	DIMM0_DDR2_DQ26	25
IO_L8N_CC_19	E38	DIMM0_DDR2_DQ29	25
IO_L15N_19	D37	DIMM0_DDR2_DQ28	25
IO_L5P_19	J37	DIMM0_DDR2_DQ31	25
IO_L7N_19	H35	DIMM0_DDR2_DQ30	25
IO_L4N_VREF_19	L35		25
IO_L7P_19	N35	DIMM0_DDR2_DQ32	25
IO_L6N_19	V34	DIMM0_DDR2_DQ34	25
IO_L15P_19	P36	DIMM0_DDR2_DQ33	25
IO_L1P_19	J35	DIMM0_DDR2_DQ36	25
IO_L3P_19	U34	DIMM0_DDR2_DQ35	25
IO_L3N_19	N36	DIMM0_DDR2_DQ38	25
IO_L1N_19	L36	DIMM0_DDR2_DQ37	25
IO_L18N_19	M37	DIMM0_DDR2_S1_B	25
IO_L6P_19	P35	DIMM0_DDR2_DQ39	25,26
IO_L9N_CC_19	U33	DIMM0_DDR2_DQS3_N	25
IO_L9P_CC_19	T34	DIMM0_DDR2_DQS3_P	25

5VLX330TFF1738

VREF_DDR2
5,6,7,9,25,27,28,30,69



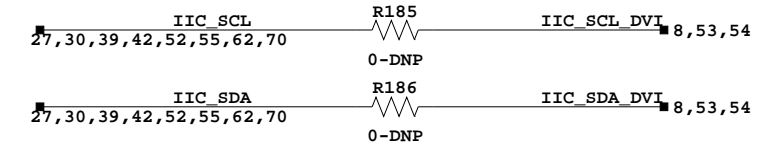
VCC3_PCI

L8 VCC01_20
P9 VCC02_20
R6 VCC03_20

FF1738 BANK20

IO_L0N_20	N8	PCI_P_CBEL_B	33,35,37,40
IO_L0P_20	N9	PCI_P_CBEL_B	33,35,37,40
IO_L10N_CC_20	G8	PCI_P_SERR_B	33,35,37,38,40
IO_L10P_CC_20	G7	PCI_P_PERR_B	33,35,37,38
IO_L11N_CC_20	J9	PCI_P_CLK1_R	39
IO_L11P_CC_20	U8	PCI_P_CLK0_R	39
IO_L12N_VRP_20	H9	UART0_TXD	44
IO_L12P_VRN_20	H8	UART0_CTS_B	44
IO_L13N_20	F11	UART0_RXD	44
IO_L13P_20	F10	UART1_TXD	44
IO_L14N_VREF_20	J8	UART1_CTS_B	44
IO_L14P_20	V11	UART1_RXD	44
IO_L15N_20	V11	PCI_P_CLK4_R	39
IO_L15P_20	K9	UART1_RTS_B	44
IO_L16N_20	K8	FPGA_SDA	39
IO_L16P_20	L7	FPGA_SCL	39
IO_L17N_20	K7	FLASH_RESET_B	39
IO_L17P_20	M8	DVI_DE	59
IO_L18N_20	M7	IIC_SDA_DVI	53
IO_L18P_20	L9	IIC_SCL_DVI	8,53,54
IO_L19N_20	M9	PCI_P_CLK3_R	39
IO_L11N_20	E8	PCI_P_PAR	33,35,37,40
IO_L1P_20	E9	PCI_P_CBE0_B	33,35,37,40
IO_L2N_20	F8	PCI_P_IRDY_B	33,35,37,38,40
IO_L2P_20	F7	PCI_P_FRAME_B	33,35,37,38,40
IO_L3N_20	E7	PCI_P_REQ0_B	35,38
IO_L3P_20	D7	PCI_P_REQ2_B	38
IO_L4N_VREF_20	R8	PCI_P_REQ1_B	37,38
IO_L4P_20	R7	PCI_P_REQ4_B	33,38
IO_L5N_20	F6	PCI_P_REQ3_B	38,40,43
IO_L5P_20	F7	PCI_P_GNT1_B	37,38
IO_L6N_20	F9	PCI_P_GNT0_B	35,38
IO_L6P_20	F9	PCI_P_GNT3_B	38,40
IO_L7N_20	F5	PCI_P_GNT2_B	38
IO_L7P_20	E5	PCI_P_GNT4_B	33,38
IO_L8N_CC_20	V10	PCI_P_TRDY_B	33,35,37,38,40
IO_L8P_CC_20	V9	PCI_P_CLK5_R	39
IO_L9N_CC_20	F9	PCI_P_STOP_B	33,35,37,38,40
IO_L9P_CC_20	F9	PCI_P_DEVSEL_B	33,35,37,38,40

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FPGA - BANK 19,20



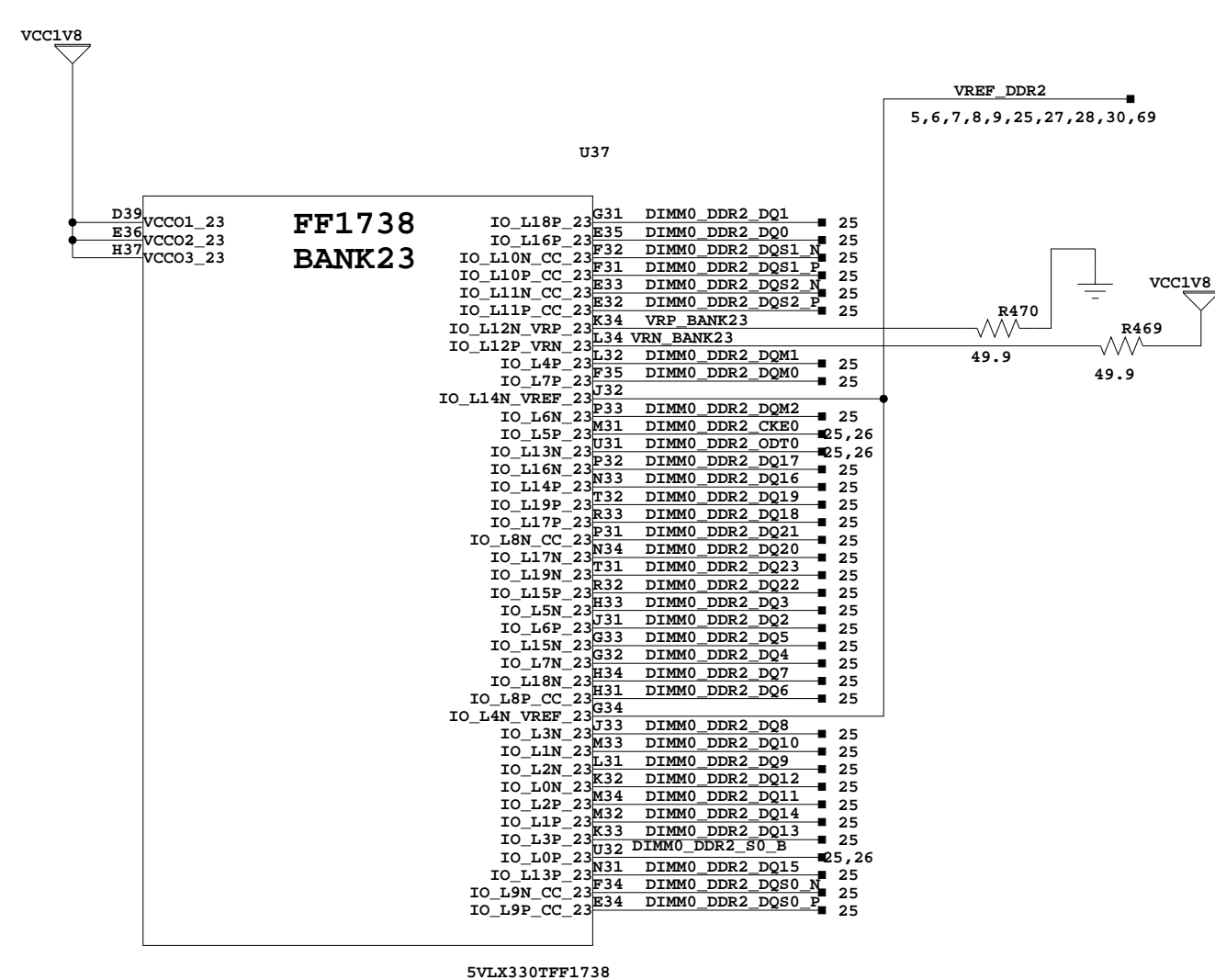
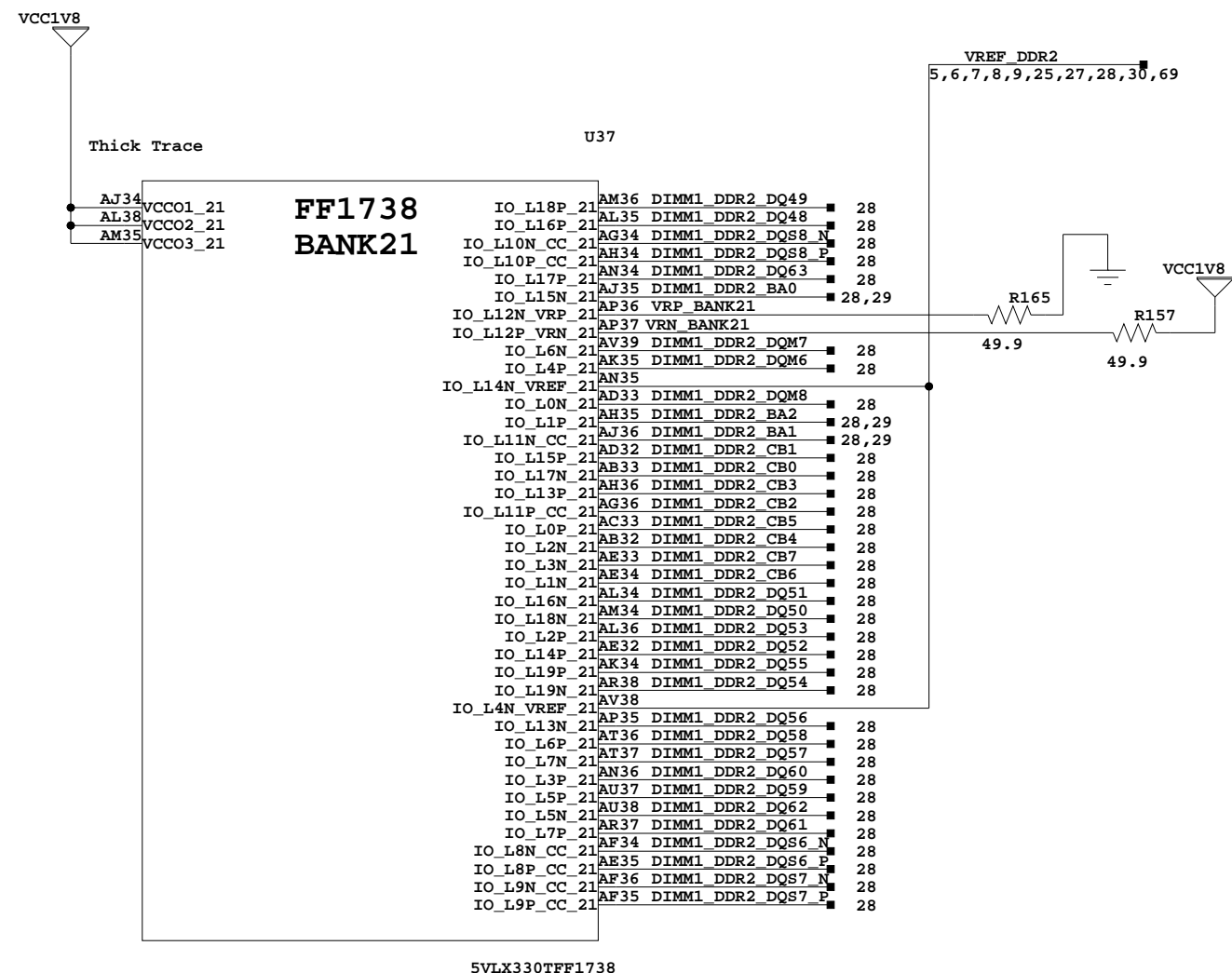
SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
FPGA - BANK 19,20 DDR2, PCI, IIC, UART

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FPGA - BANK 21,23

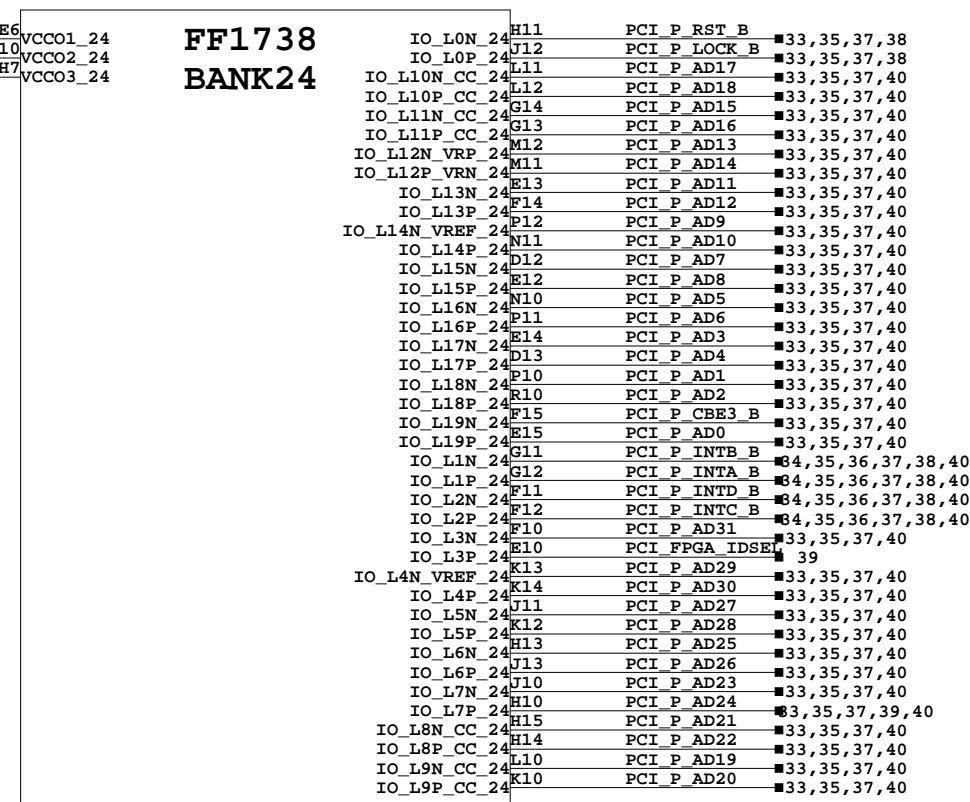


SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM	
FPGA - BANK 21,23 DDR2	
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VCC3_PCI

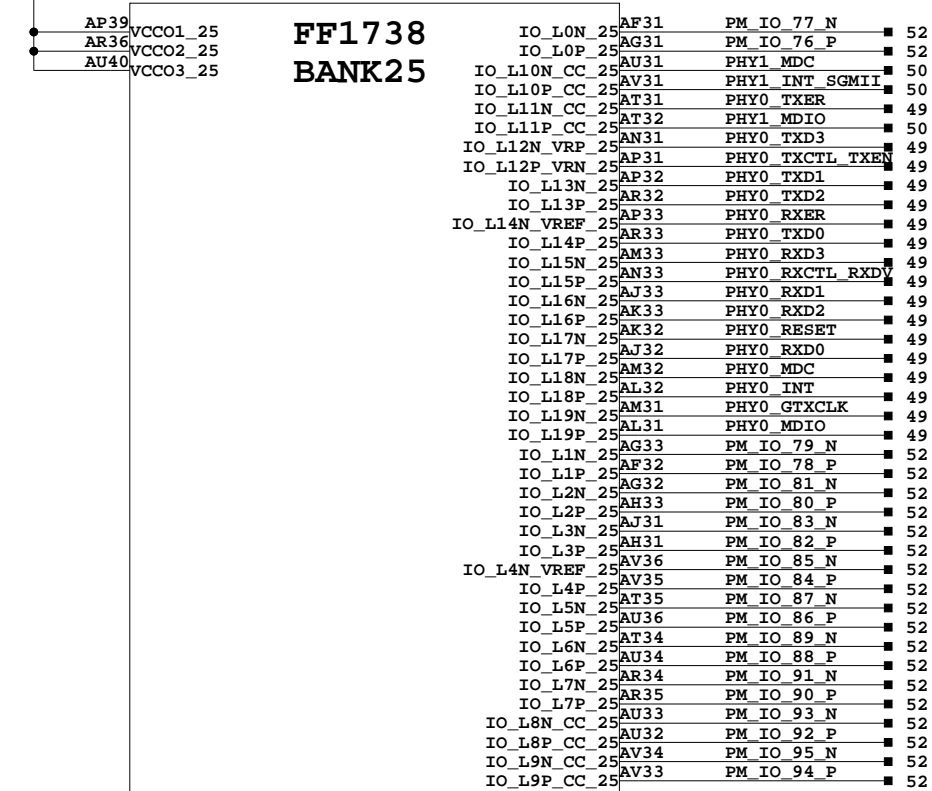
U37



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VCC2V5

U37



5VLX330TFF1738

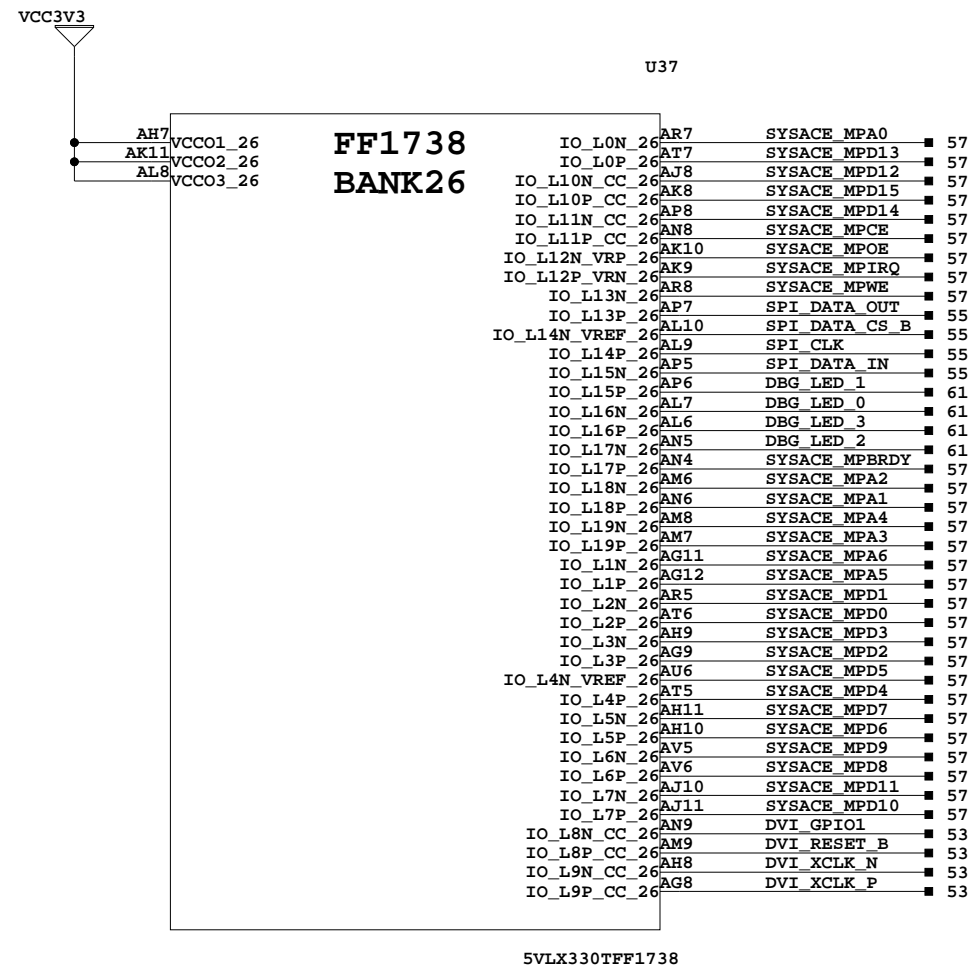
FPGA - BANK 24,25



SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTRM
 FPGA - BANK 24,25 PCI, PERSONALITY MODULE, PHY

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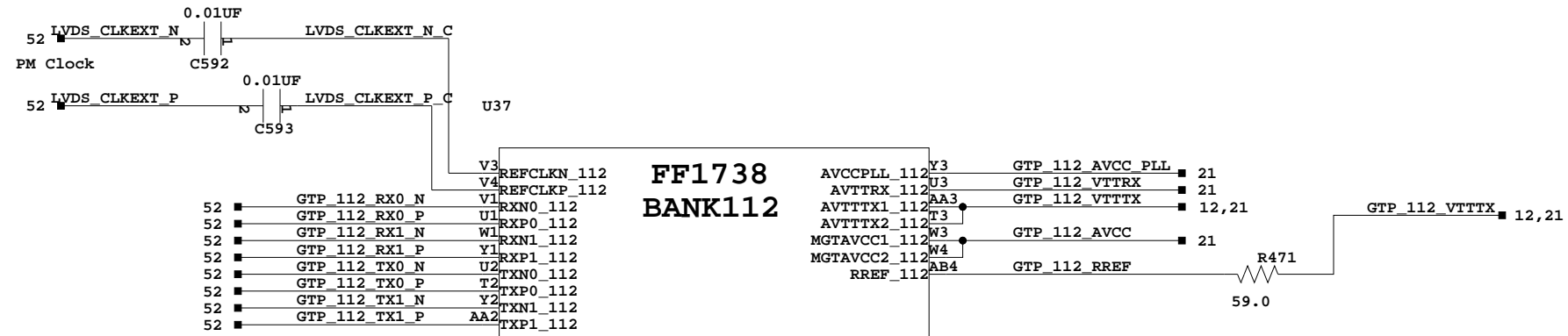
FPGA - BANK 26



SCH P/N 0381255
 ART P/N 0532059
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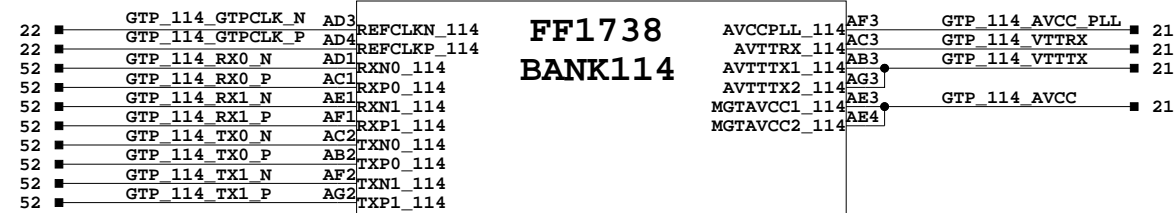
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 FPGA - BANK 26 SYSTEM ACE, DVI, SPI, LEDES

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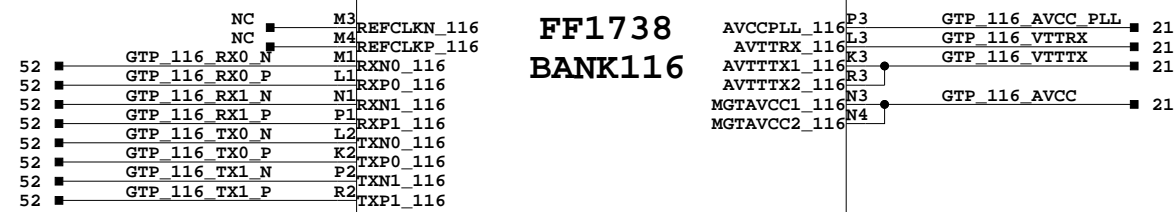
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5VLX330TFF1738

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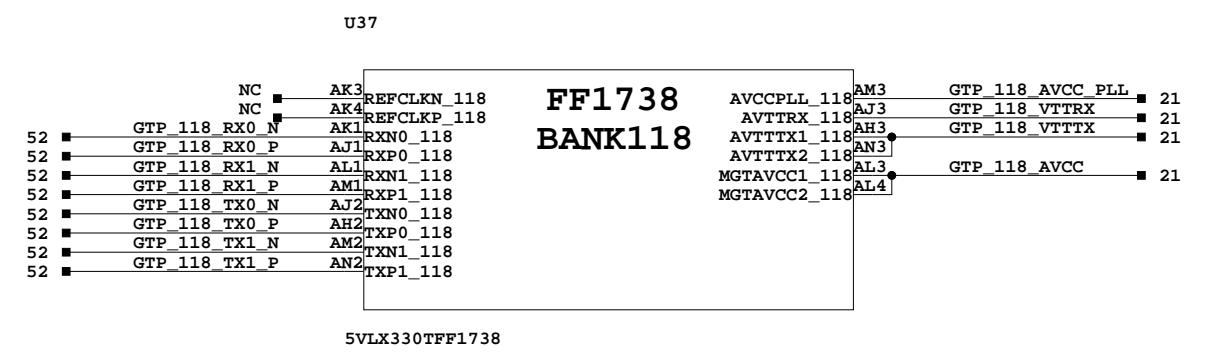
FPGA - BANK 112, 114, 116



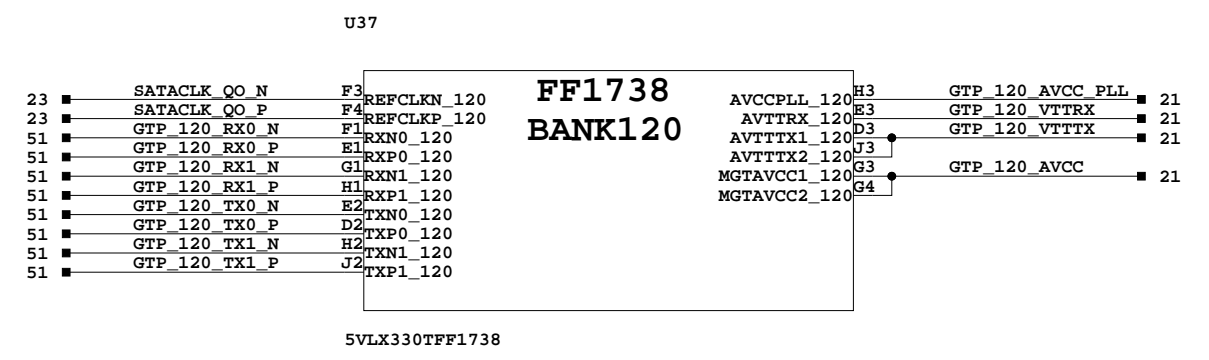
SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 FPGA-BANK 112, 114, 116 PERSONALITY MODULES

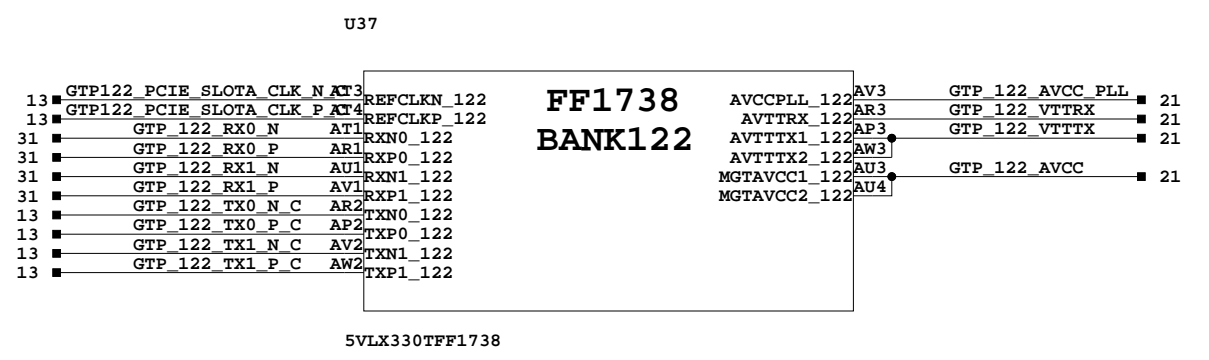
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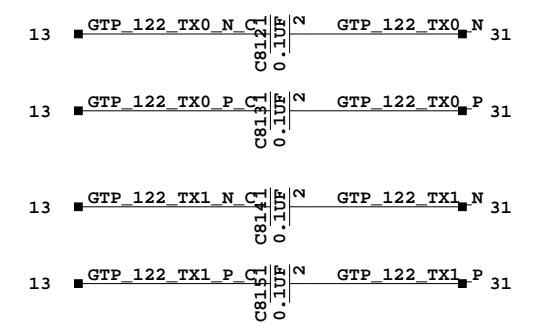
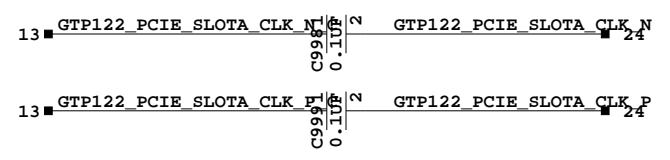
PM



SATA
SATA Clock



PCie Slot A



FPGA - BANK 118,120,122



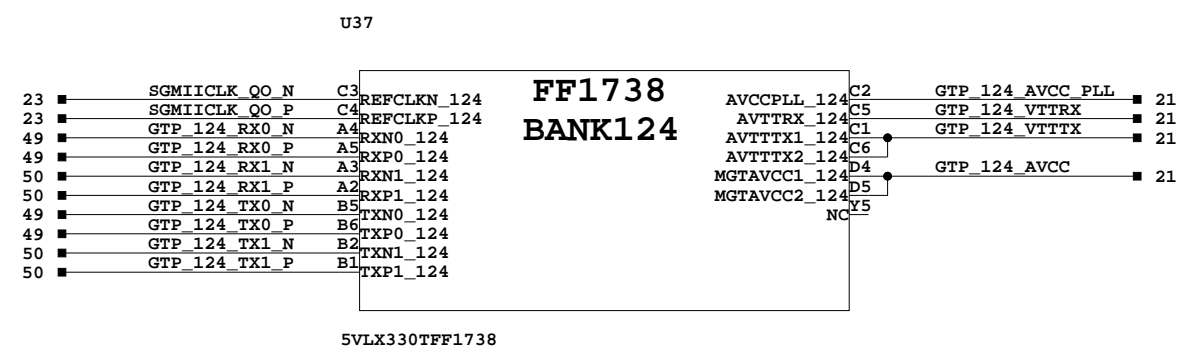
SCH P/N 0381255
 ART P/N 0532059
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Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 FPGA - BANK 118,120,122 PM, SATA, PCI-E

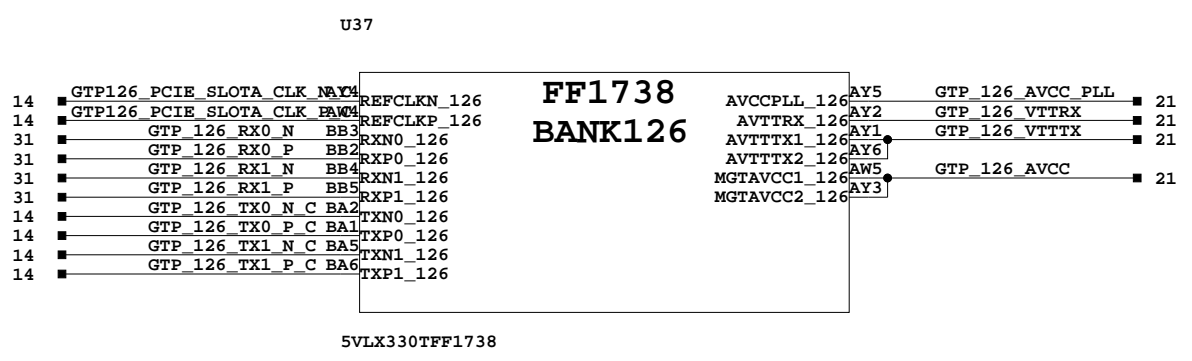
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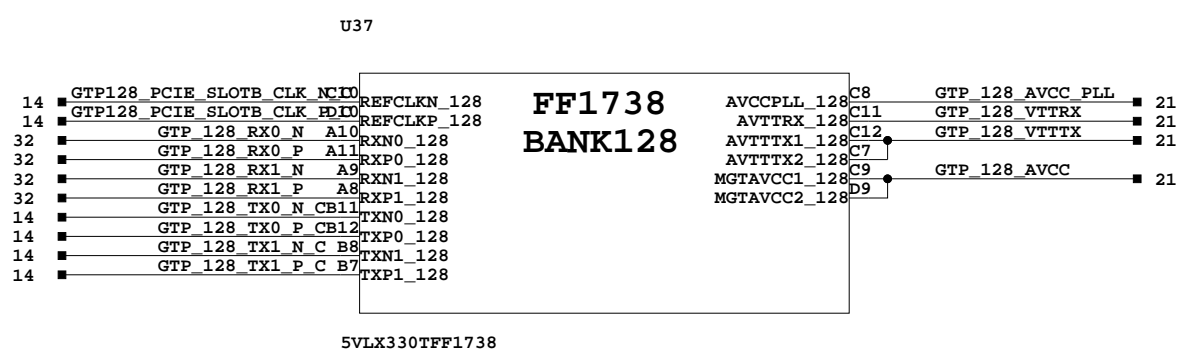
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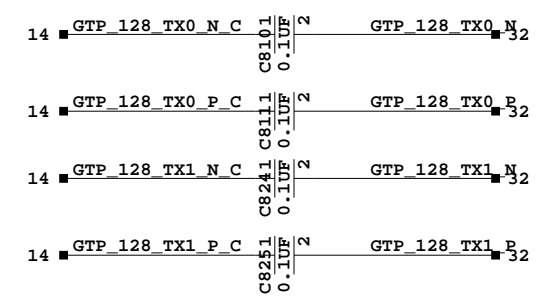
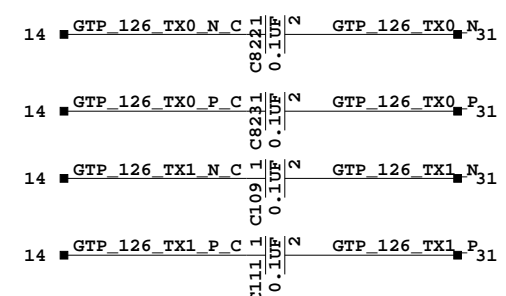
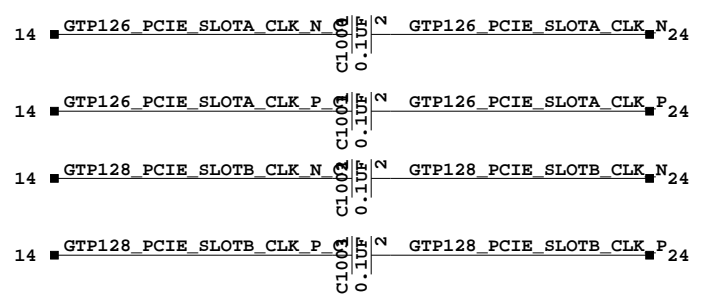
SGMII



PCie Slot A



PCie Slot B
(FX130T / FX200T / LX330T only)



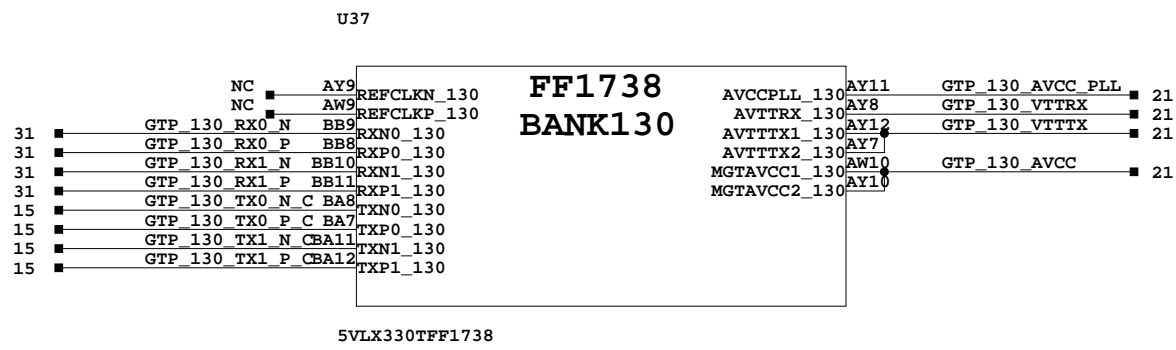
FPGA - BANK 124,126,128



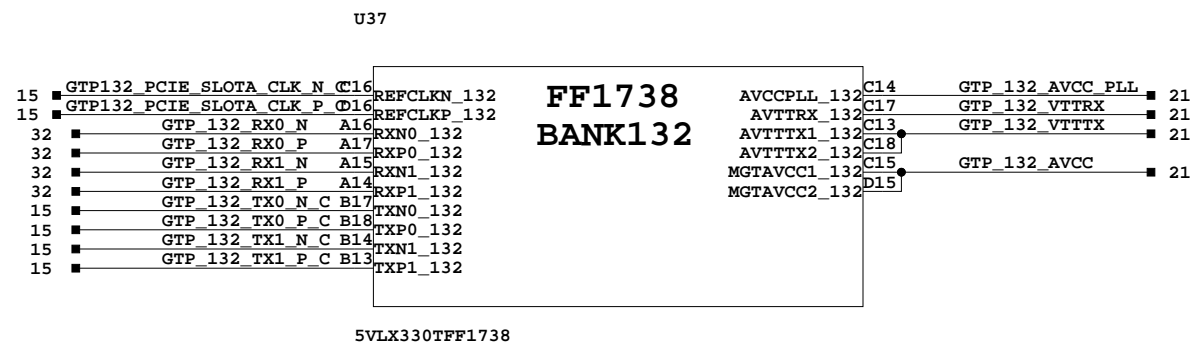
SCH P/N 0381255
 ART P/N 0532059
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Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 FPGA - BANK 124,126,128 SGMII, PCI-E

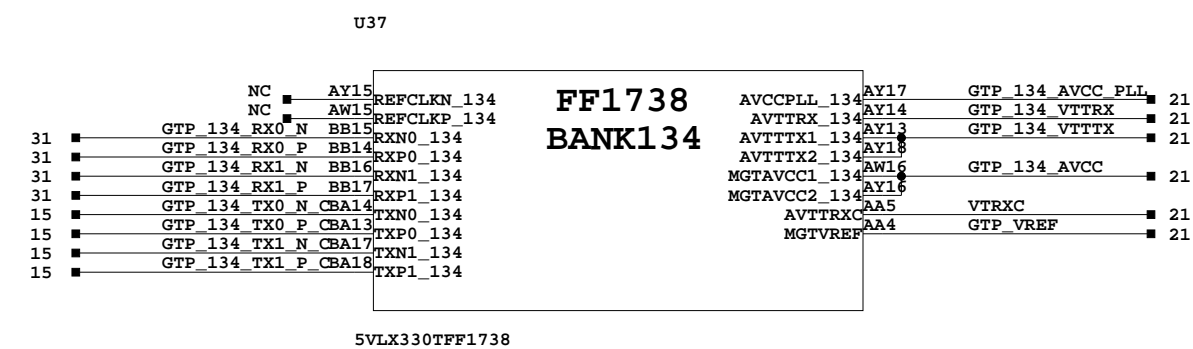
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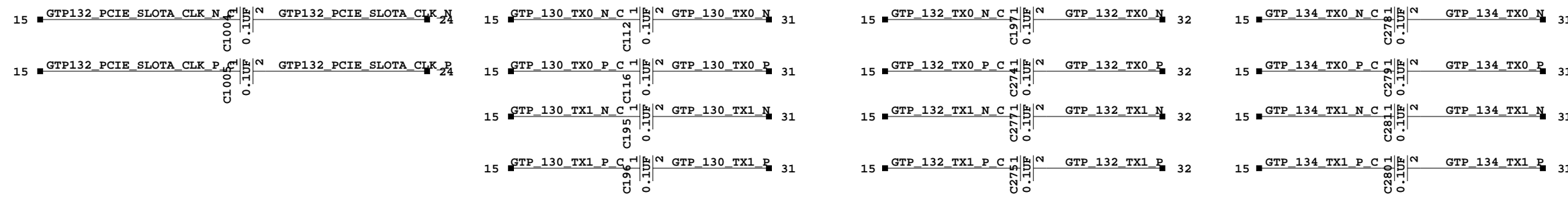
PCie Slot A
(FX130T / FX200T / LX330T only)



PCie Slot B
(FX200T / LX330T only)



PCie Slot A
(FX200T / LX330T only)

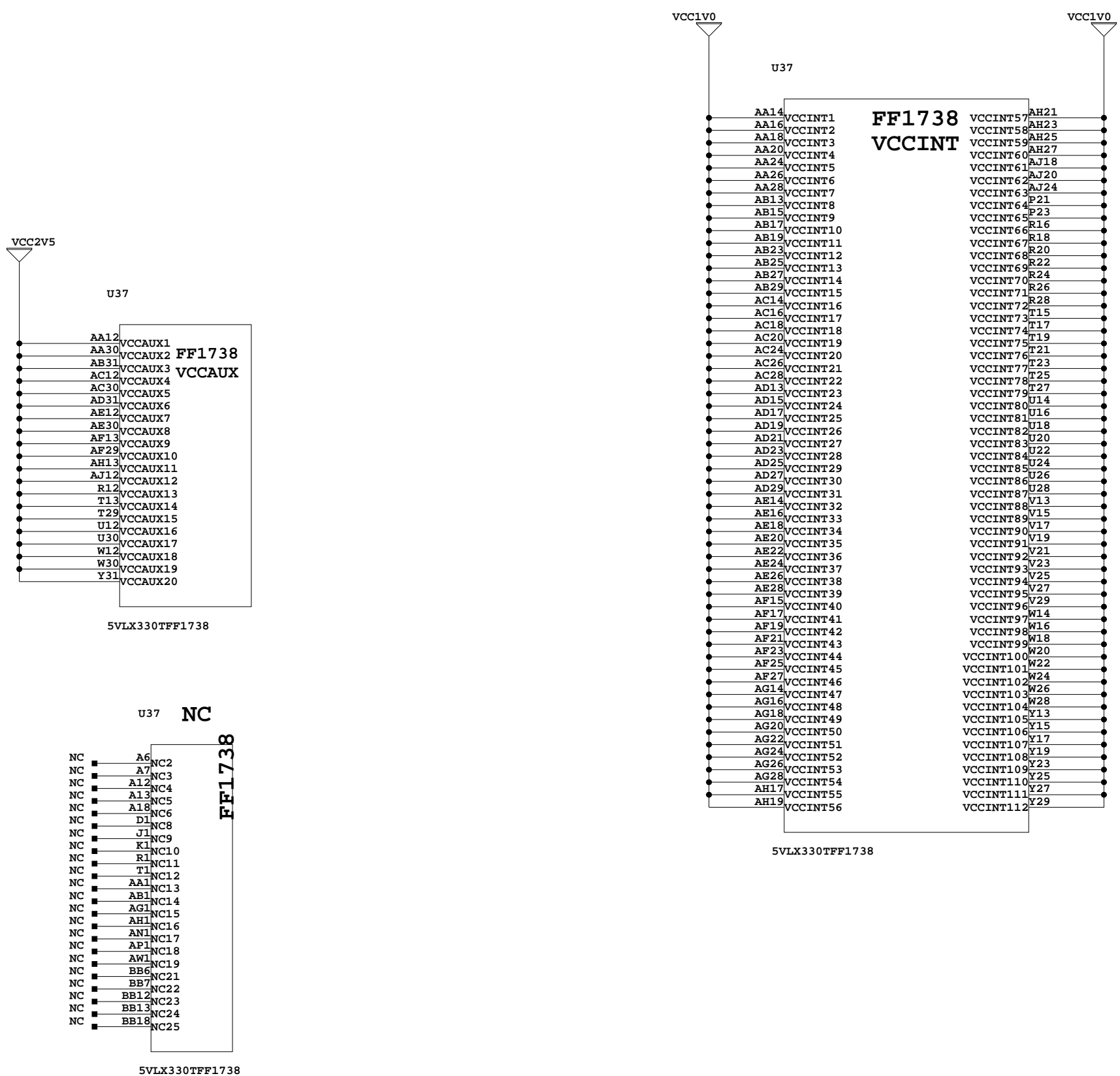


FPGA - BANK 130,132,134

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
FPGA - BANK 130,132,134 PCI-E

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FPGA - VCCAUX, VCCINT, NC

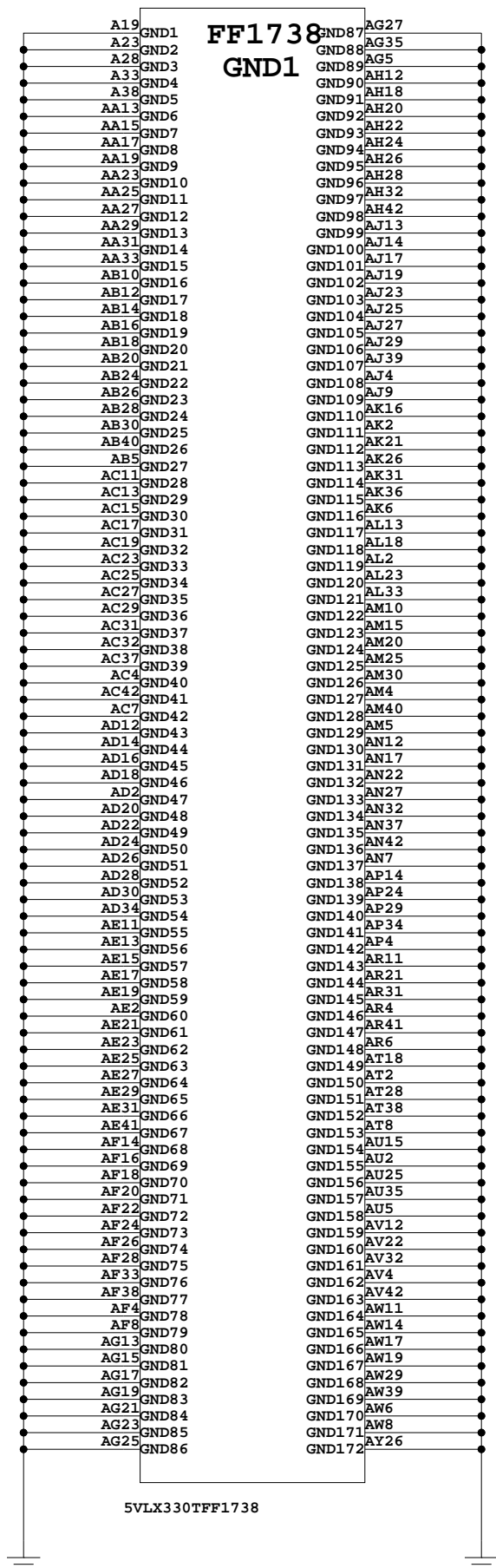


SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

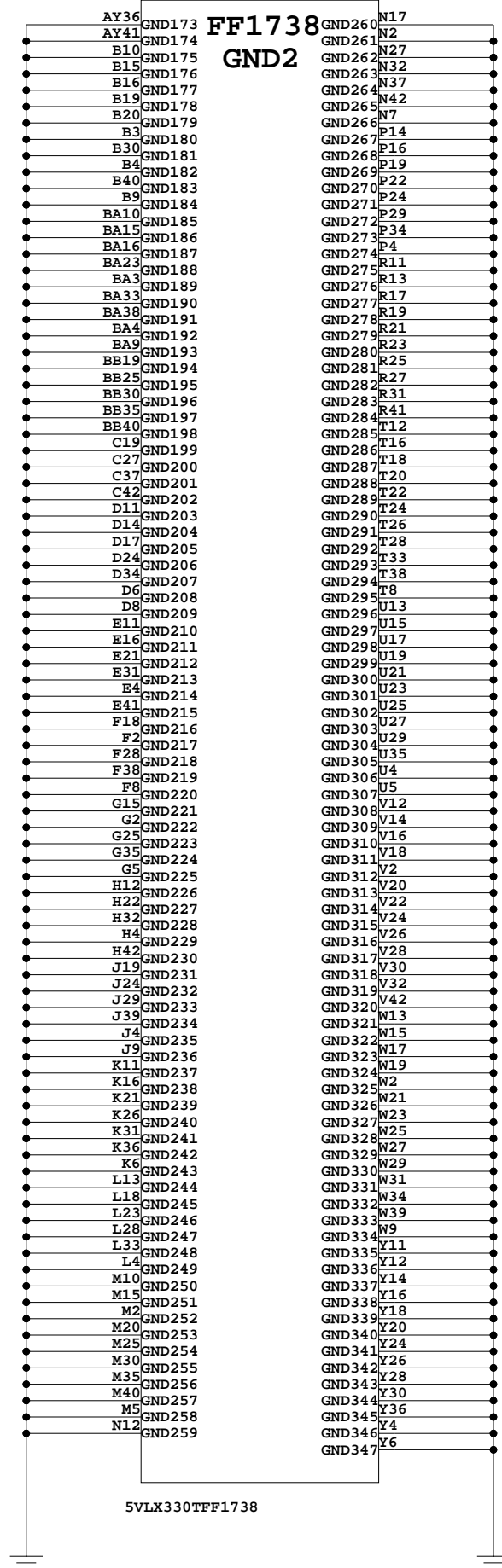
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 FPGA - VCCAUX, VCCINT, NC

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U37



U37



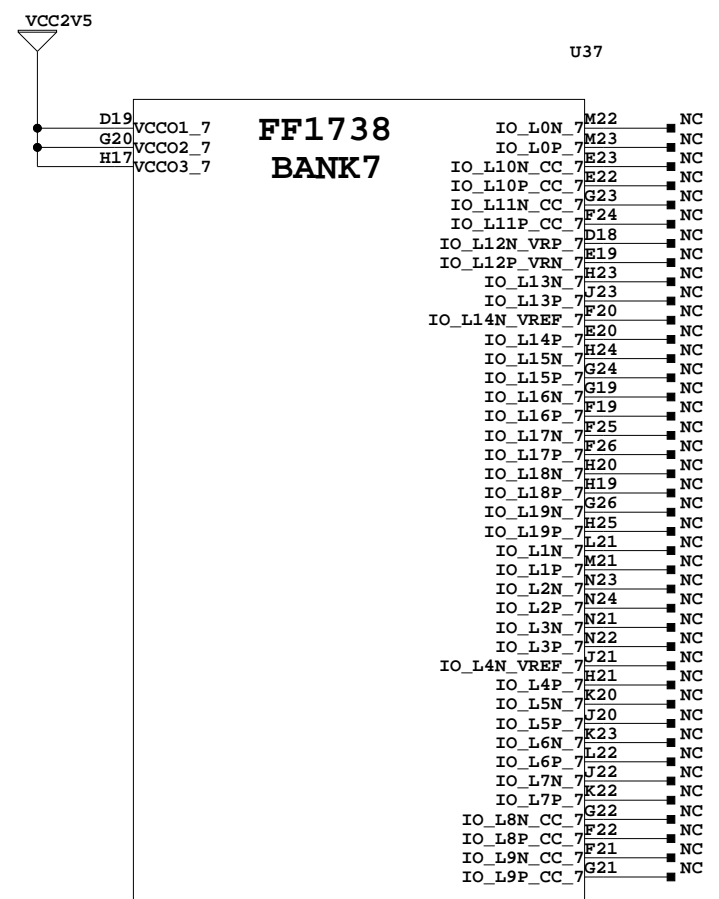
FPGA - GND



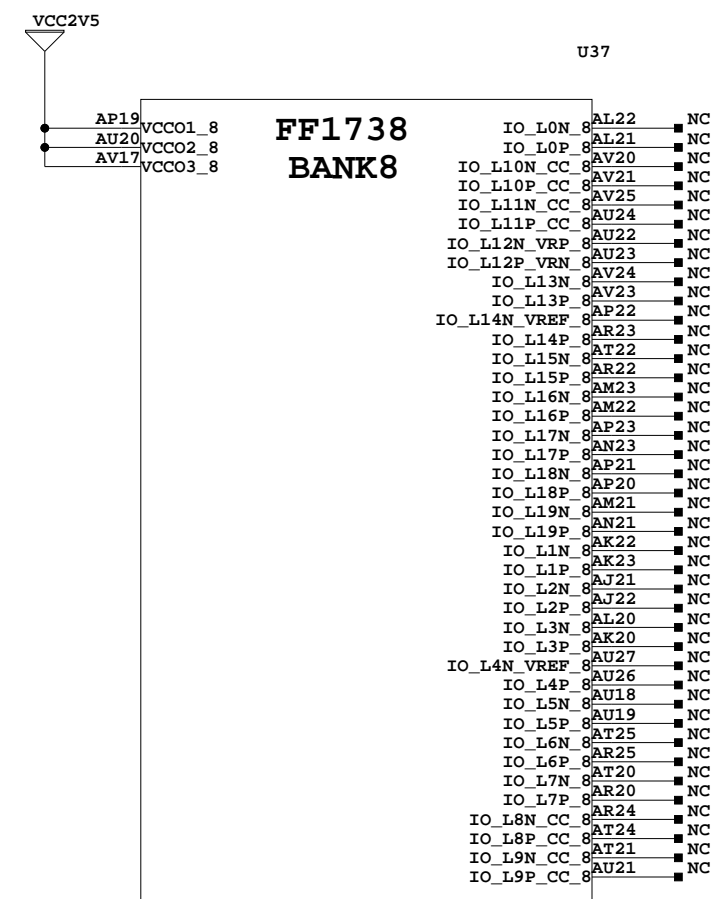
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 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 FPGA GROUND PINS

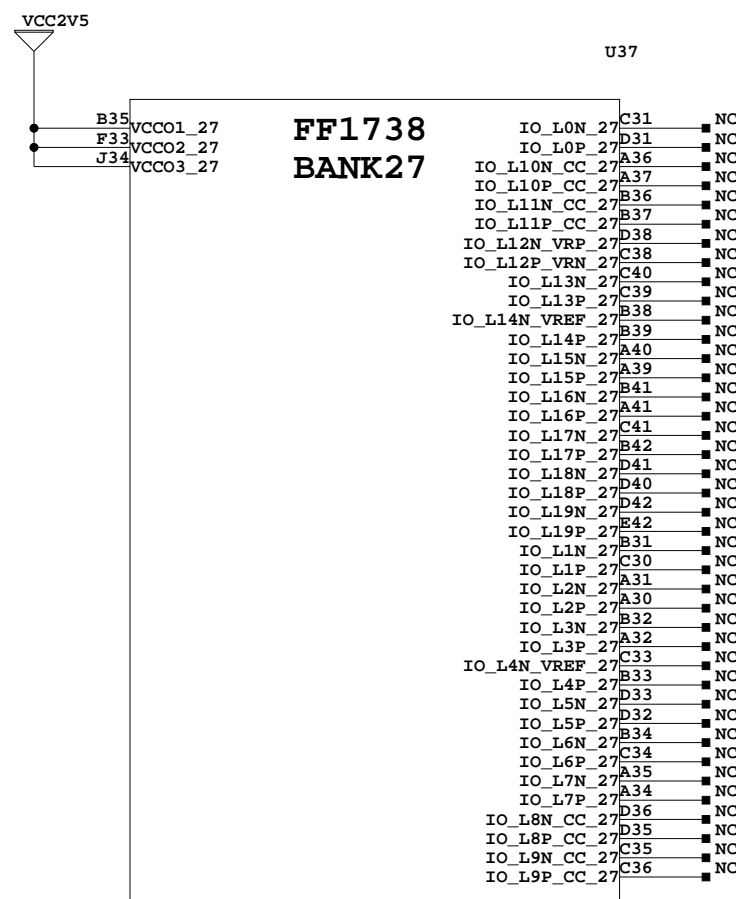
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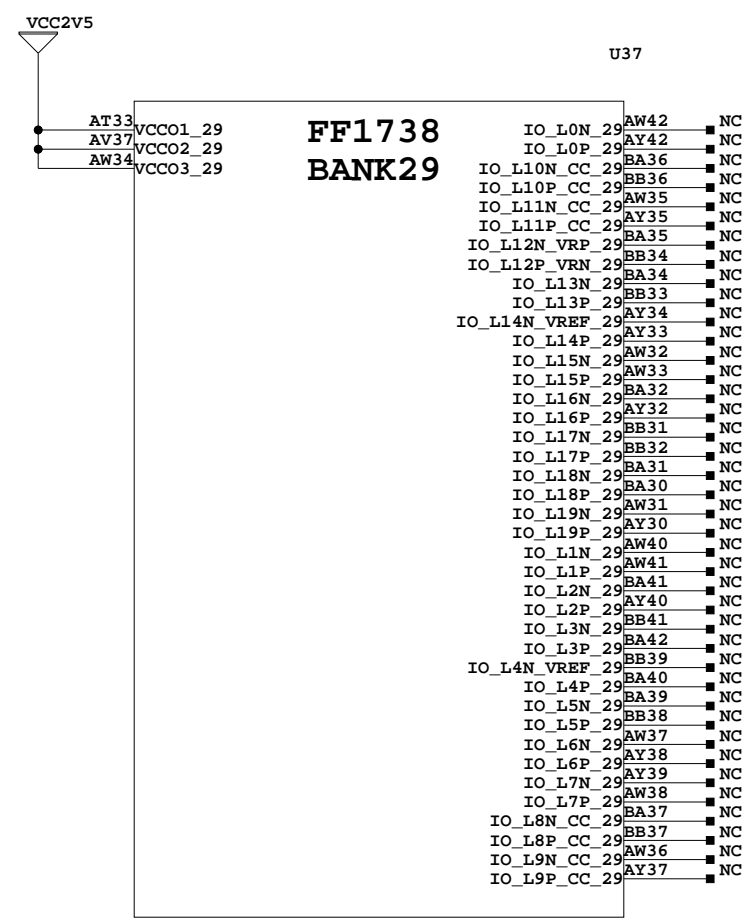
5VLX330TFF1738



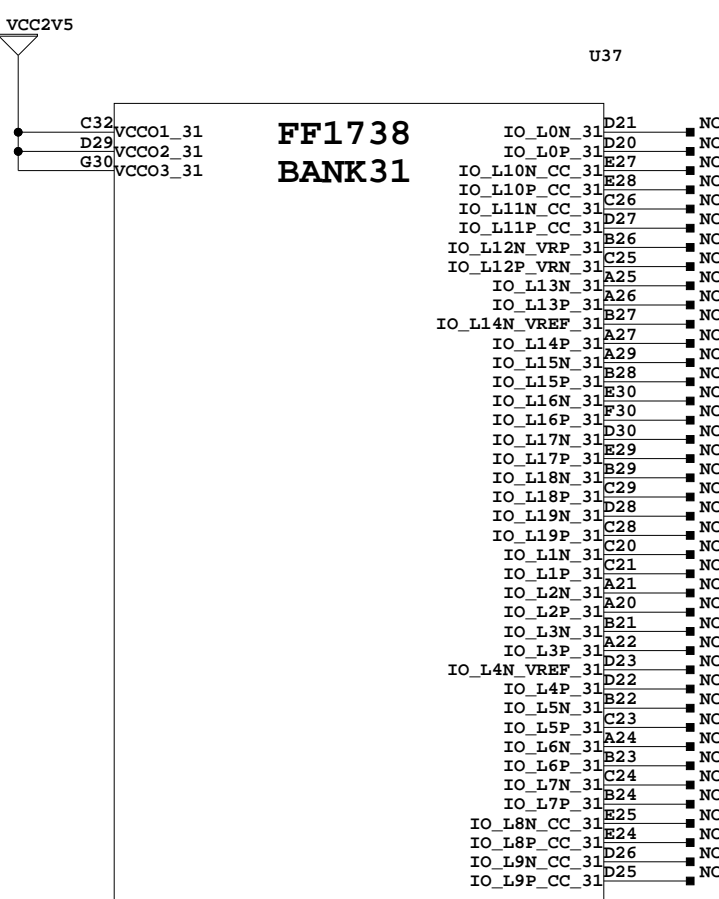
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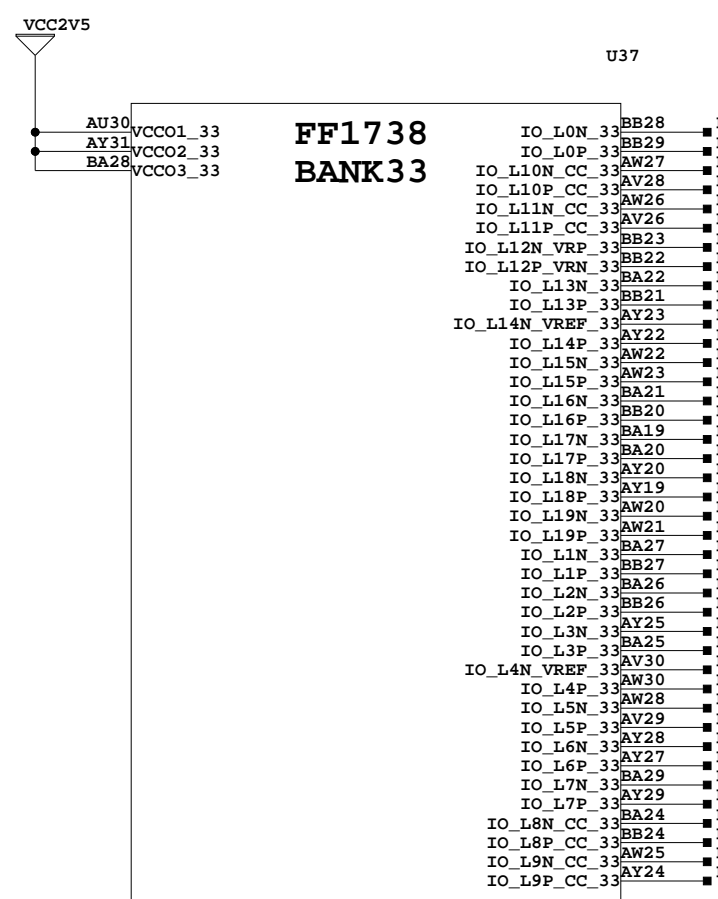
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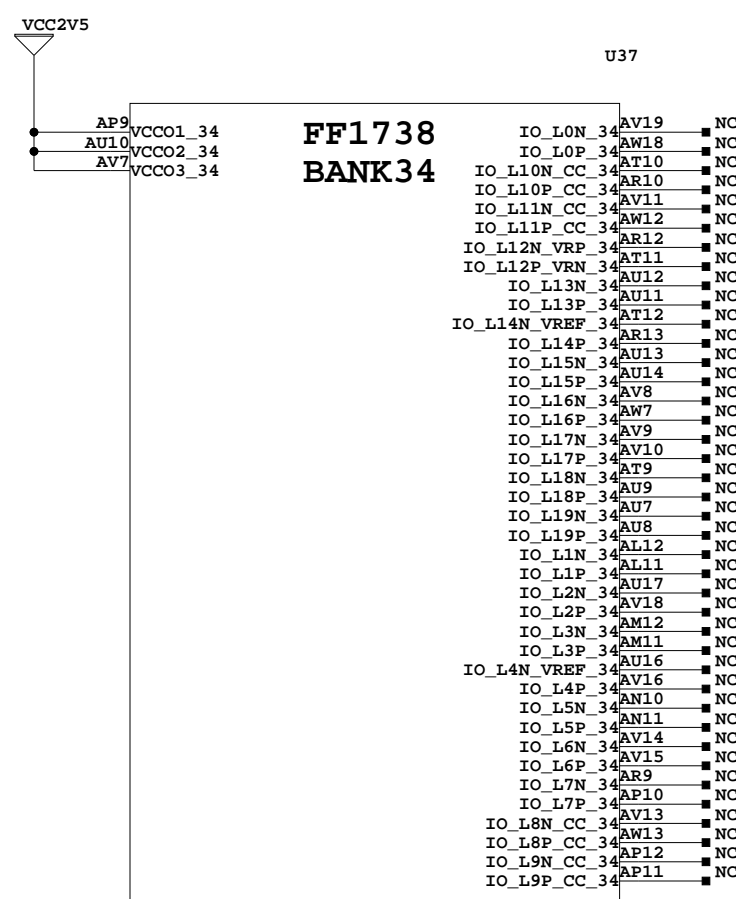
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5VLX330TFF1738



5VLX330TFF1738



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FPGA - BANK 7,8,27,29,31,33,34



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

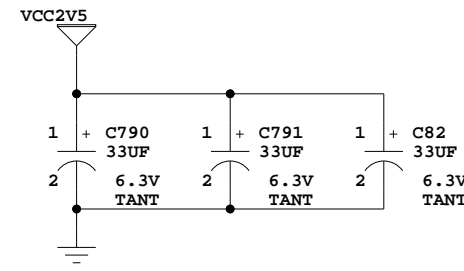
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FPGA - BANK 7,8,27,29,31,33,34 UNUSED BANKS

Date: 7-10-2008_10:19 Ver: C

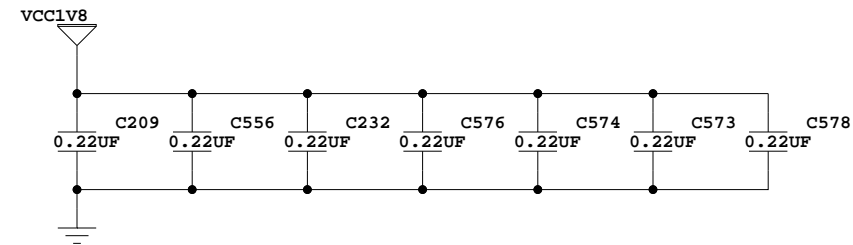
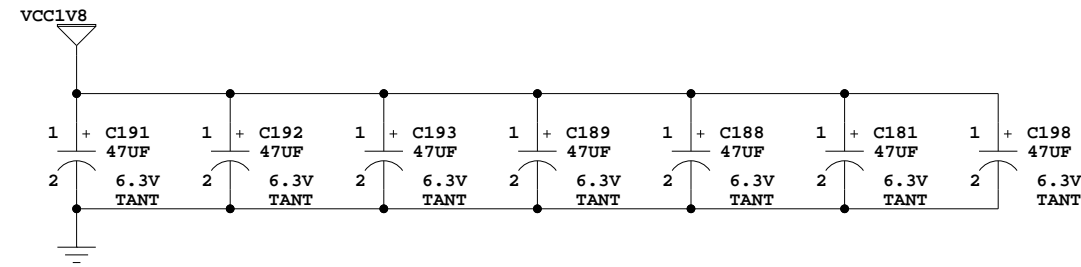
Sheet Size: B Rev: 01

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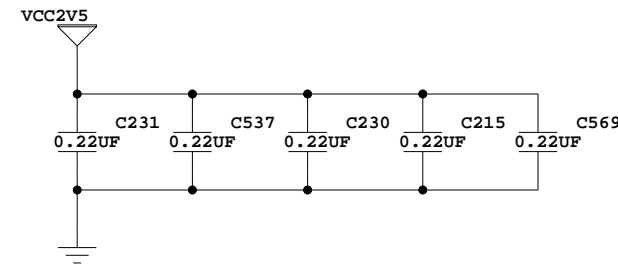
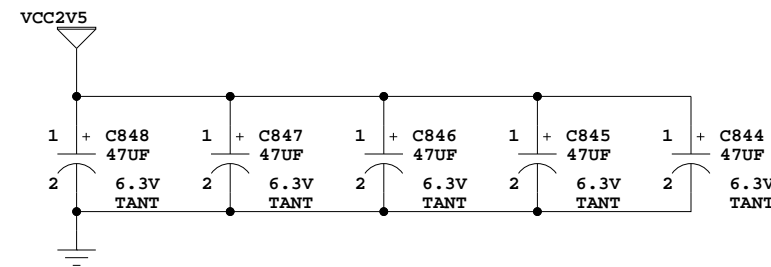
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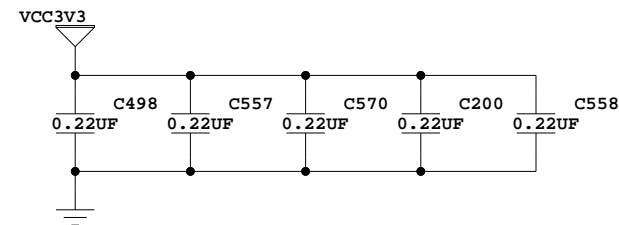
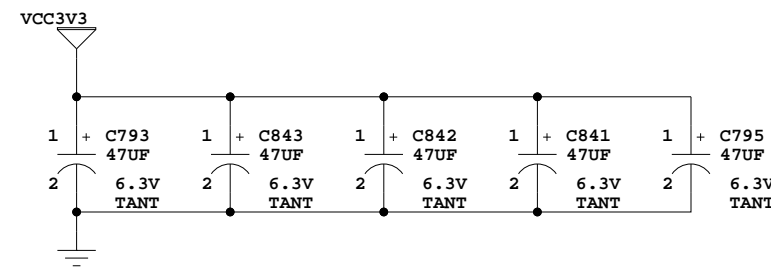
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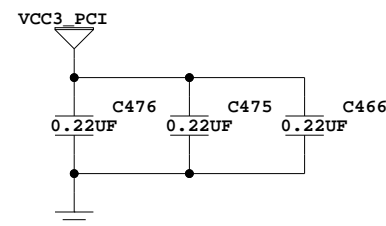
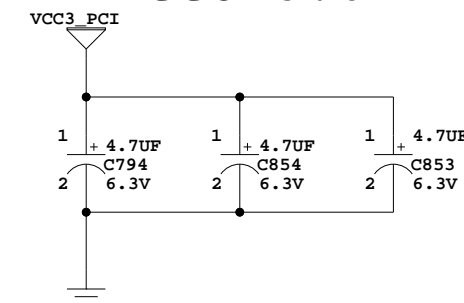
VCCO 2.5V



VCCO 3.3V



VCCO 3.0V PCI



Supply	Banks Used	Capacitors Used
VCCAUX 2.5V	N/A	33uf: 3
VCCINT 1.0V	N/A	330uf: 7 / 0.22uf: 52
VCCO 3.3V	0,1,2,4,26	47uf: 5 / 0.22uf: 5
VCCO 2.5V	3,5,6,18,25	47uf: 5 / 0.22uf: 5
VCCO 1.8V	11,13,15,17,19,21,23	47uf: 7 / 0.22uf: 7
VCCO 3.0V PCI	12,20,24	47uf: 3 / 0.22uf: 3

Note: Bank 12 defaults to 3.0V_PCI

FPGA DECOUPLING

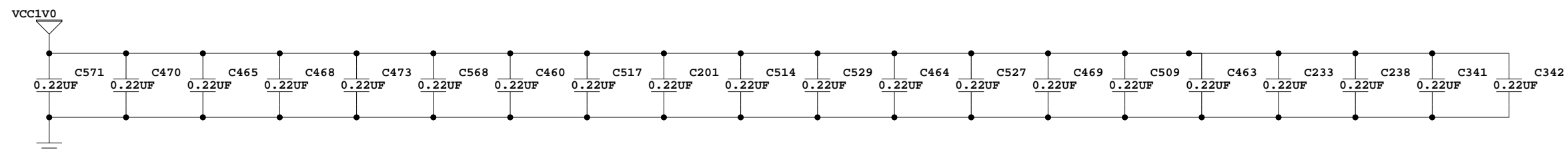
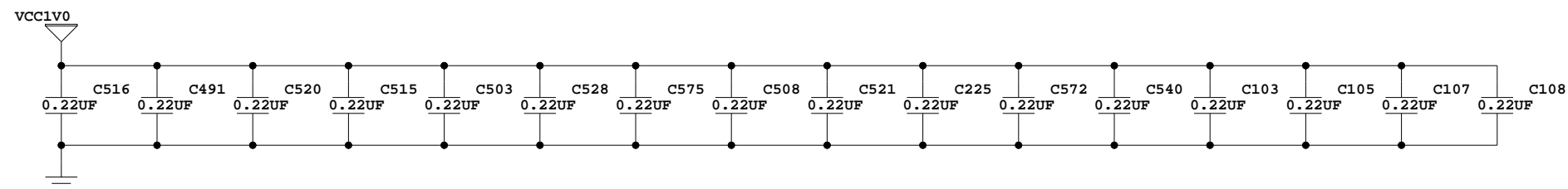
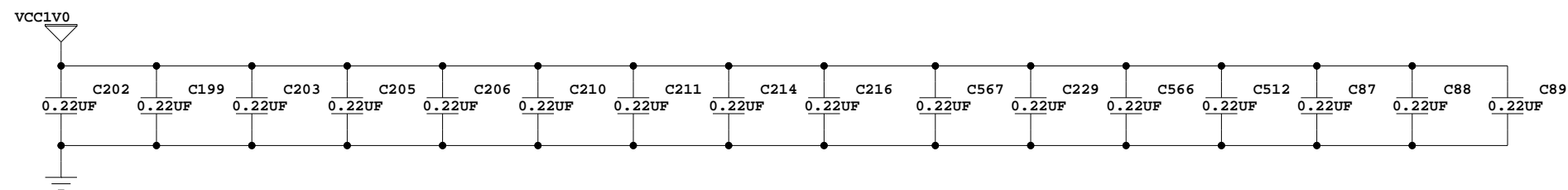
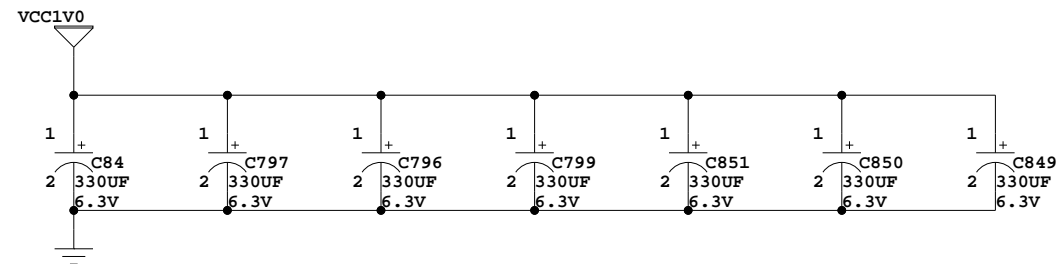


SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFORM
FPGA DECOUPLING

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VCCINT 1.0V



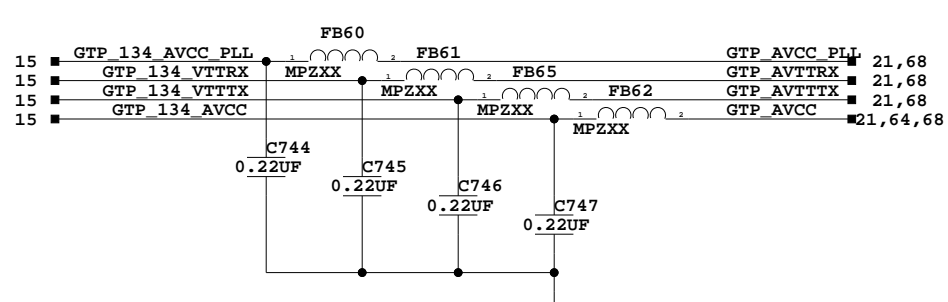
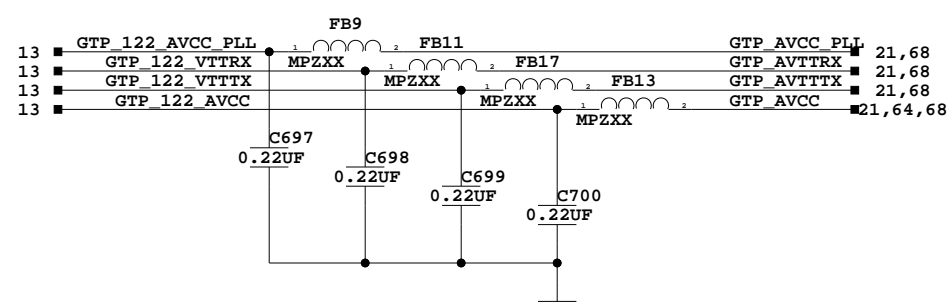
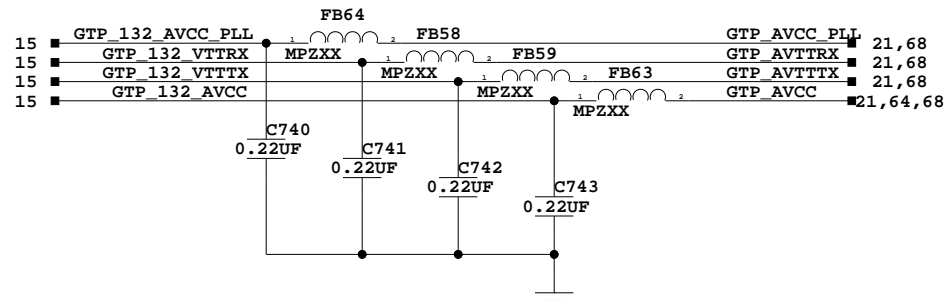
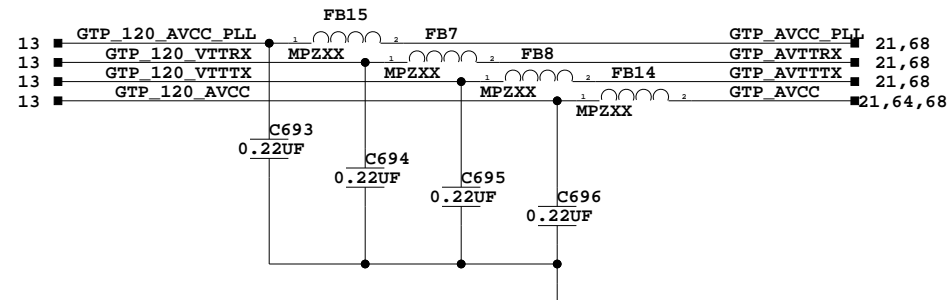
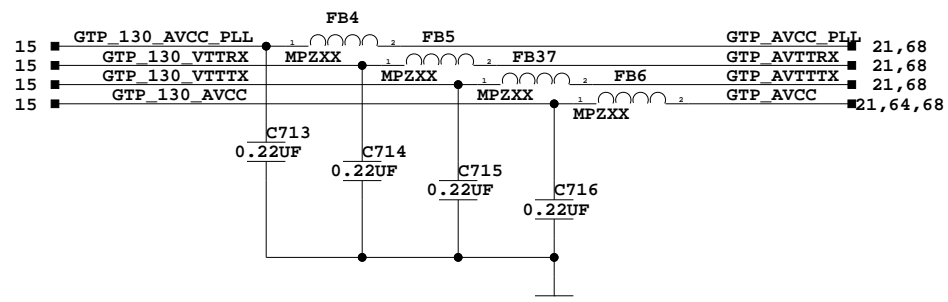
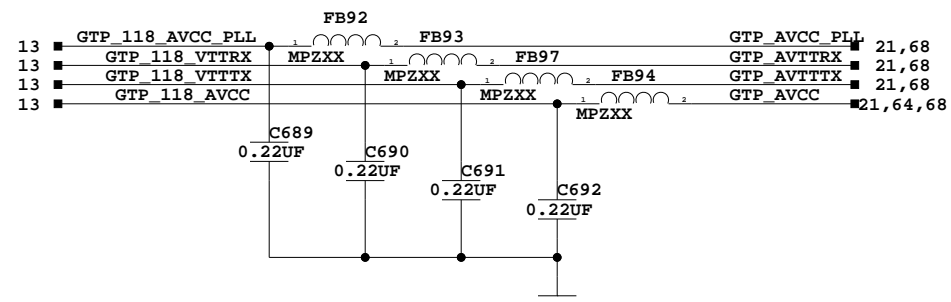
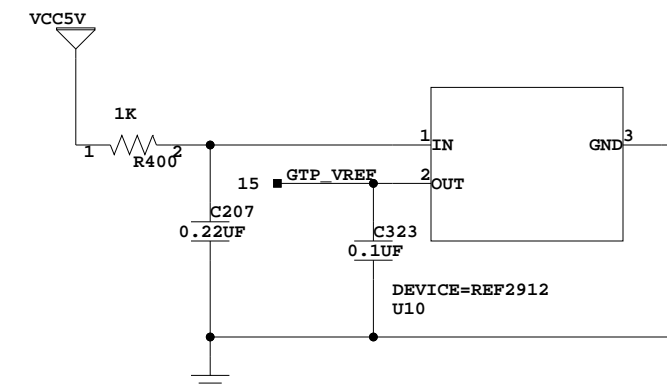
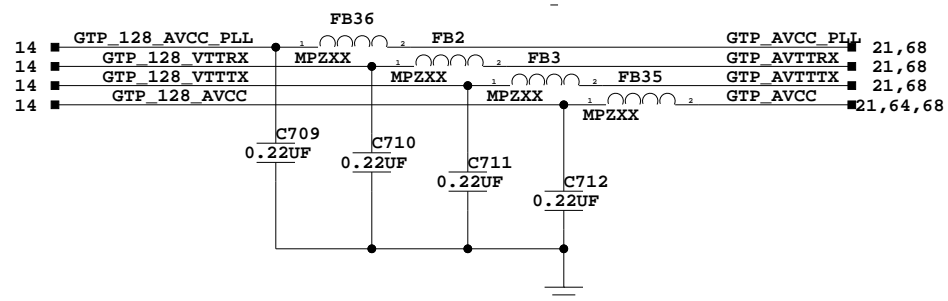
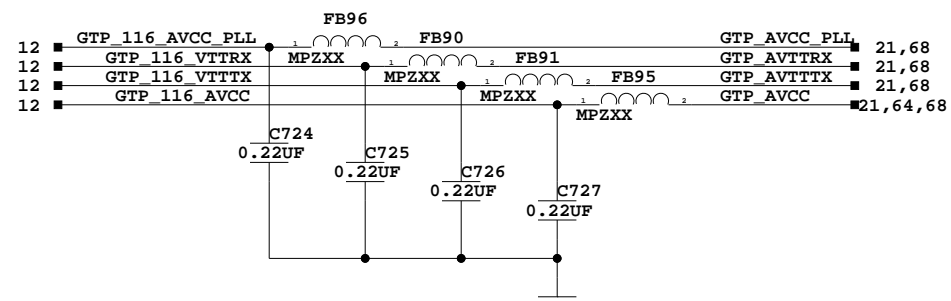
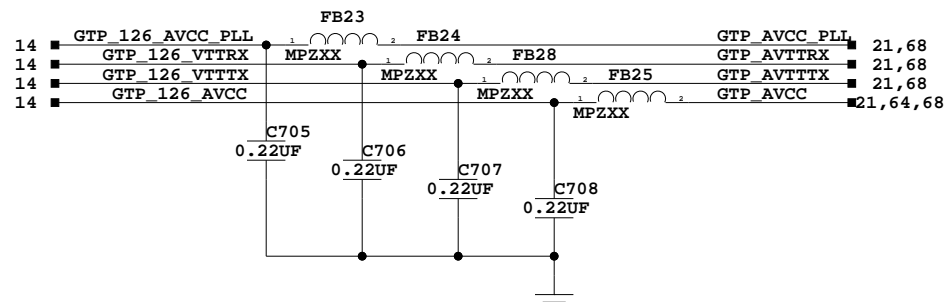
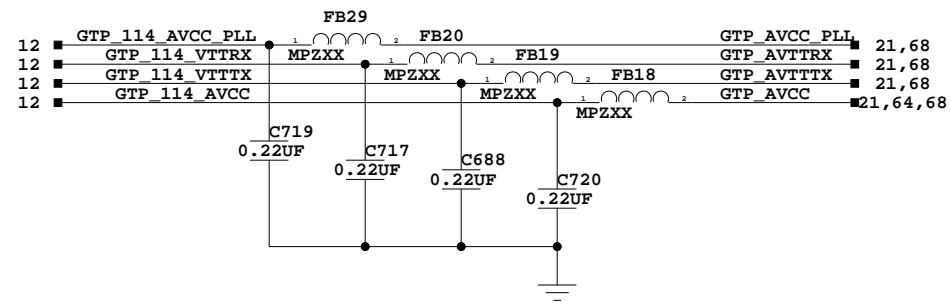
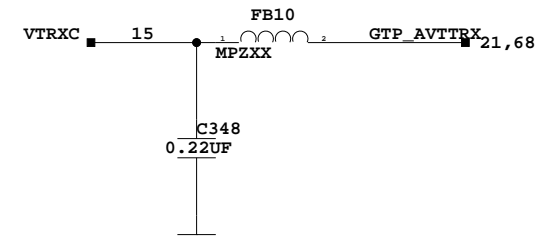
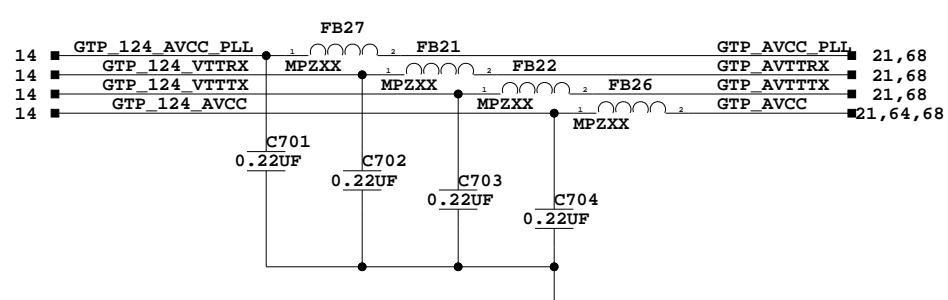
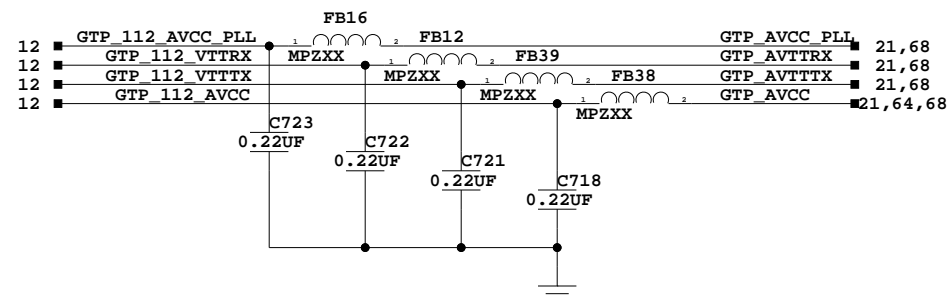
FPGA DECOUPLING PAGE 2



SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 FPGA DECOUPLING PAGE 2

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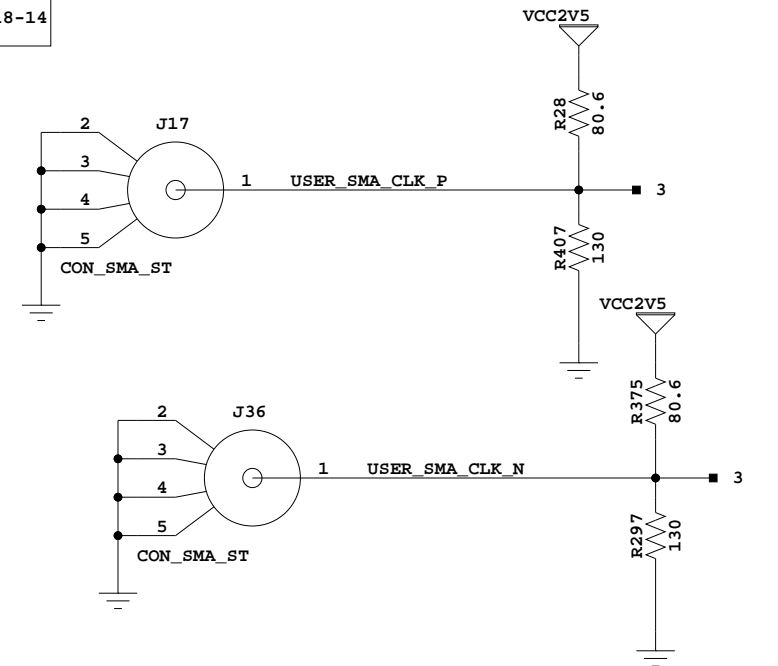
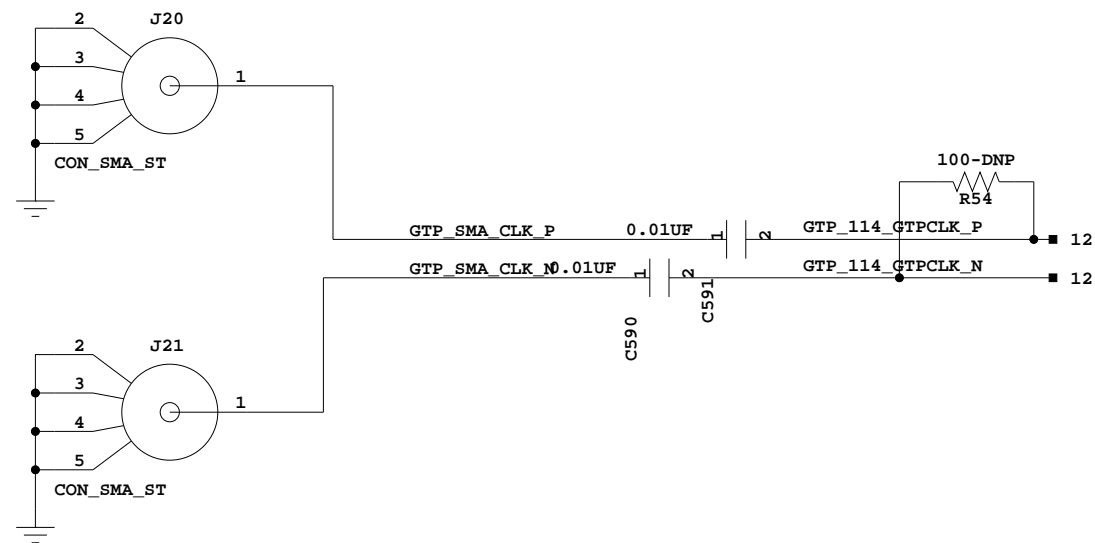
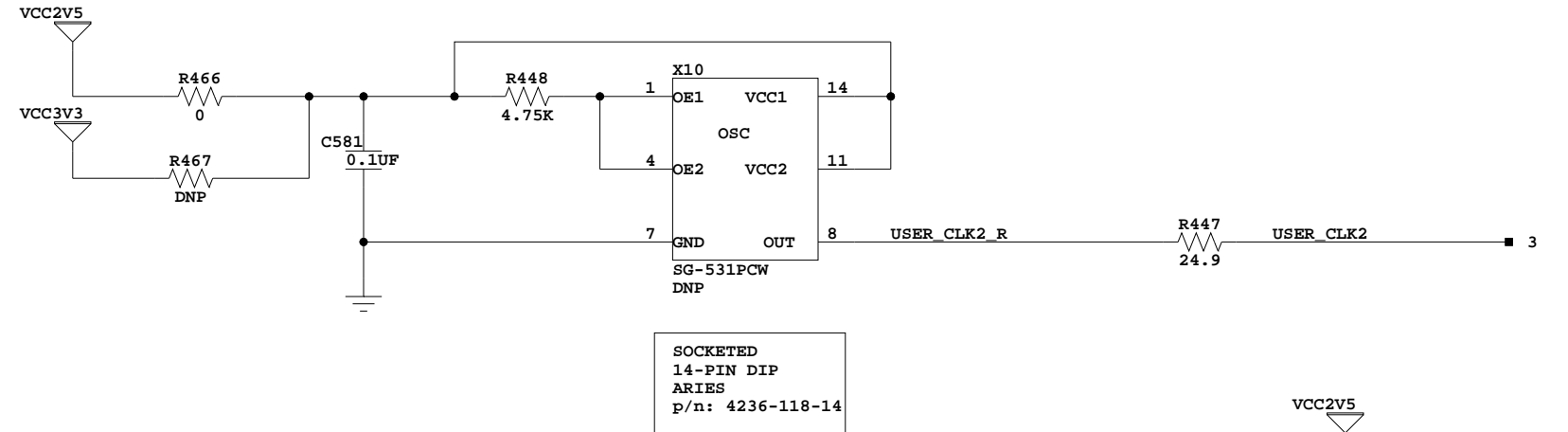
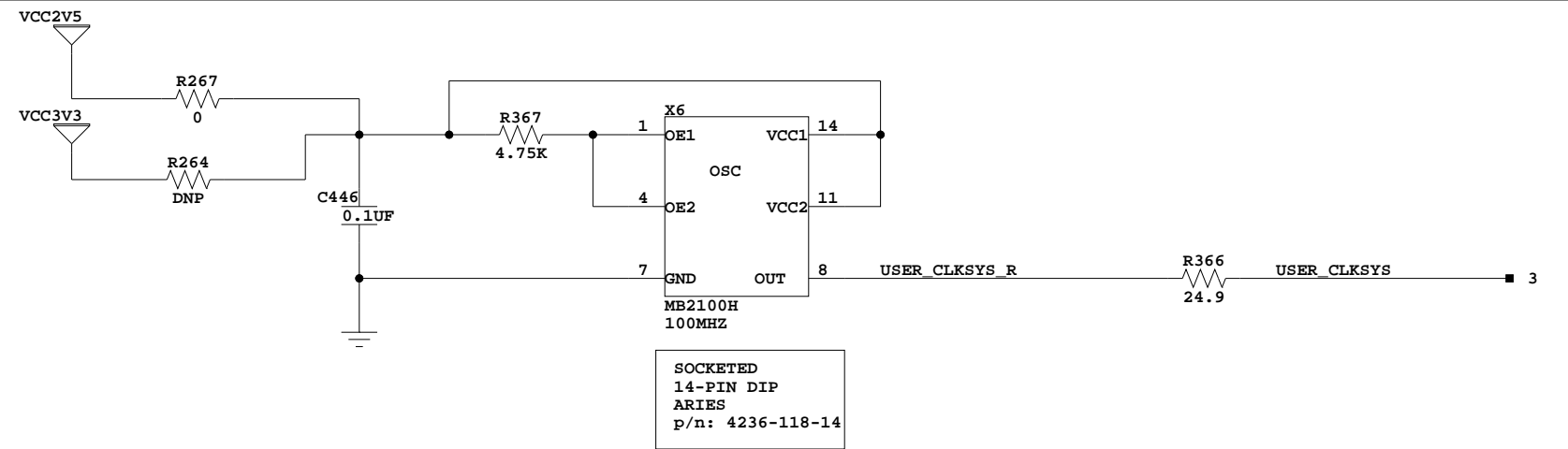
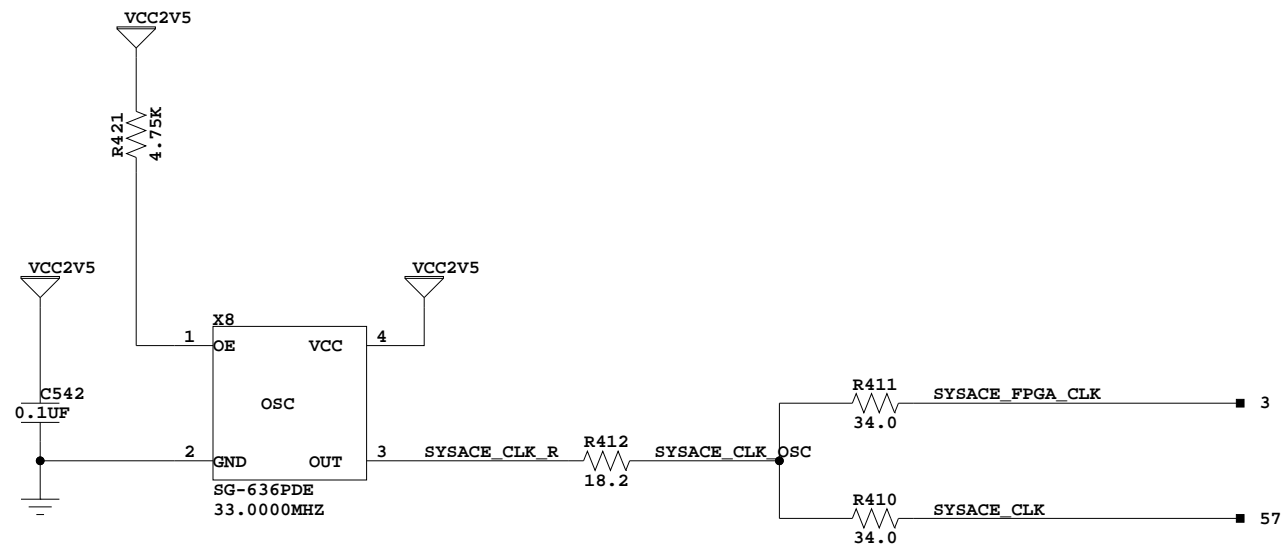
GTP POWER FILTER



SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 GTP POWER FILTER

Date:	7-10-2008_10:19	Ver:	C
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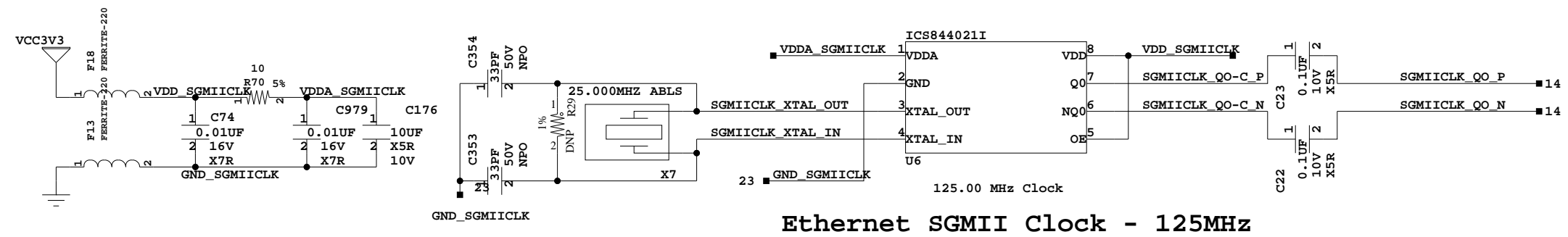
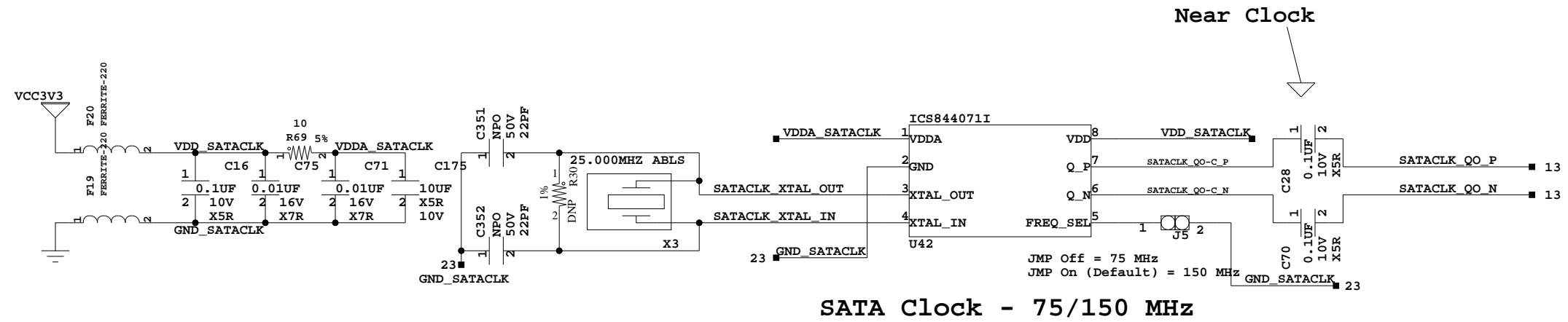
CLOCKS: USER, MGT, SYSACE



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
CLKS: USR, MGT, SYSACE

Date:	7-10-2008_10:19	Ver:	C
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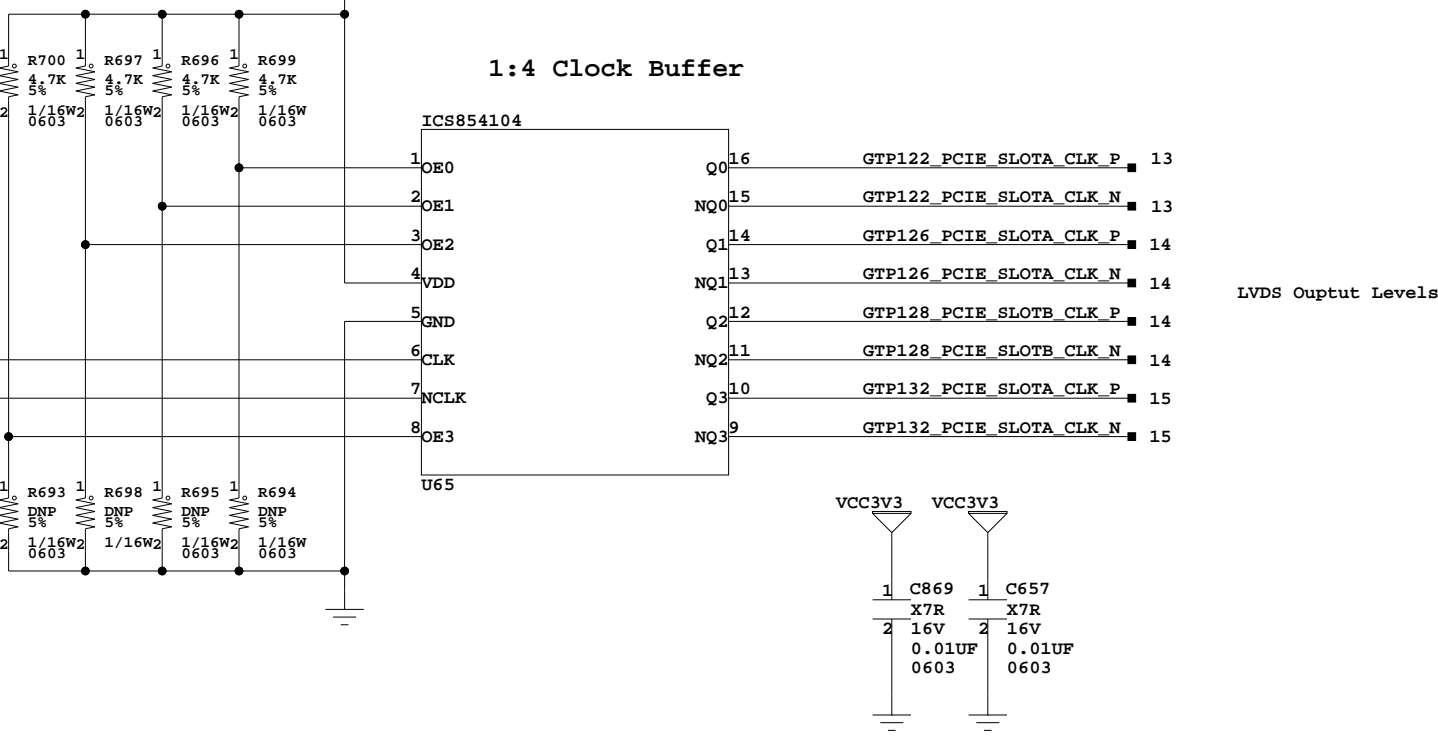
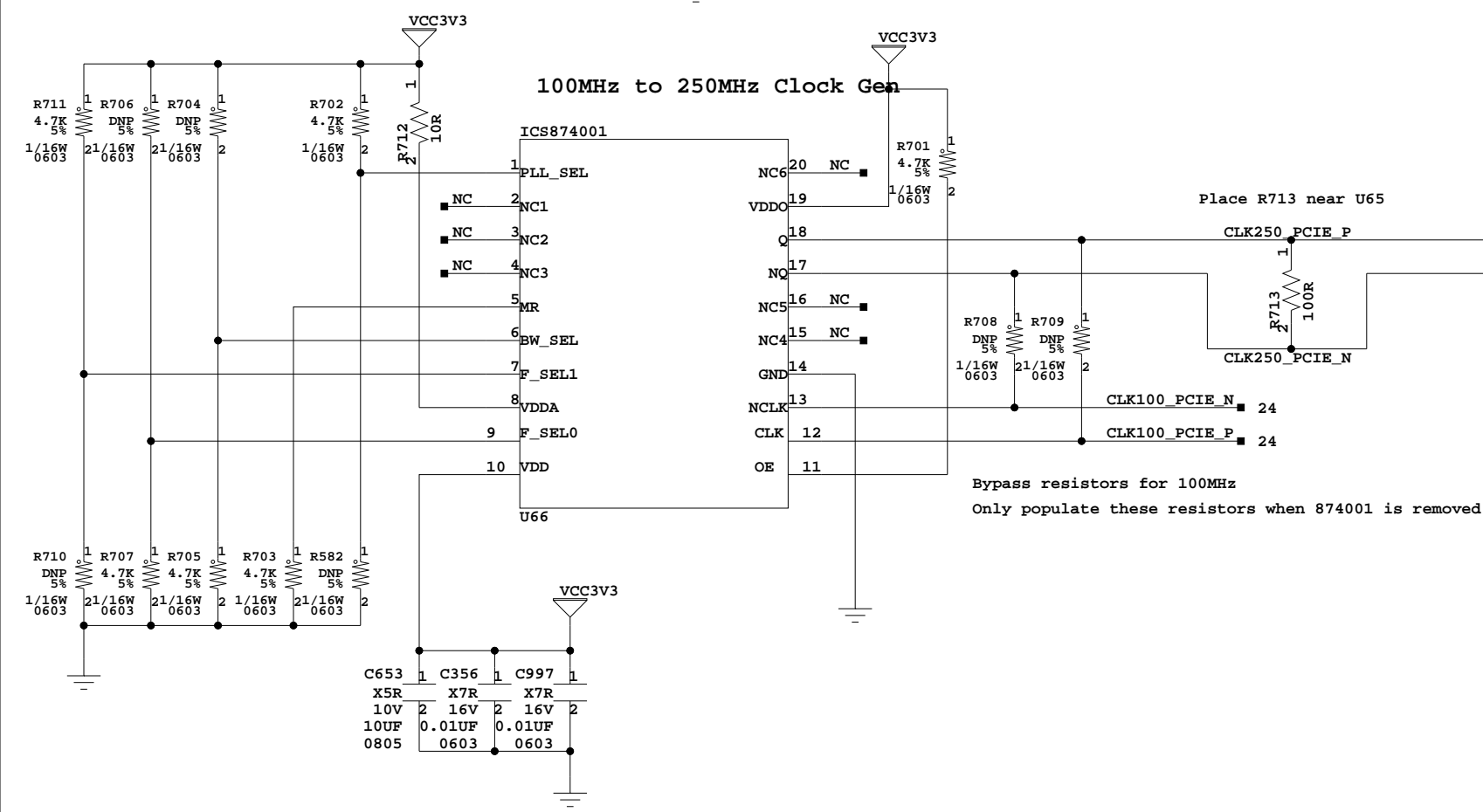
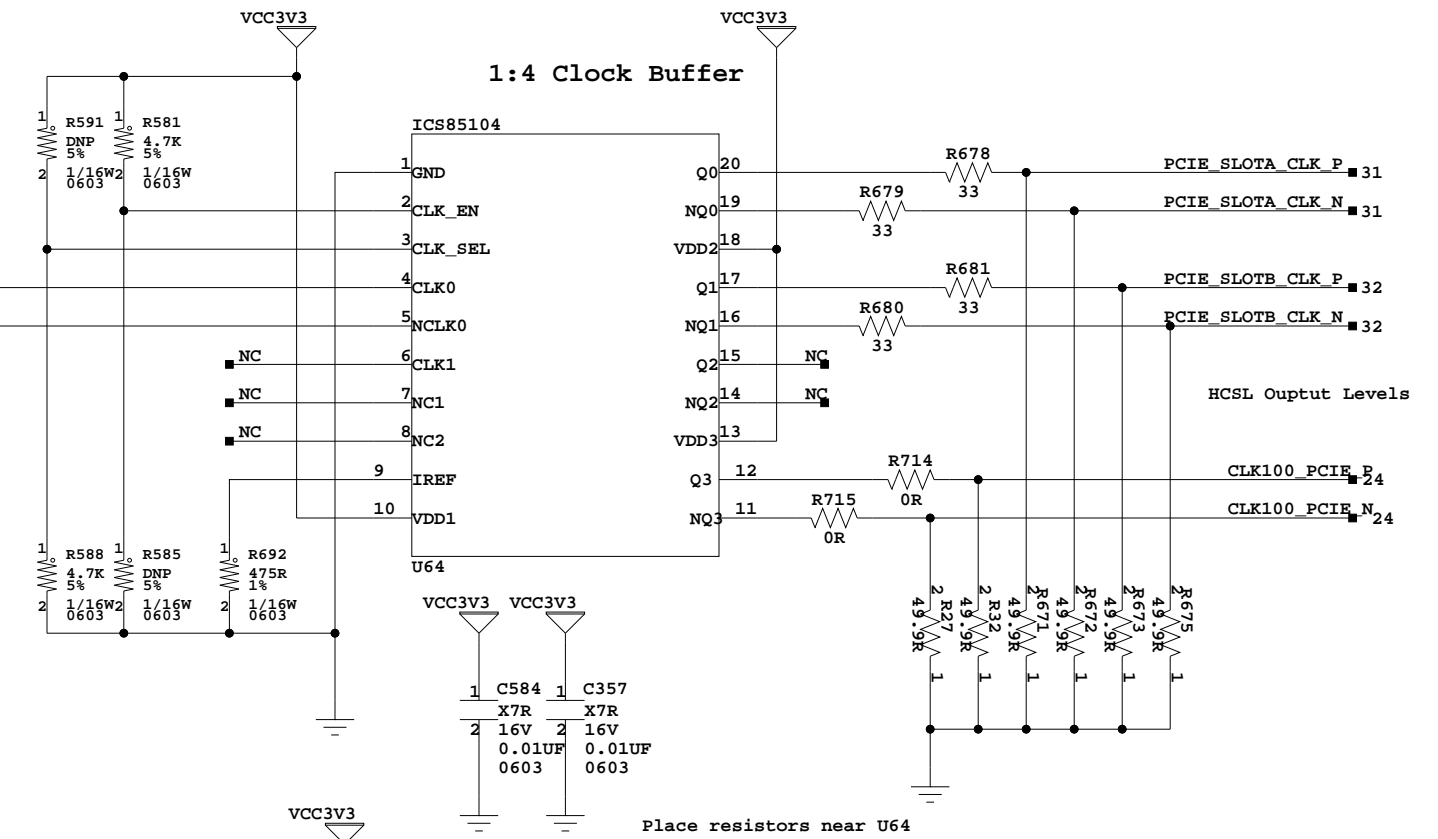
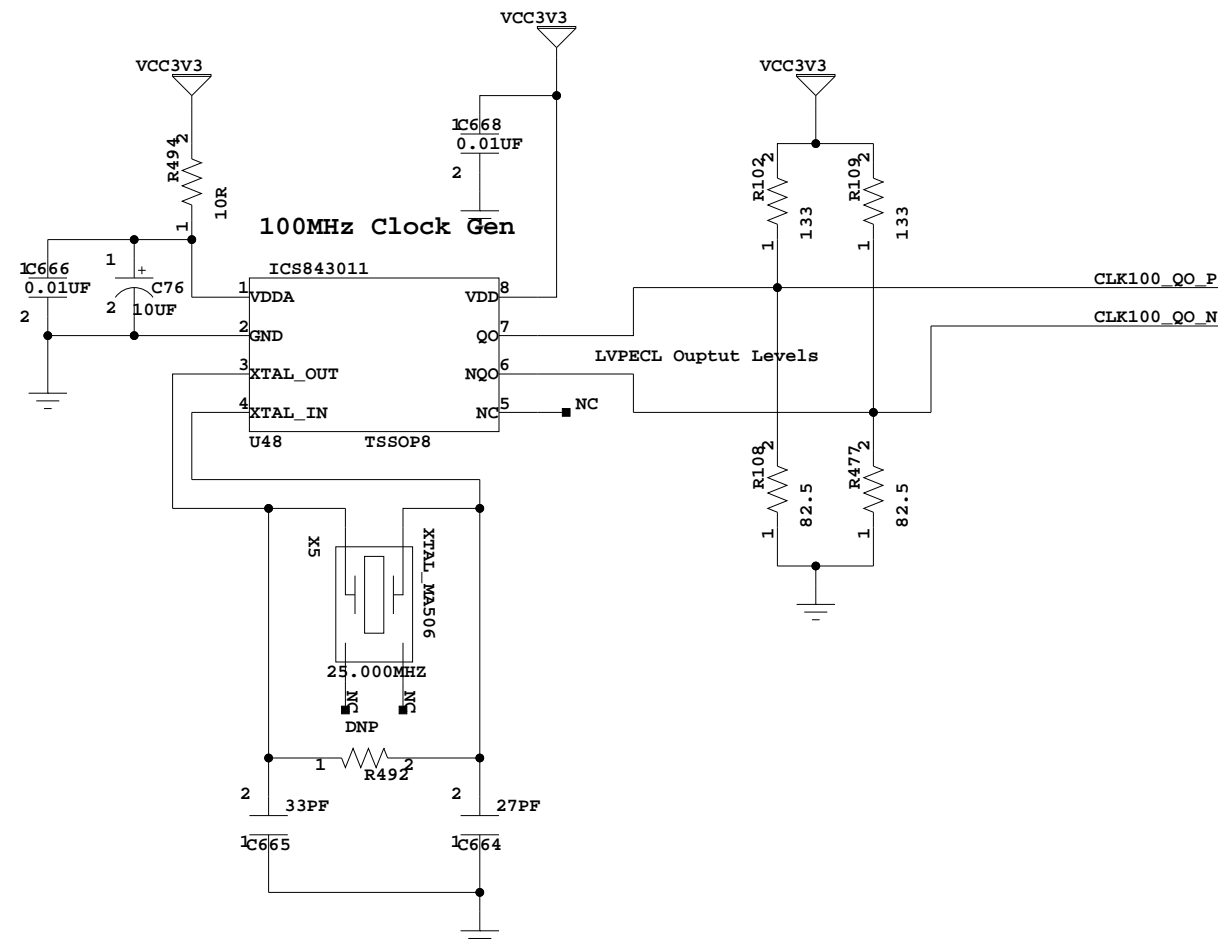


SATA, SGMII CLOCKS

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
SATA, SGMII CLOCKS

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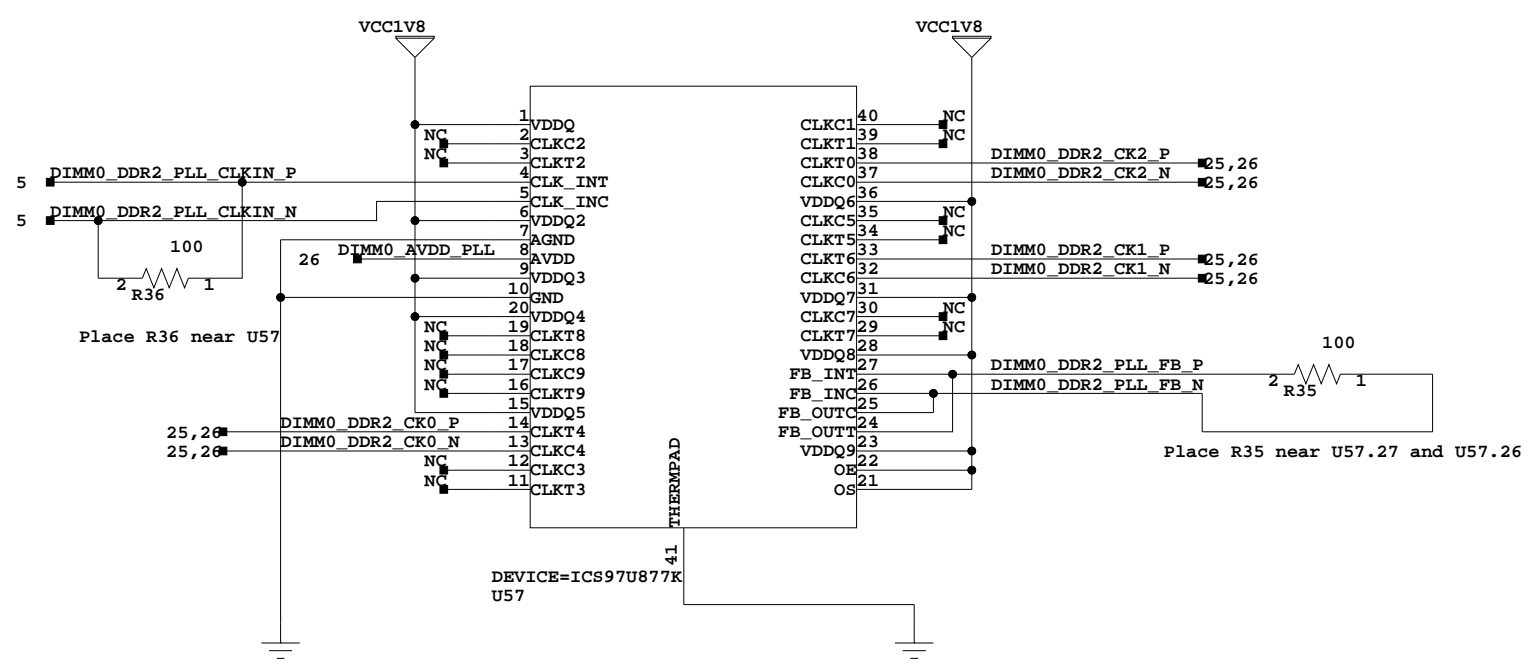
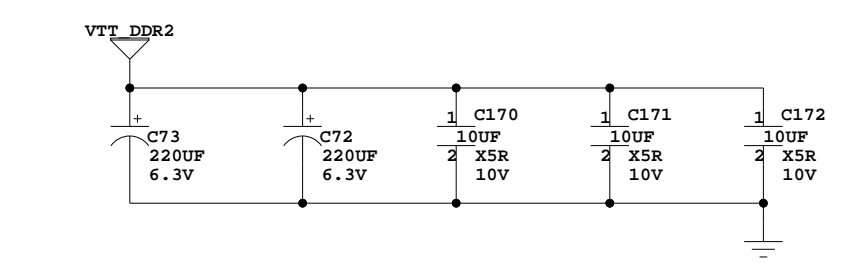
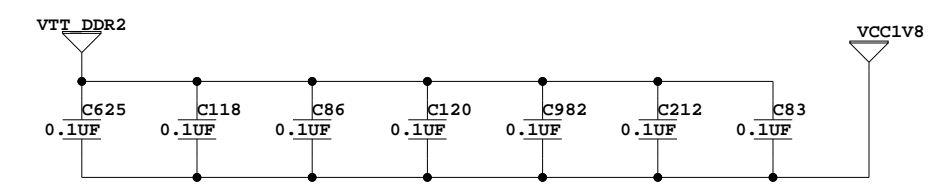
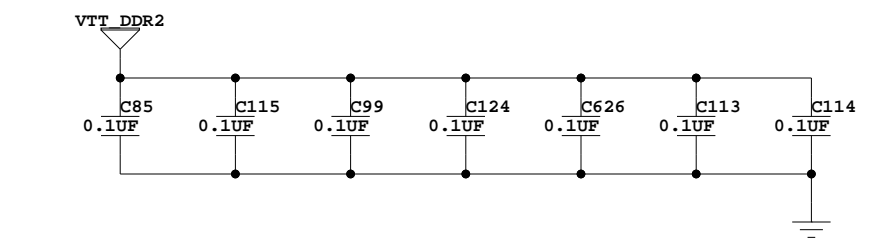
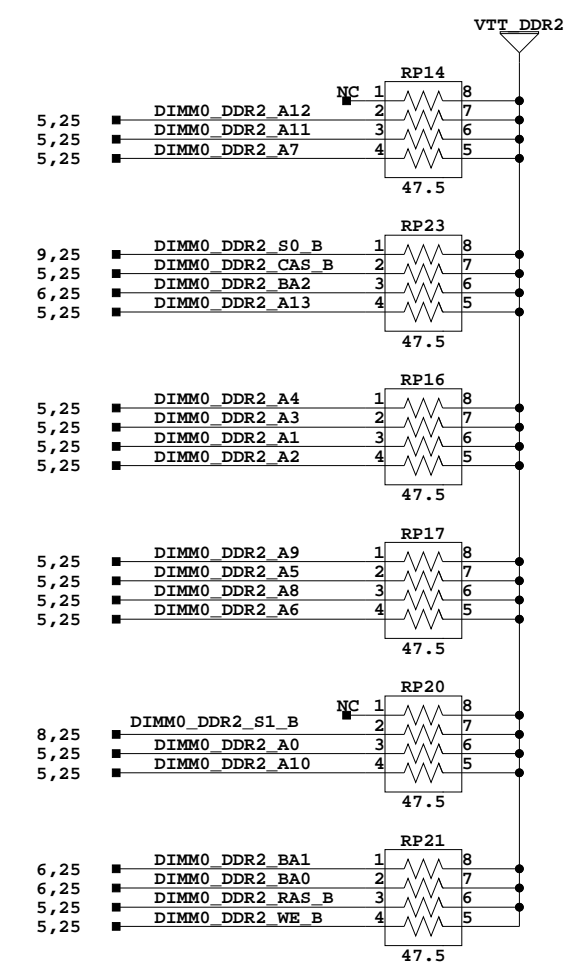
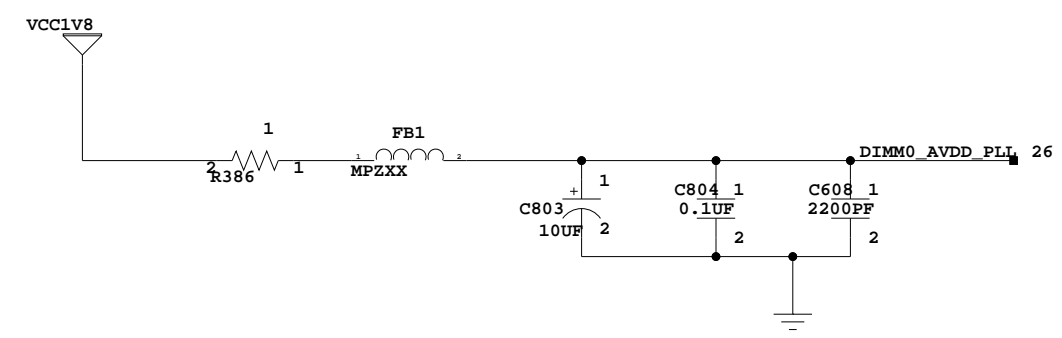
PCie CLOCKS

SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

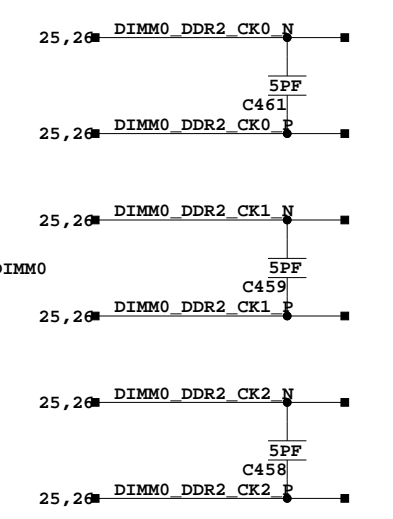
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
PCIE CLOCKS

Date: 7-10-2008_10:19 Ver: C
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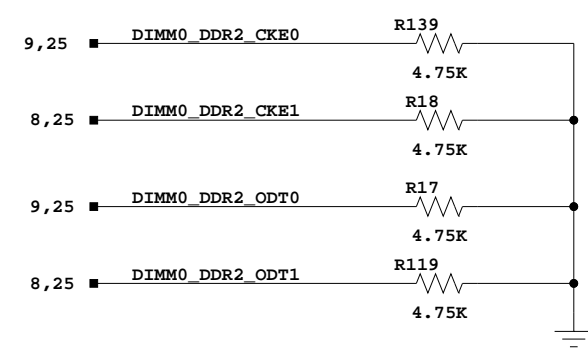
Since this is a source-sink power supply, split of decoupling capacitors between VTT-GND and VTT-VCC1V8



DIMM0_DDR2_PLL_FB* to be length matched to DIMM0_DDR2_CLKIN_*



Place these 5pf caps near DDR2 DIMM0



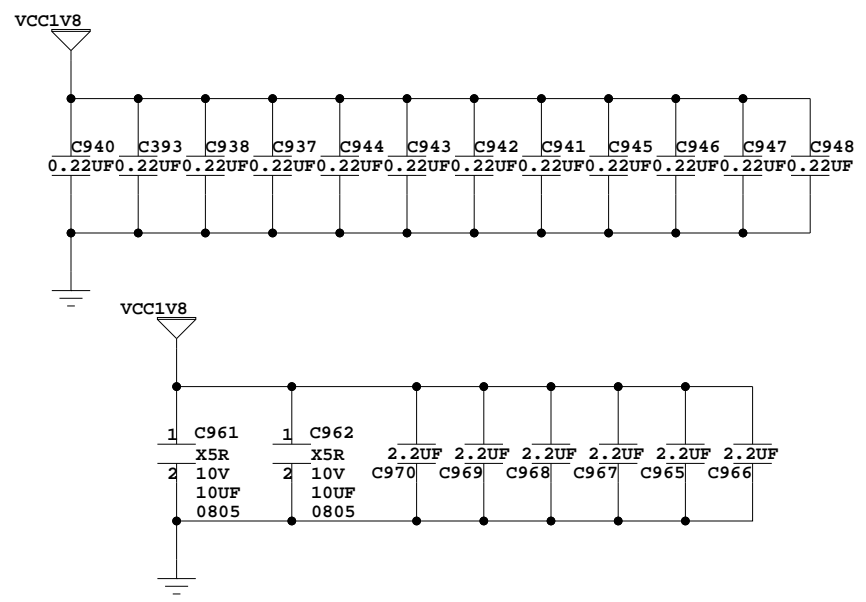
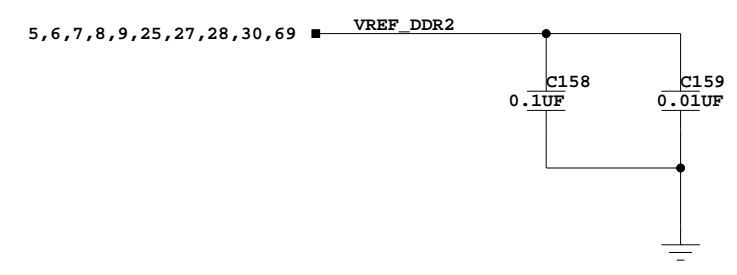
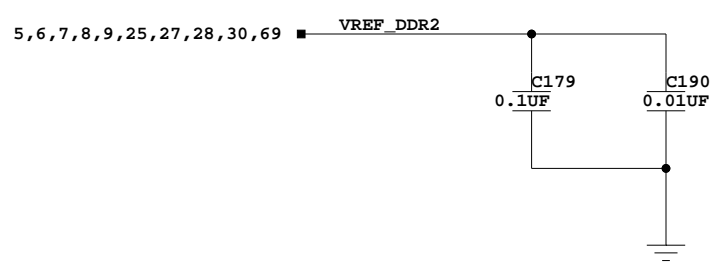
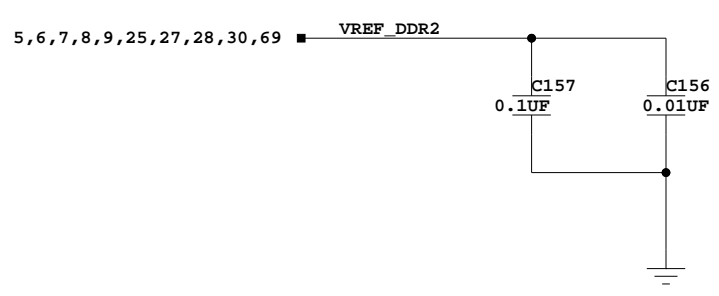
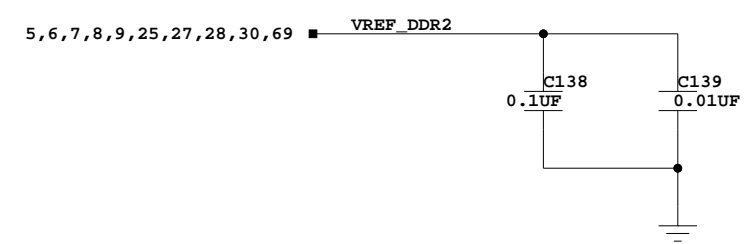
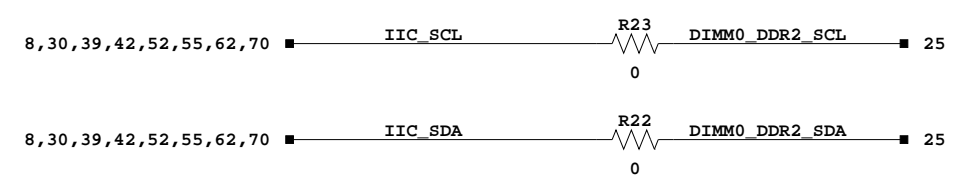
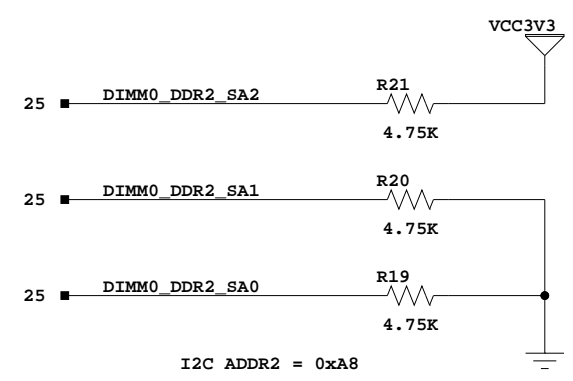
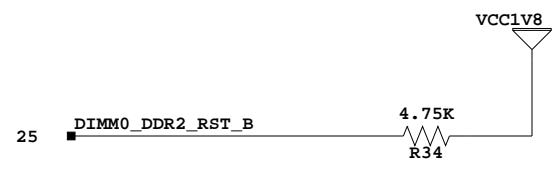
DIMM0 DDR2 SSTL-2 TERMINATION



SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 DIMM0 DDR2 SSTL-2 TERMINATION

Date:	7-10-2008_10:19	Ver:	C
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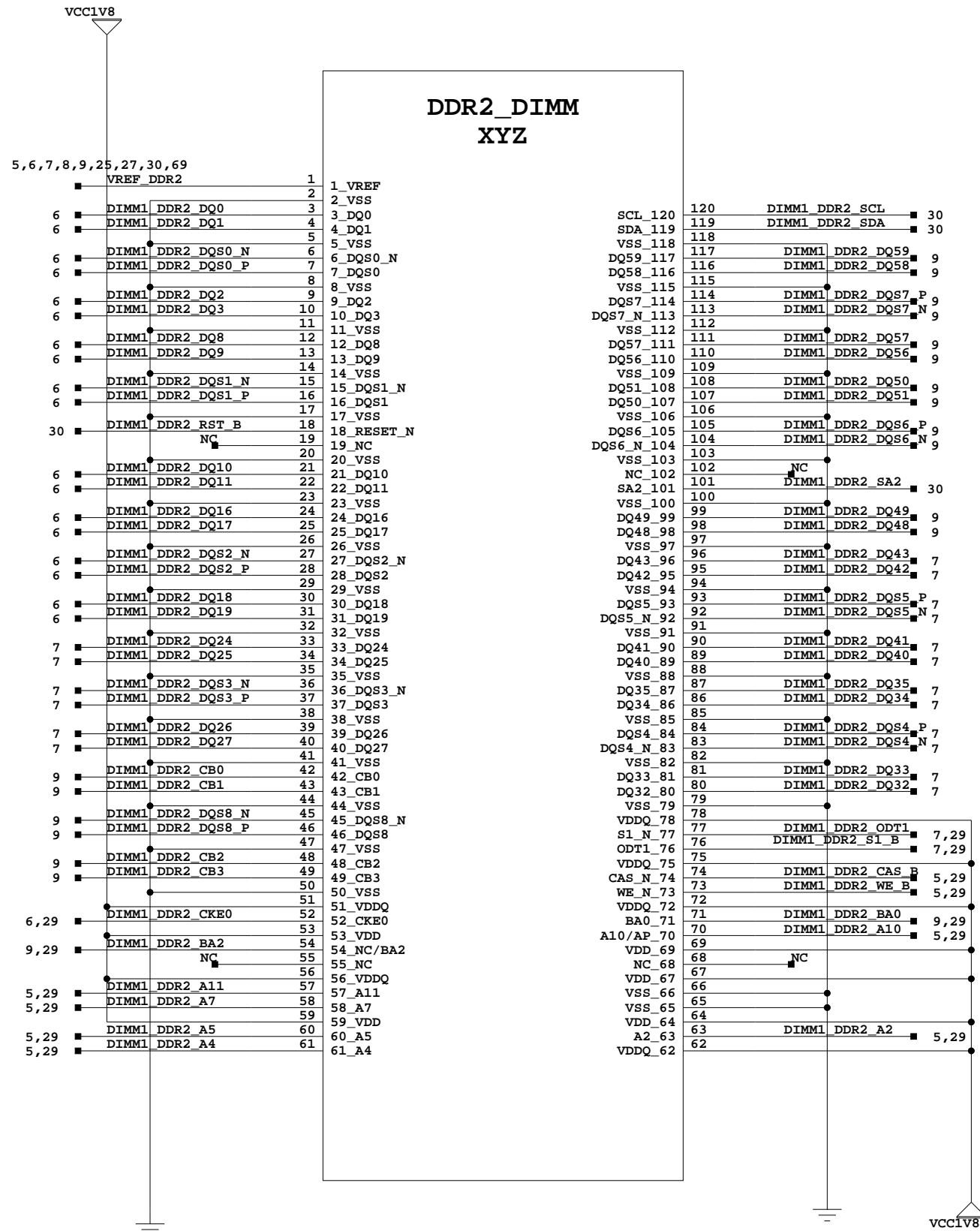


DIMM0 DDR2 DECOUPLING

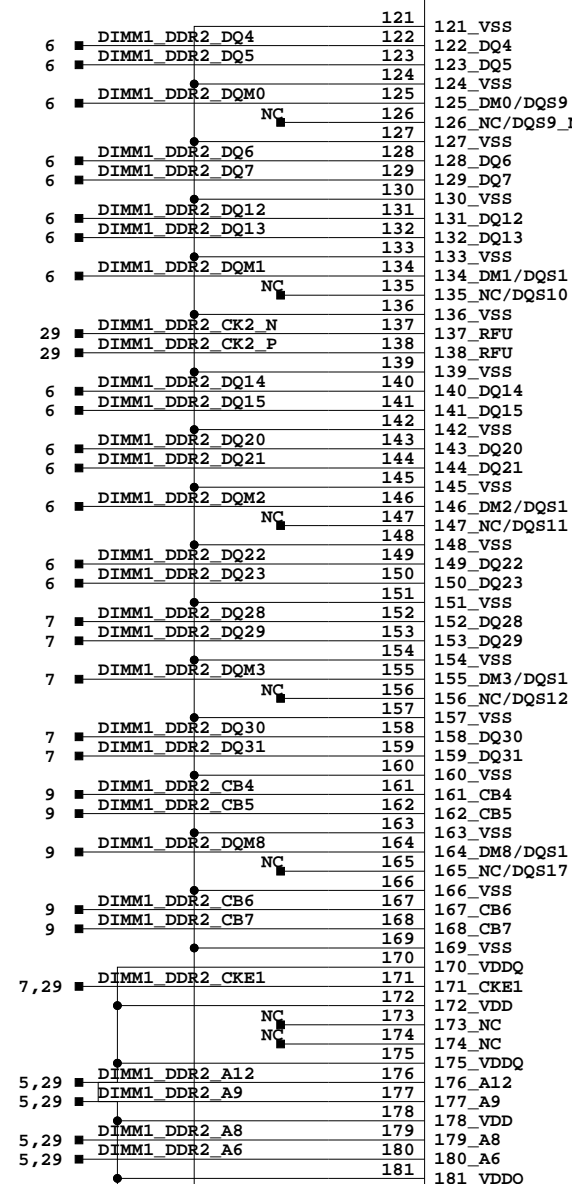
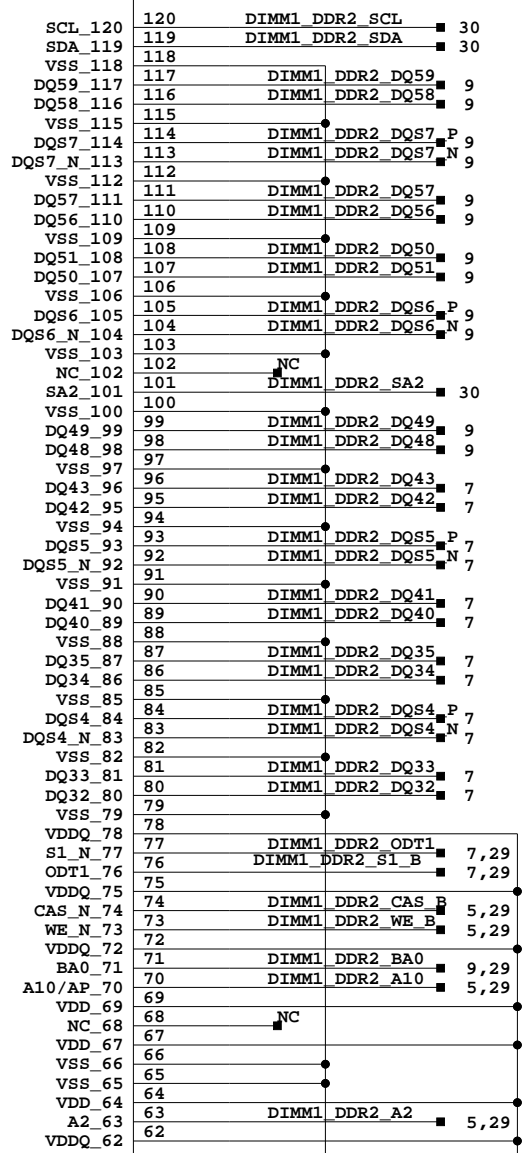


SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM DIMM0 DDR2 DECOUPLING	
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P9
 DEVICE=DDR2_DIMM
 PKG_TYPE=CON-240-DDRAM
 PARTS=1
 LEVEL=STD



P9
 DEVICE=DDR2_DIMM
 PKG_TYPE=CON-240-DDRAM
 PARTS=1
 LEVEL=STD

I2C ADDR = 0xA6

DDR2_DIMM XYZ

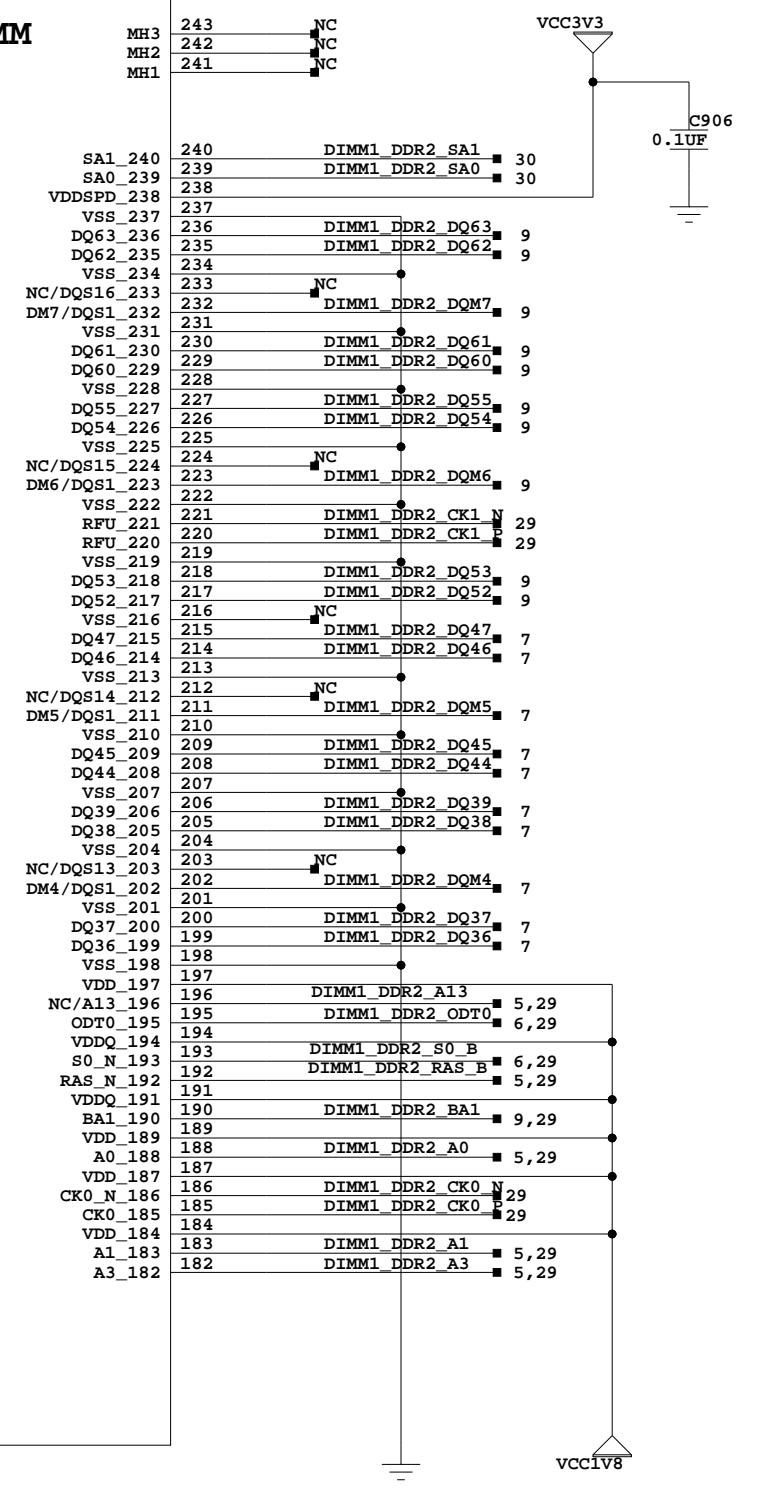
DDR2 DIMM1 CONNECTOR



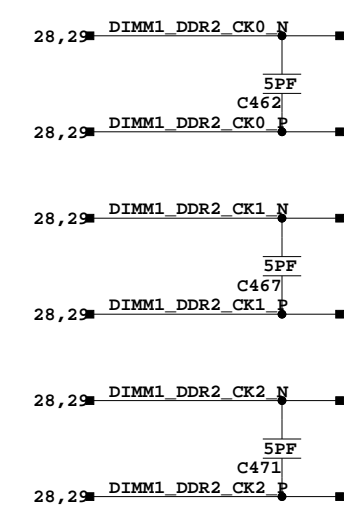
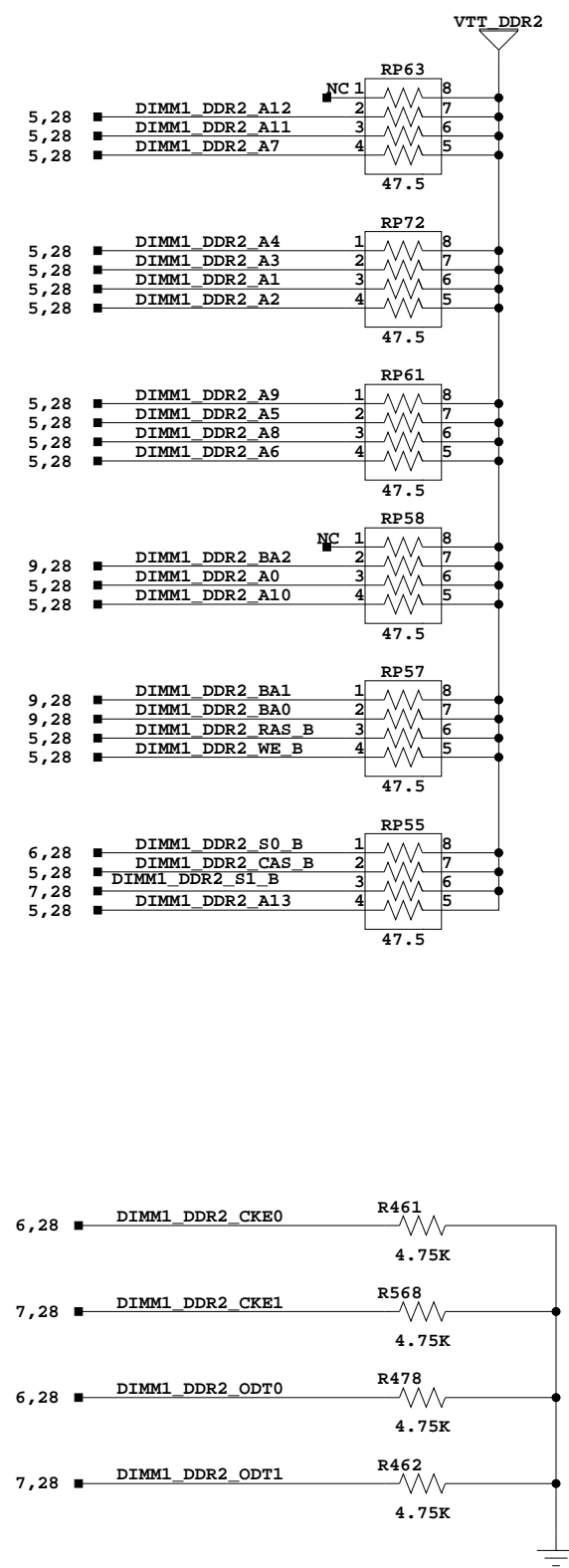
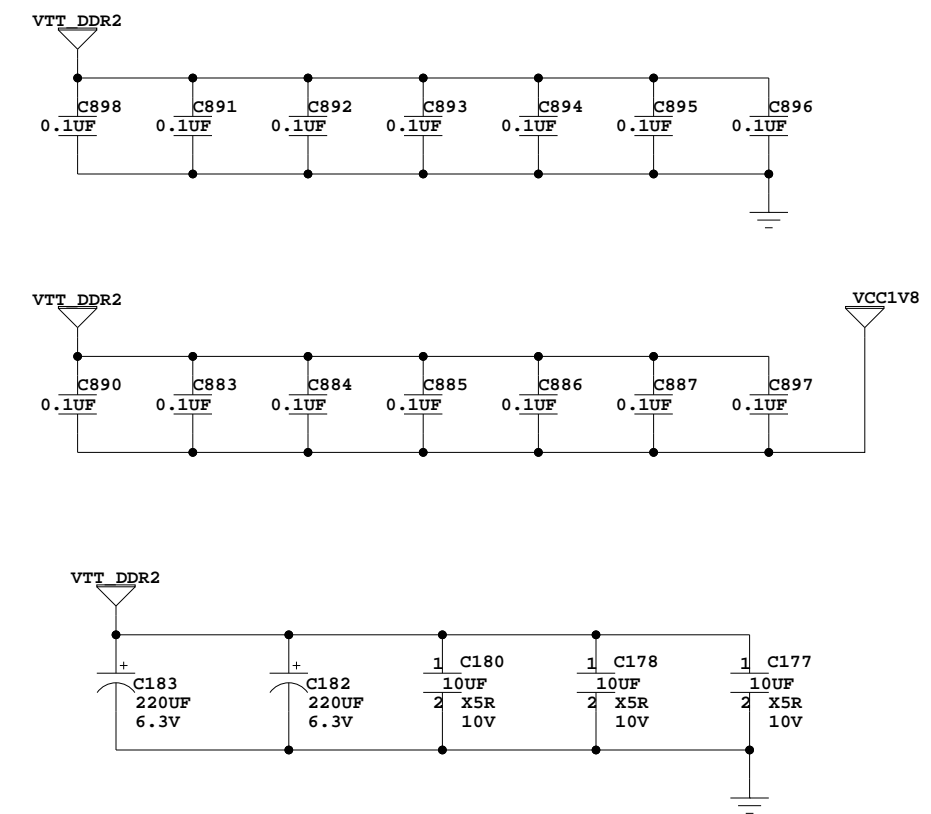
SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 DDR2 DIMM2 CONNECTOR

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Since this is a source-sink power supply, split of decoupling capacitors between VTT-GND and VTT-VCC1V8



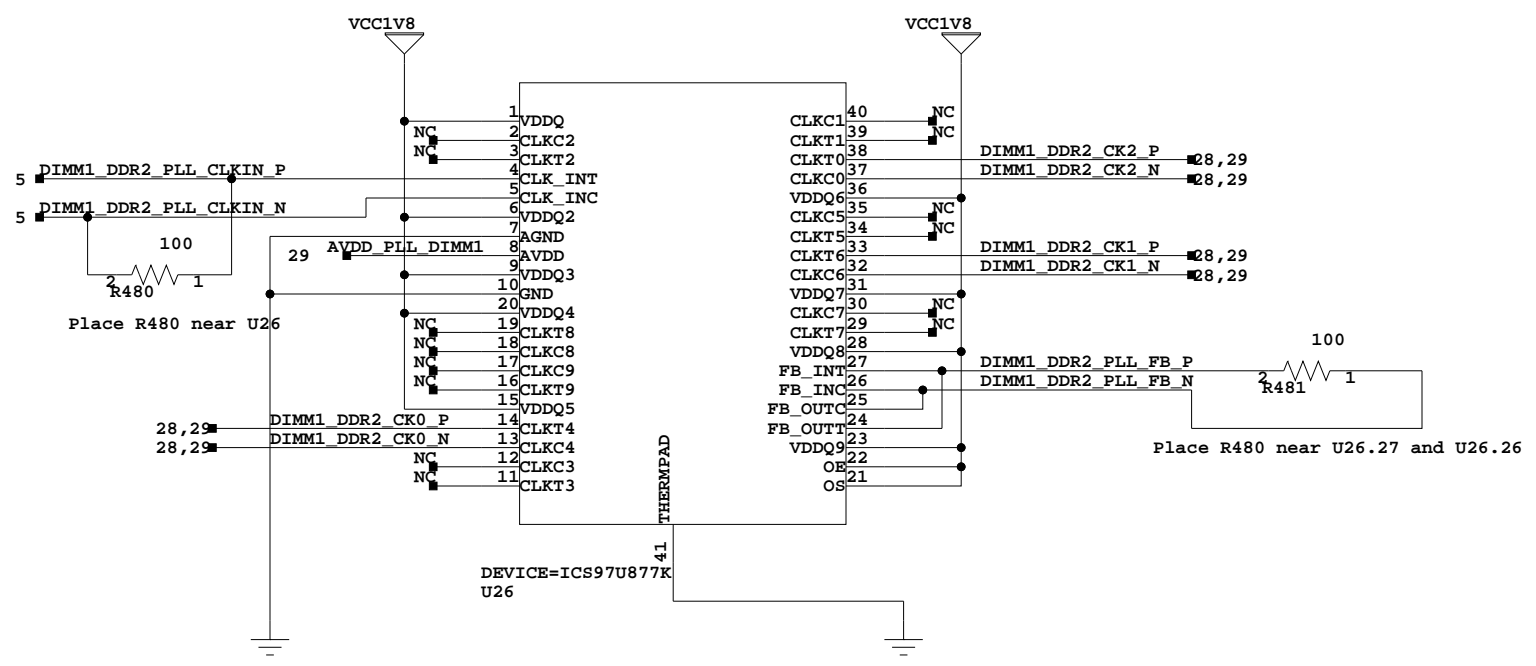
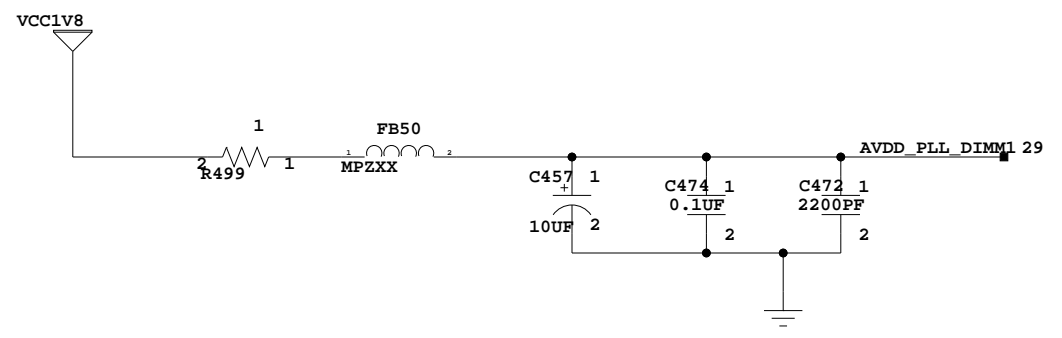
DIMM1 DDR2 SSTL-2 TERMINATION

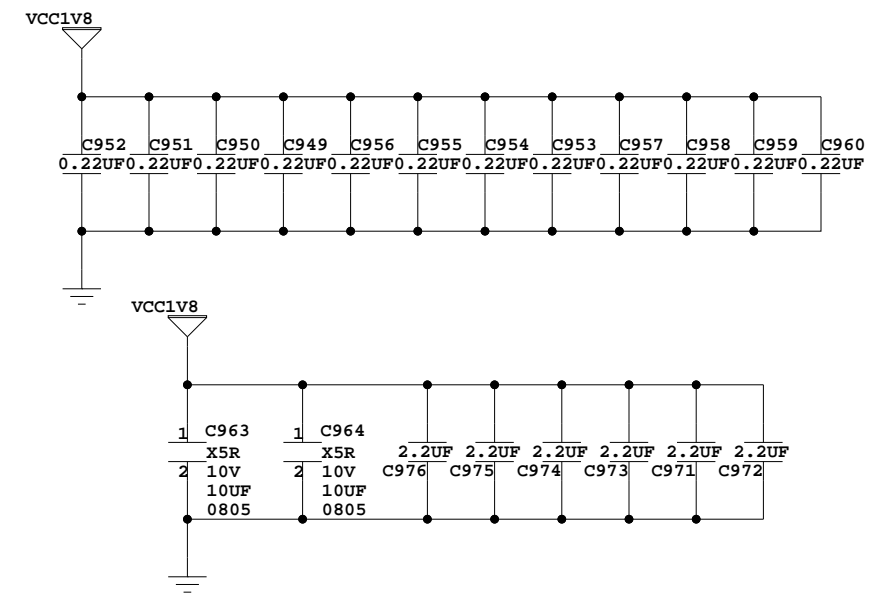
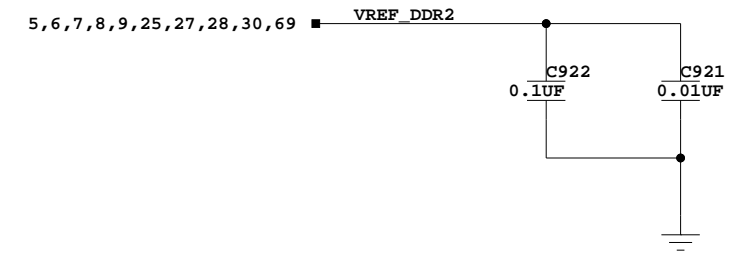
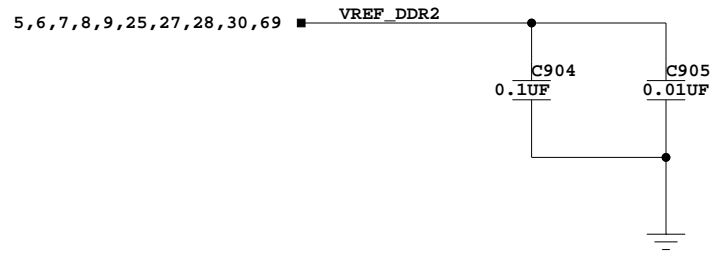
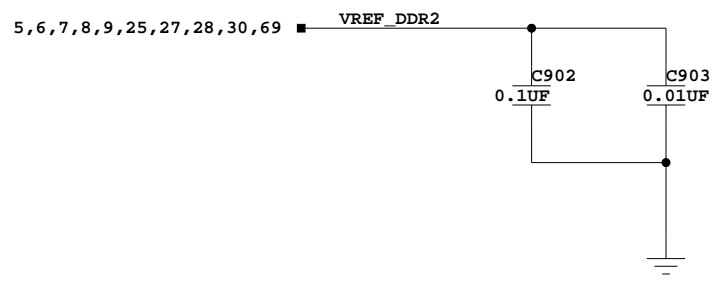
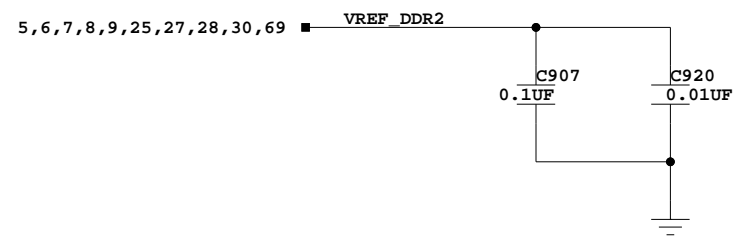
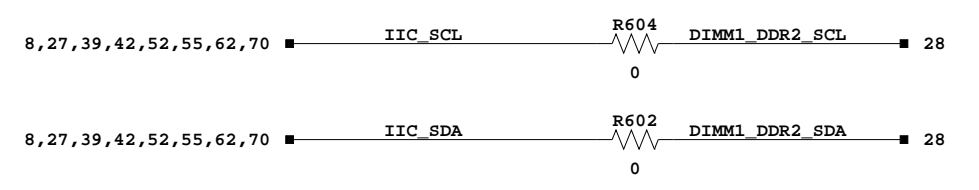
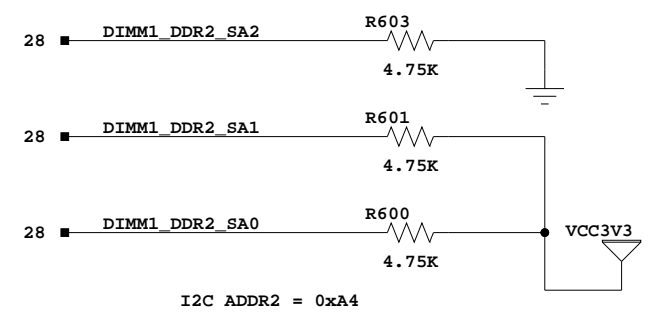
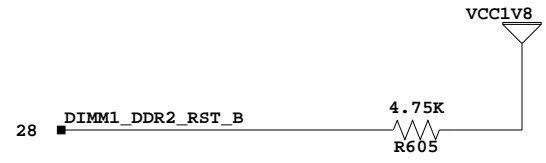


SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
DIMM1 DDR2 SSTL-2 TERMINATION

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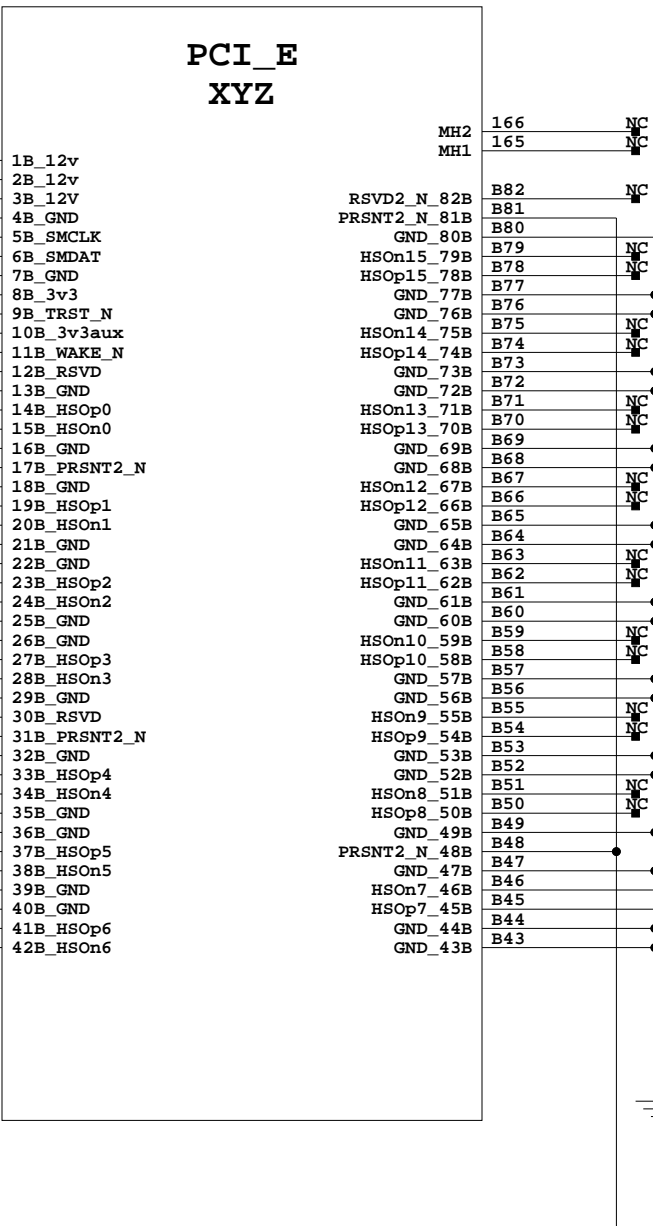
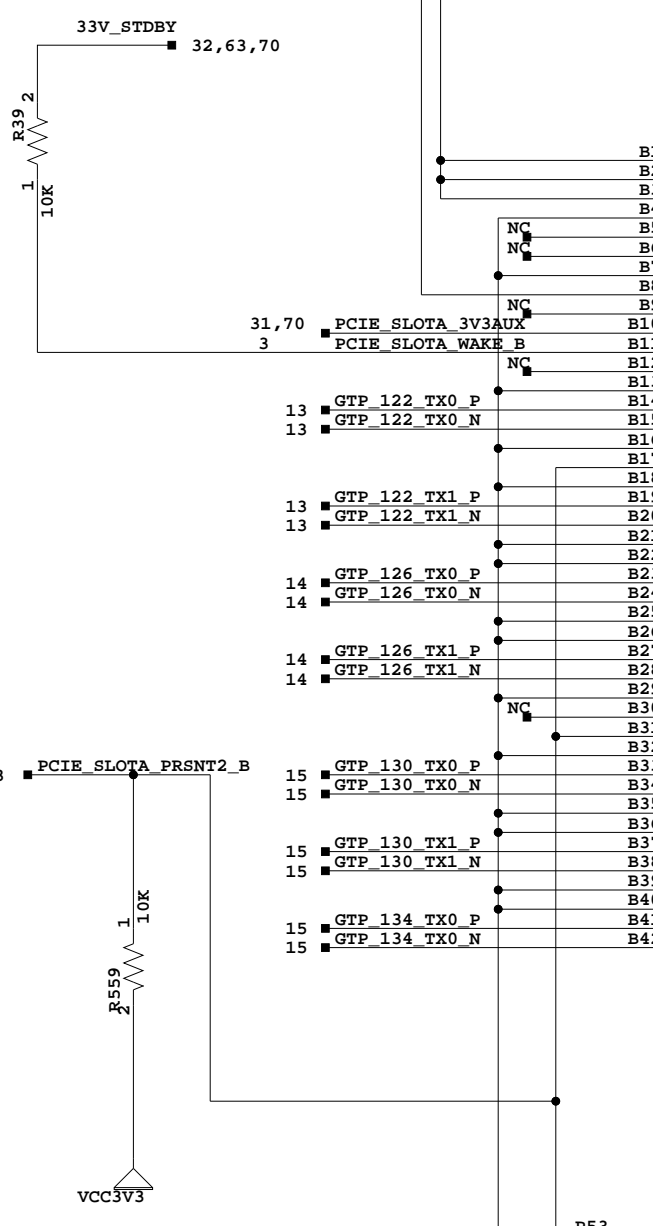
DIMM1 DDR2 DECOUPLING



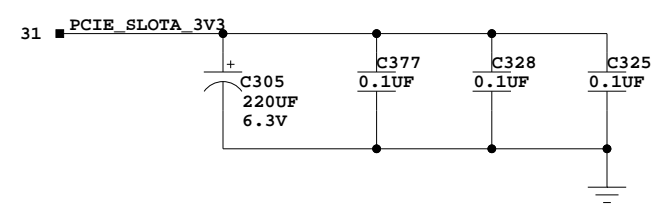
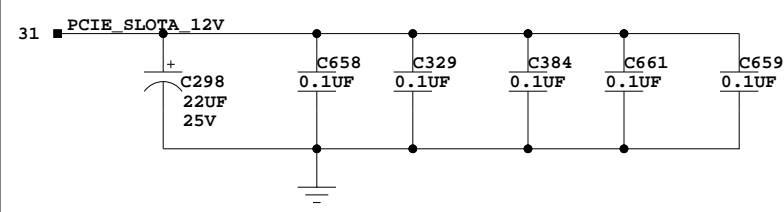
SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM	
DIMM1 DDR2 DECOUPLING	
Date: 7-10-2008_10:19	Ver: C
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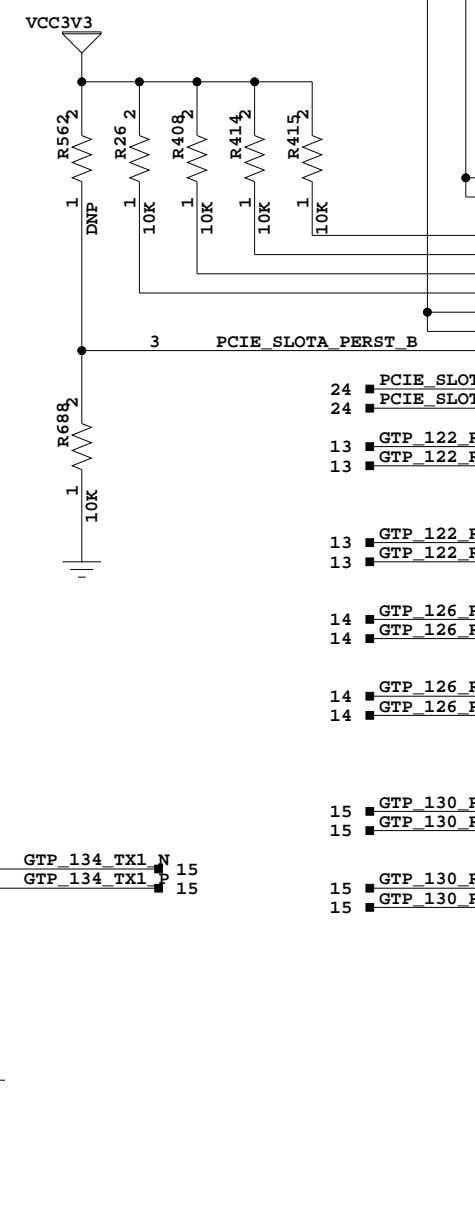
31 PCIE_SLOTA_12V
 31 PCIE_SLOTA_3V3



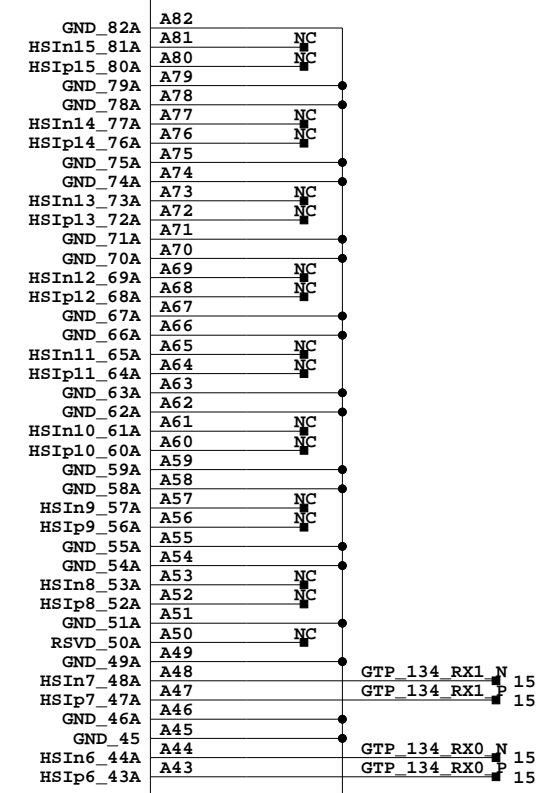
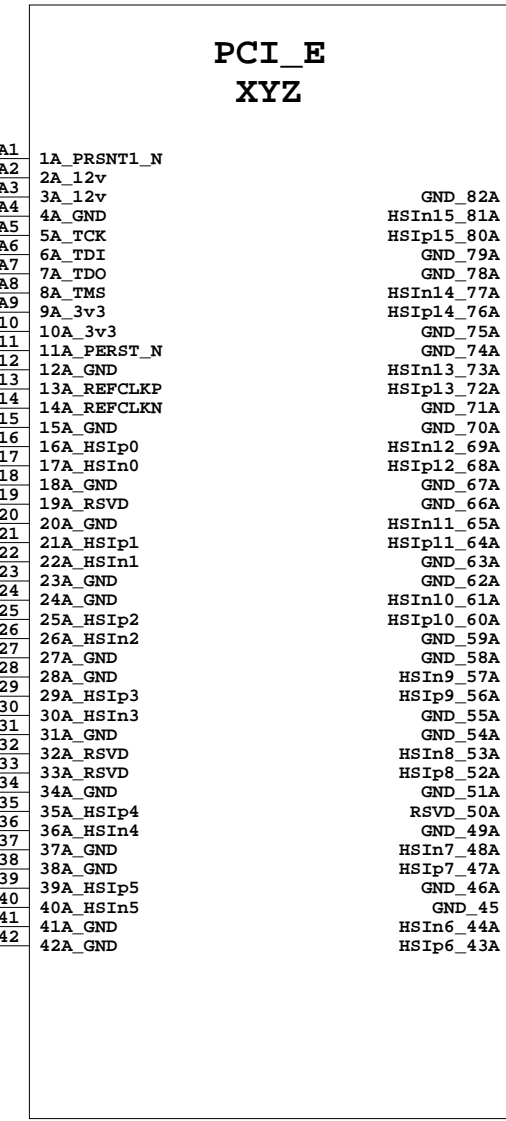
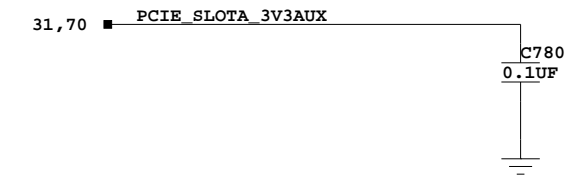
P53
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 PKG_TYPE=CON_PCI-E_164
 PARTS=1
 LEVEL=STD



31 PCIE_SLOTA_12V
 31 PCIE_SLOTA_3V3



P53
 DEVICE=PCI_E
 PKG_TYPE=CON_PCI-E_164
 PARTS=1
 LEVEL=STD



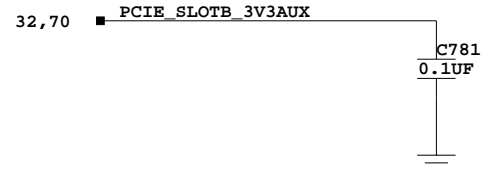
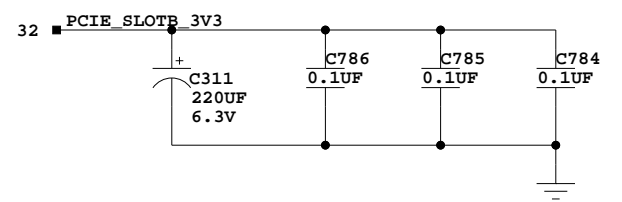
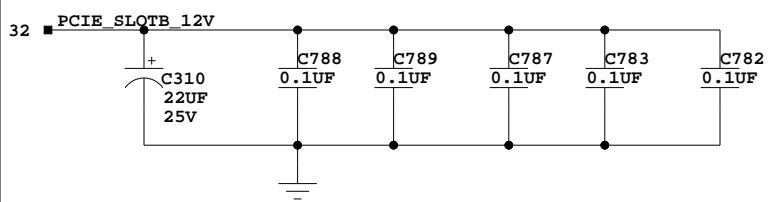
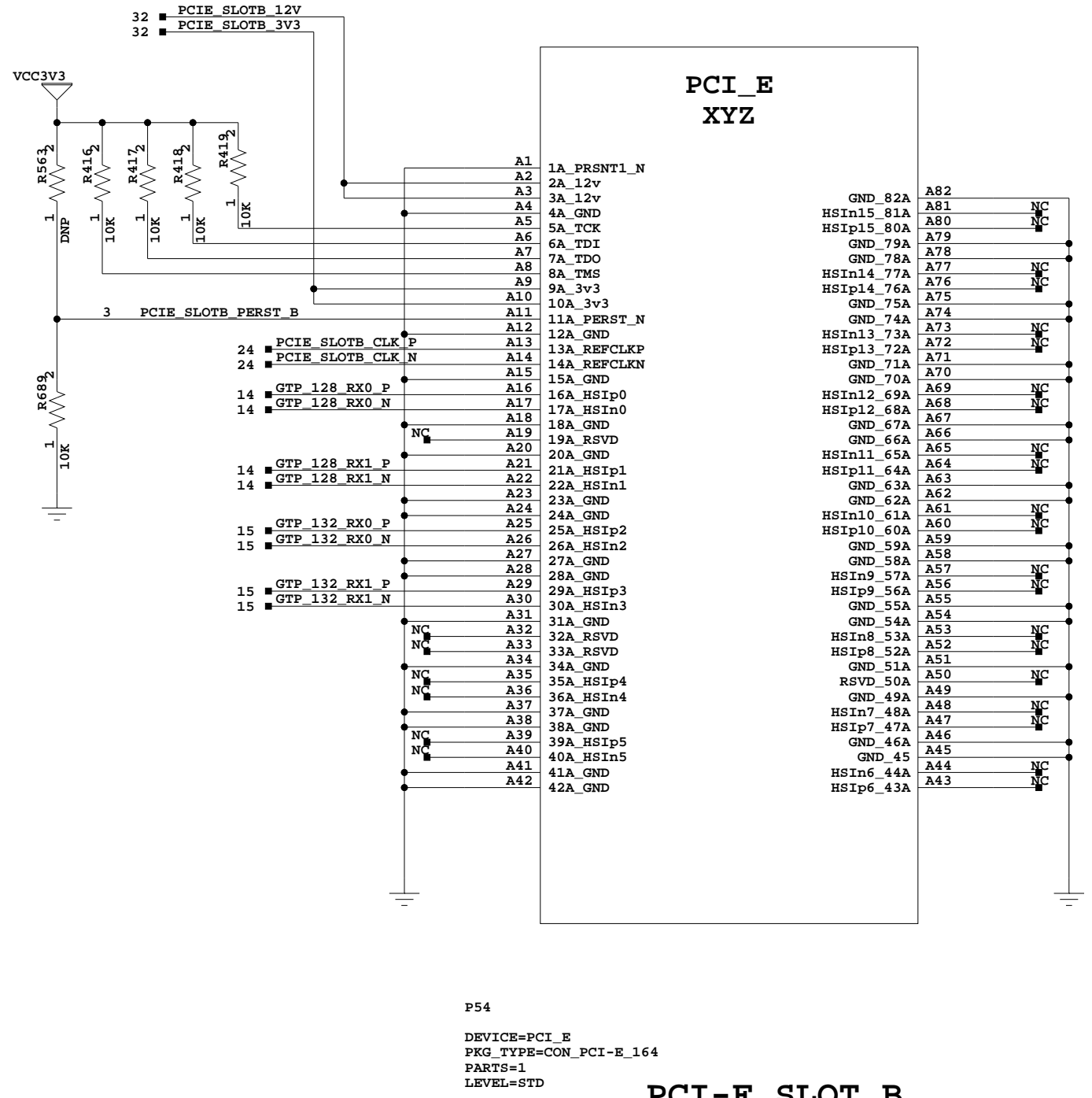
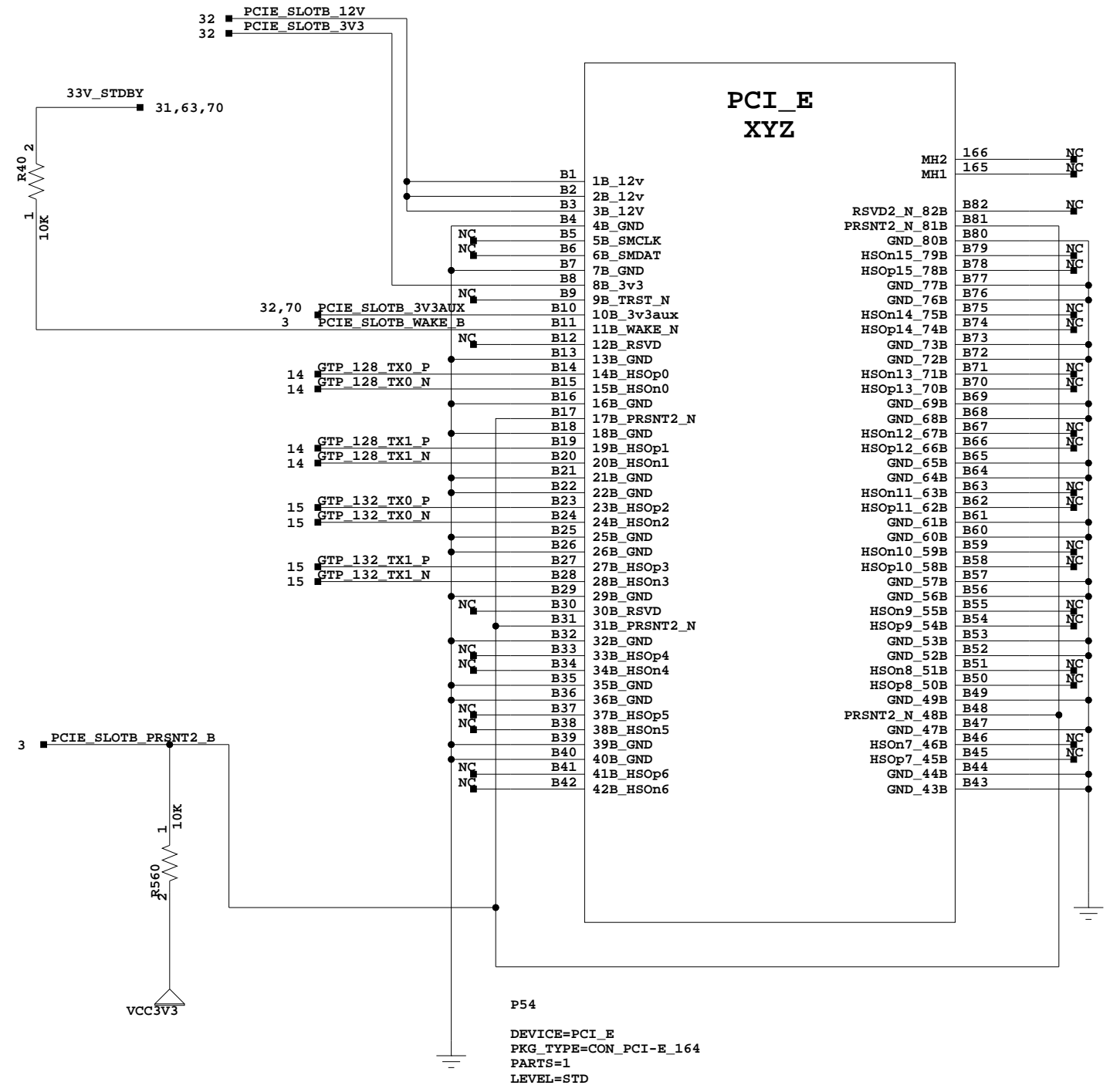
PCI-E SLOT A



SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 PCI-E SLOT A

Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	31 of 70	Drawn By	BF



PCI-E SLOT B



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFPTORM
PCI-E SLOT B

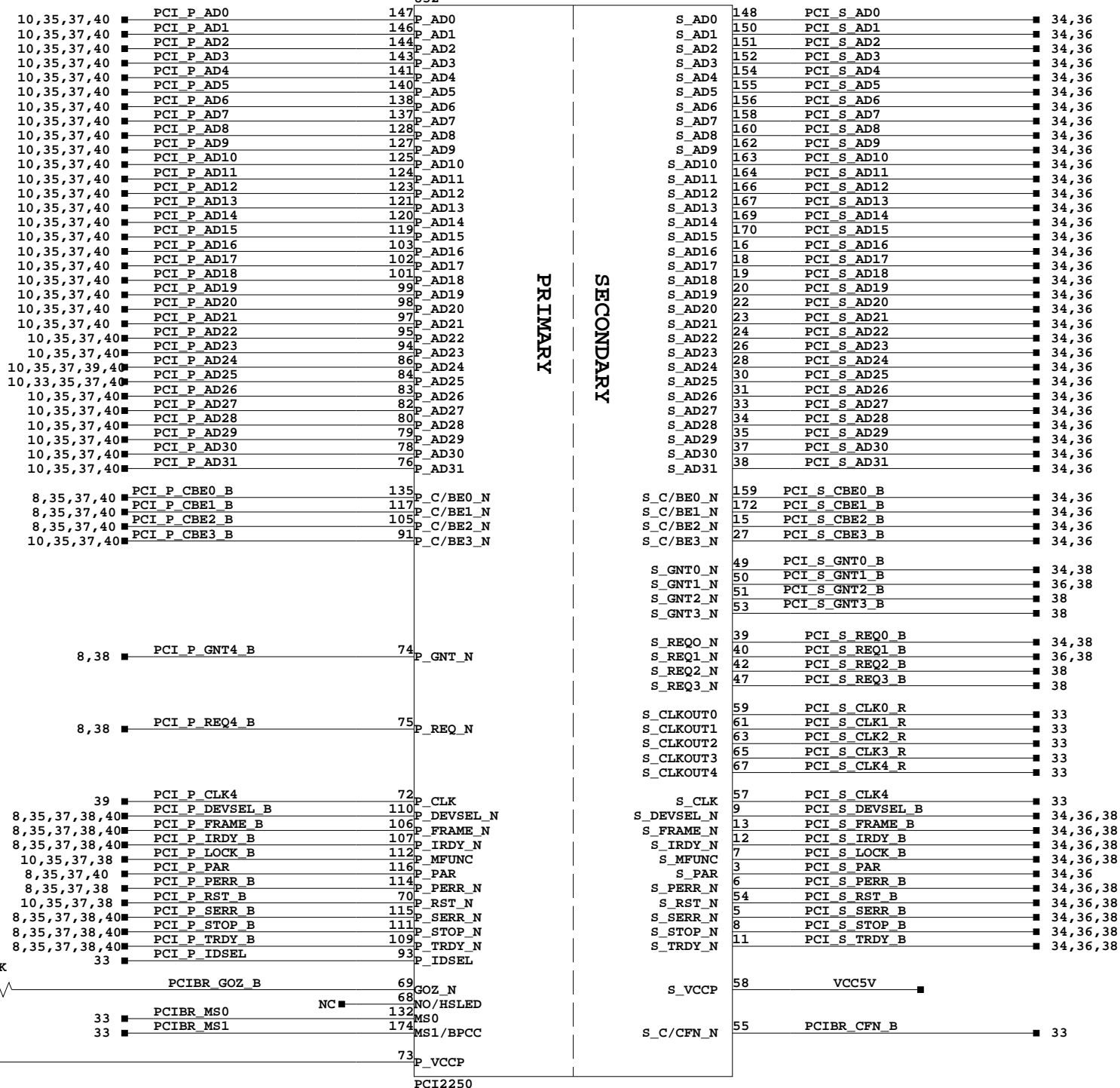
Date: 8-1-2008_15:08 Ver: C

Sheet Size: B Rev: 01

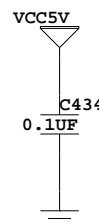
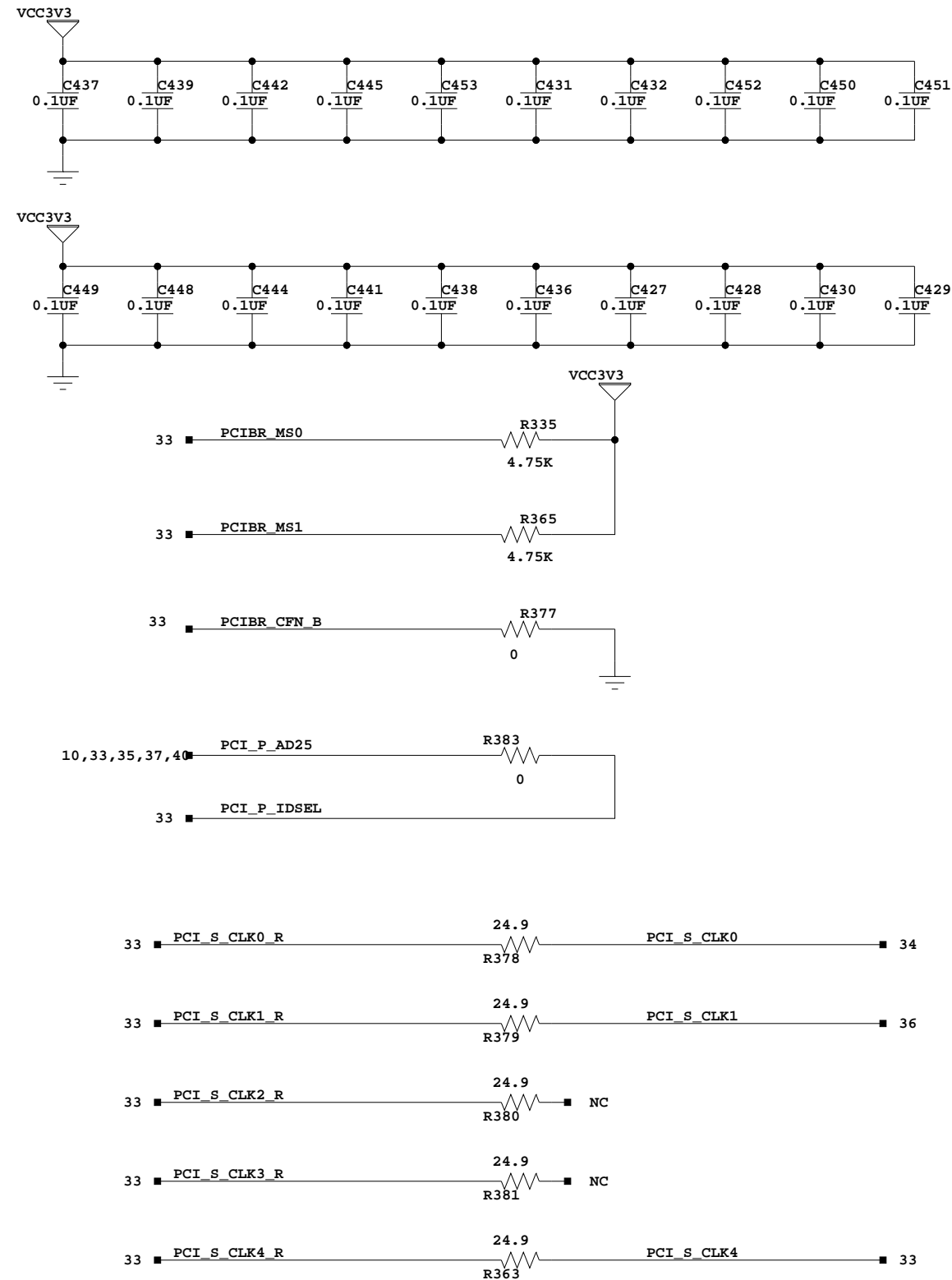
Sheet 32 of 70 Drawn By BF

PCI-PCI BRIDGE
PCI2250_PGF

U32



VCC3V3;10,17,25,32,44,52,62,66,81,88,100
VCC3V3;108,118,126,139,145,153,161,168,176
GND;1,14,21,29,36,45,56,60,64,71,77,89
GND;96,104,113,122,130,133,142,149,157,165,171
NC=2,4,41,43,46,48,85,87,90,92,129,131,134,136,173,175



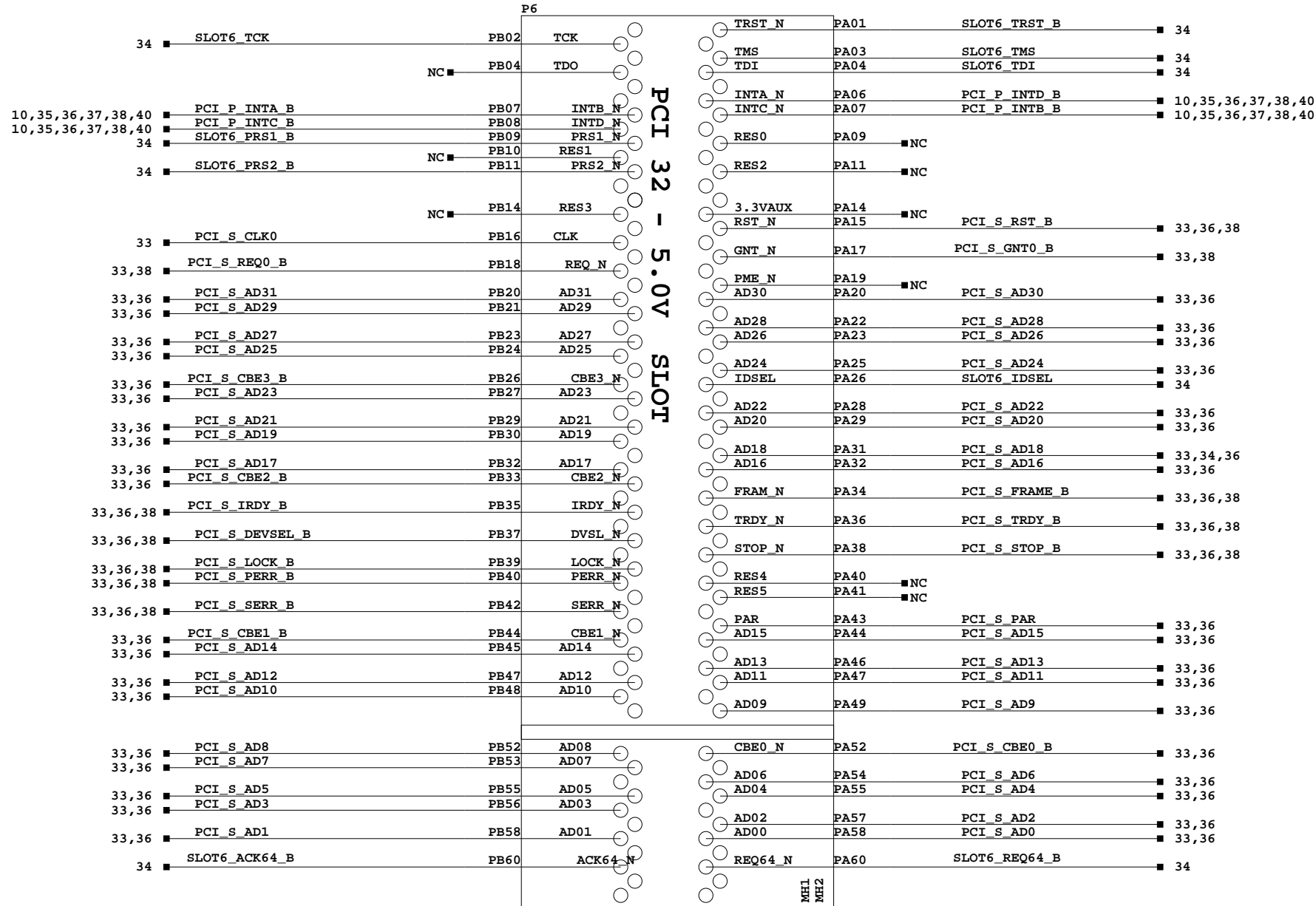
PCI-PCI BRIDGE



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
PCI-PCI BRIDGE

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	33 of 70	Drawn By	BF

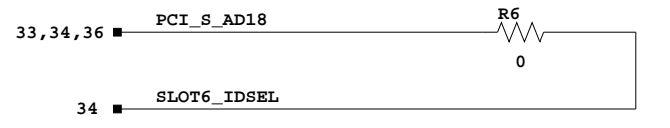
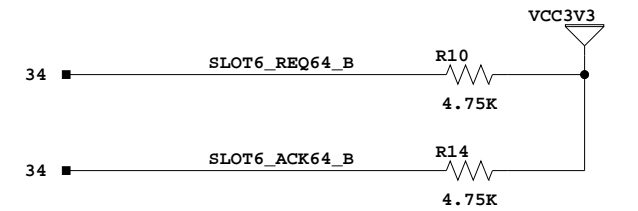
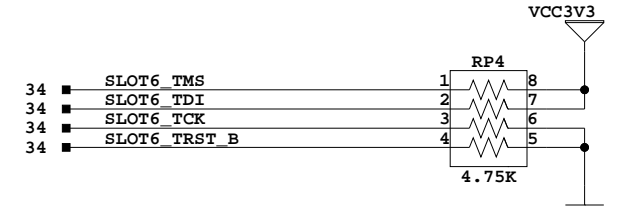
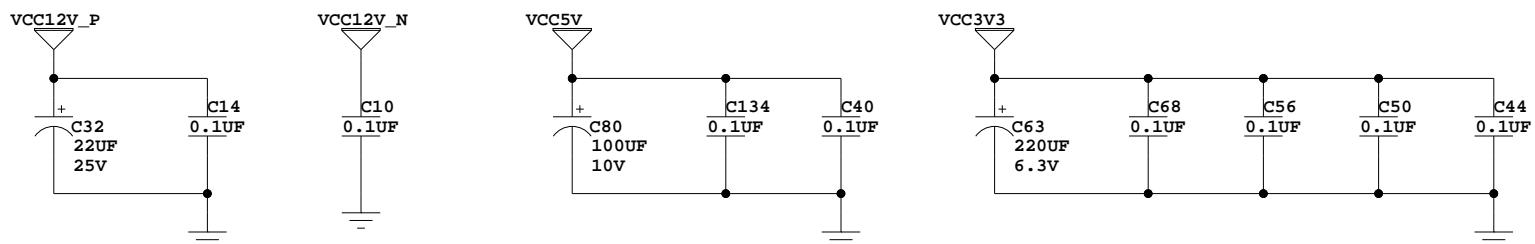


VCC12V_P;PA02
VCC12V_N;PB01
VCC5V;PA05,PB05,PB06,PA08,PA61,PA62,PB61,PB62

VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

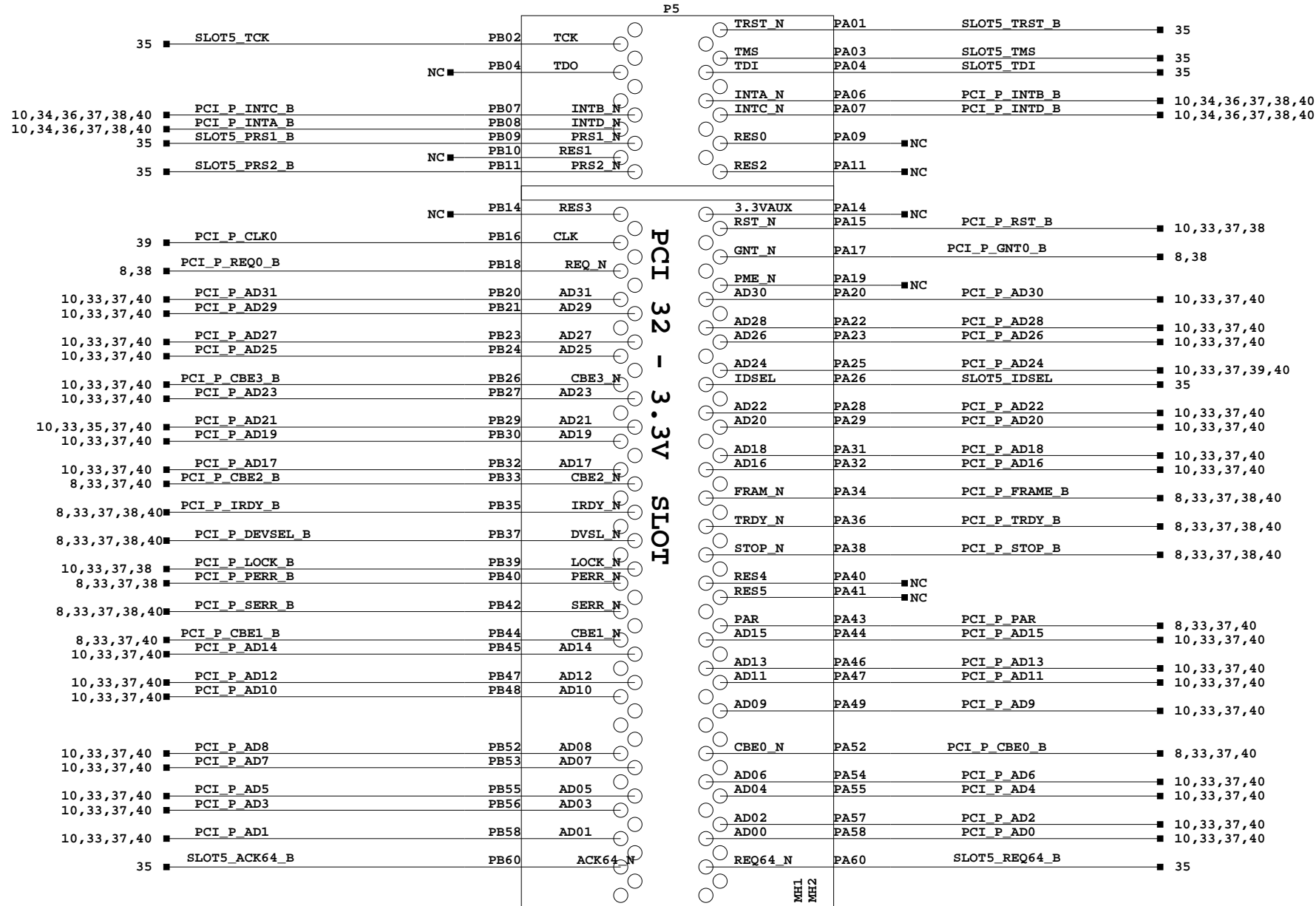
VCCIO VCC5V;PA10,PA16,PB19,PB59,PA59

GND;PB03,PB15,PB17,PA18,PB22,PA24
GND;PB28,PA30,PB34,PA35,PA37,PB38
GND;PA42,PB46,PA48,PB49,PA56,PB57
GND;PB12,PA12,PB13,PA13



PCI SLOT 6, 5.0V, SECONDARY BUS

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM PCI SLOT 6, 5.0V, SECONDARY BUS		
Date:	7-10-2008_10:19	Ver: C
Sheet Size:	B	Rev: 01
Sheet	34 of 70	Drawn By BF

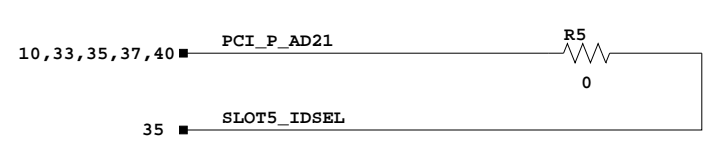
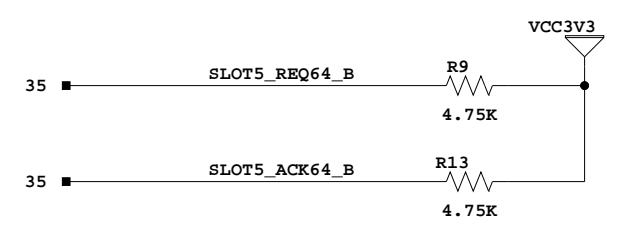
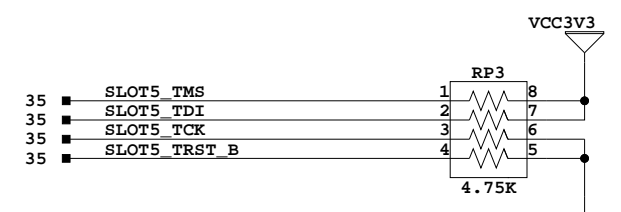
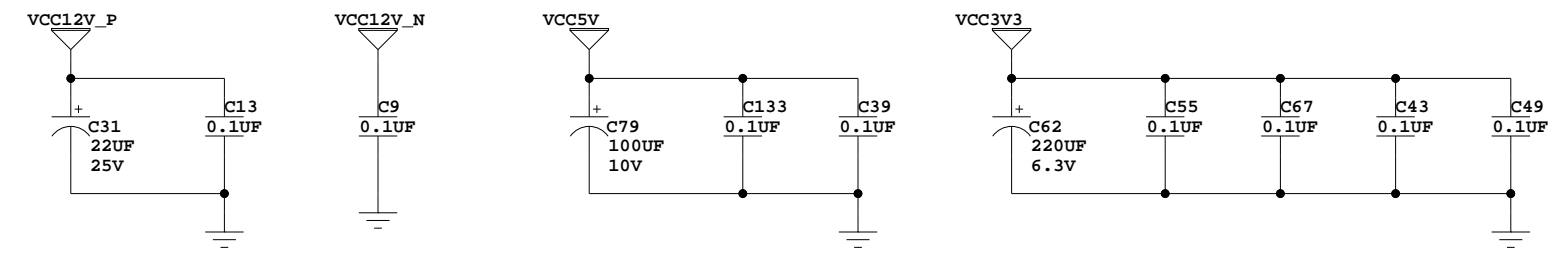


SIGNAL=GND; PA50, PA51, PB50, PB51

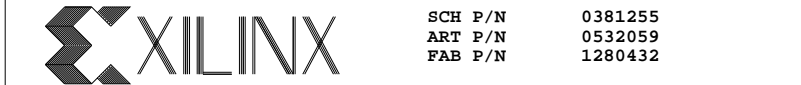
VCC12V_P;PA02
 VCC12V_N;PB01
 VCC5V;PA05, PB05, PB06, PA08
 VCC5V;PA61, PB61, PA62, PB62
 VCC3V3;PA21, PB25, PA27, PB31, PA33, PB36
 VCC3V3;PA39, PB41, PB43, PA45, PA53, PB54

VCCIO VCC3V3;PA10, PA16, PB19, PB59, PA59

GND;PB03, PB15, PB17, PA18, PB22, PA24
 GND;PB28, PA30, PB34, PA35, PA37, PB38
 GND;PA42, PB46, PA48, PB49, PA56, PB57

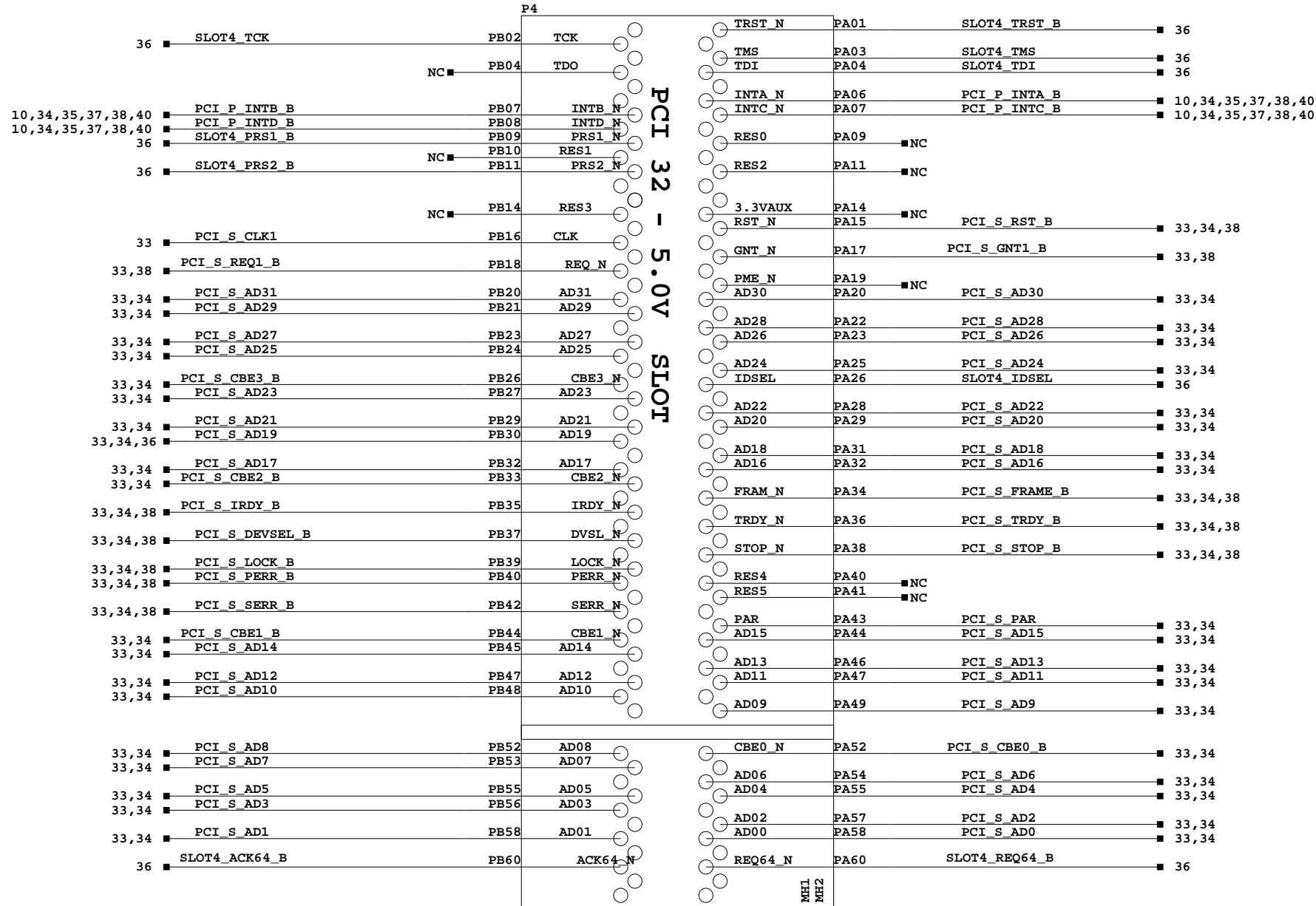


PCI SLOT 5, 3.3V, PRIMARY BUS



Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
PCI SLOT 5, 3.3V, PRIMARY BUS

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
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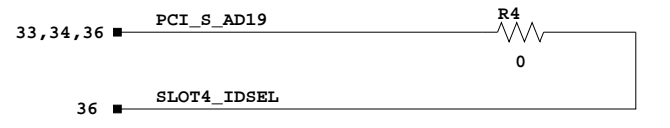
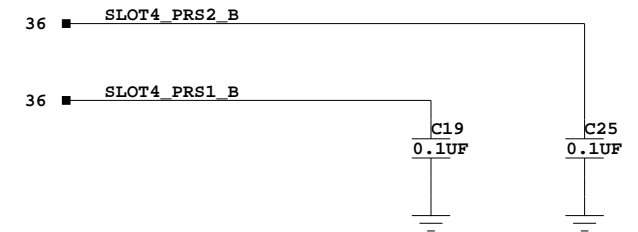
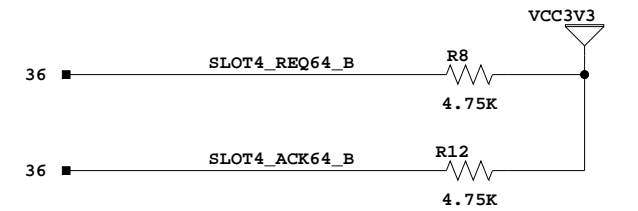
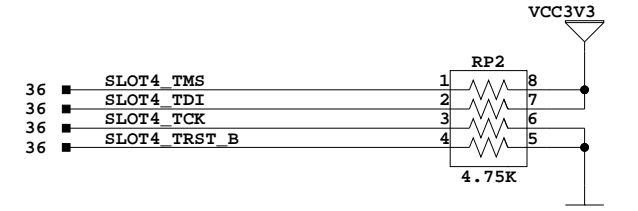
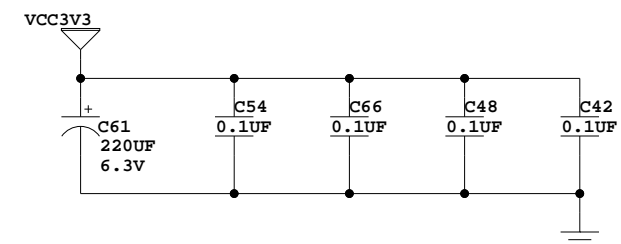
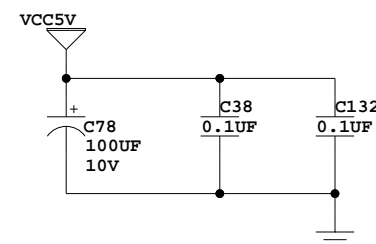
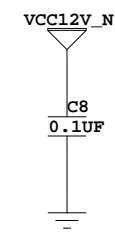
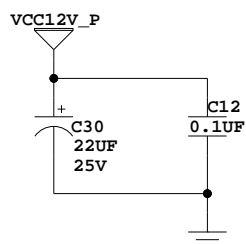


VCC12V_P;PA02
 VCC12V_N;PB01
 VCC5V;PA05, PB05, PB06, PA08, PA61, PA62, PB61, PB62

VCC3V3;PA21, PB25, PA27, PB31, PA33, PB36
 VCC3V3;PA39, PB41, PB43, PA45, PA53, PB54

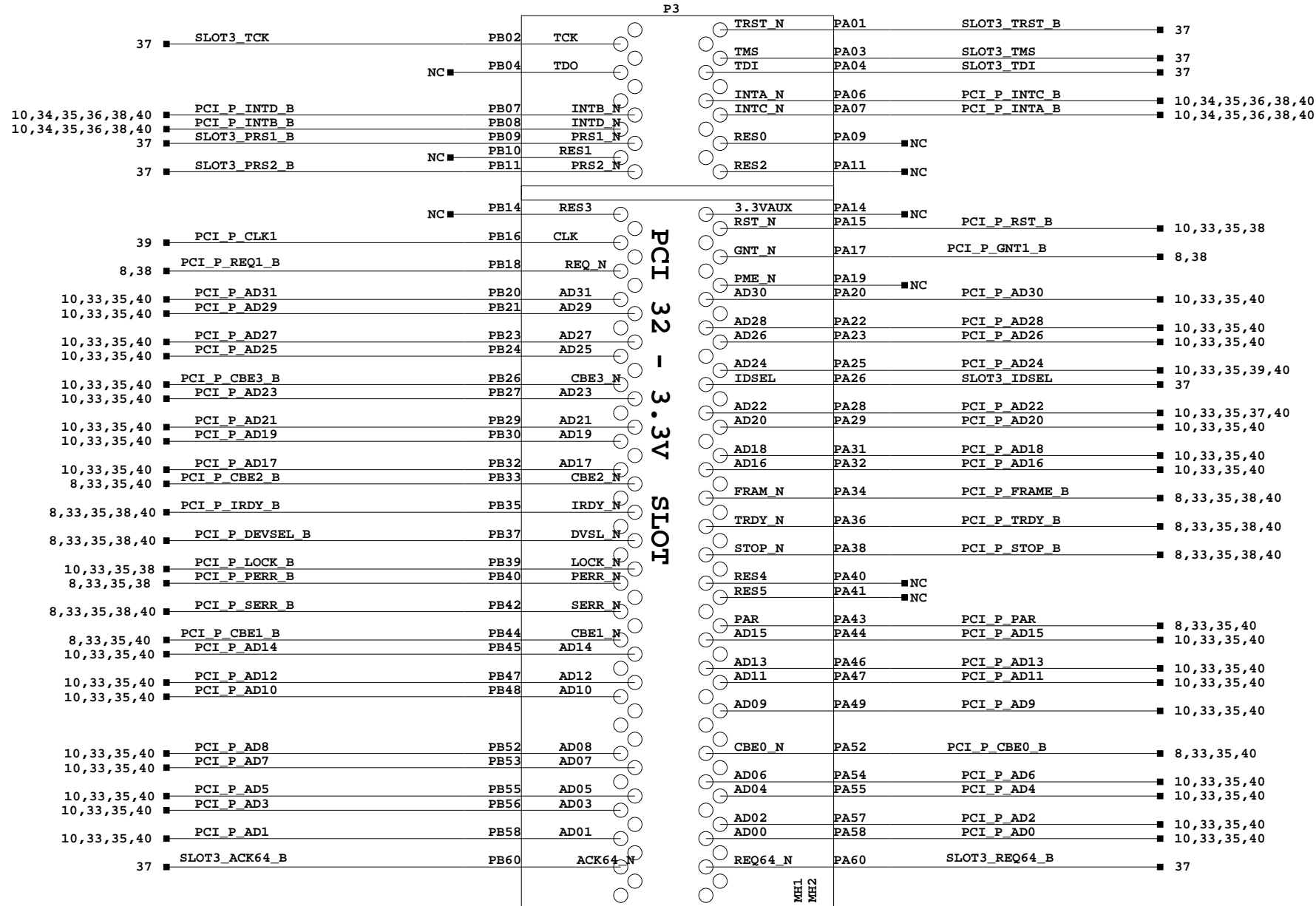
VCCIO VCC5V;PA10, PA16, PB19, PB59, PA59

GND;PB03, PB15, PB17, PA18, PB22, PA24
 GND;PB28, PA30, PB34, PA35, PA37, PB38
 GND;PA42, PB46, PA48, PB49, PA56, PB57
 GND;PB12, PA12, PB13, PA13



PCI SLOT 4, 5.0V, SECONDARY BUS

		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM			
PCI SLOT 4, 5.0V, SECONDARY BUS			
Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	36 of 70	Drawn By	BF

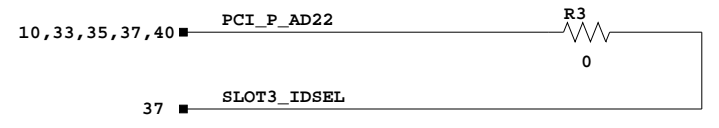
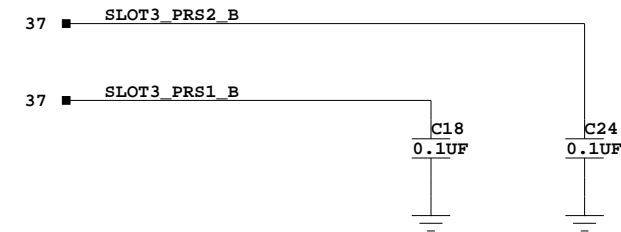
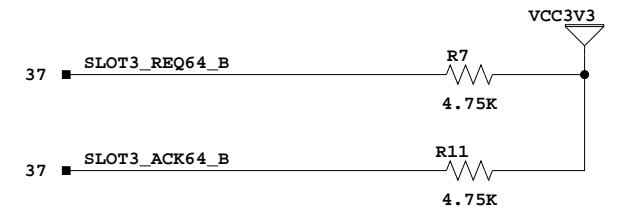
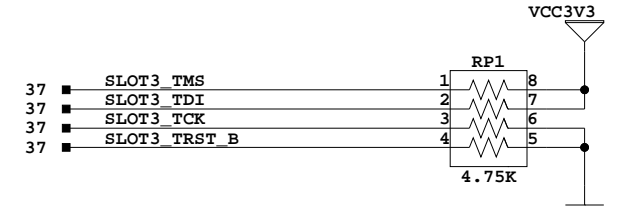
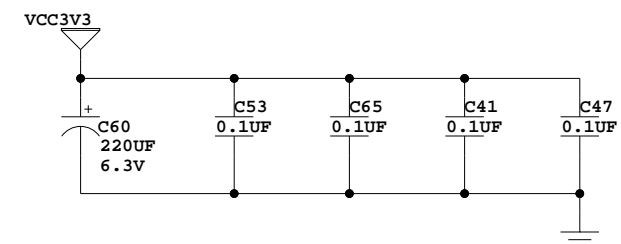
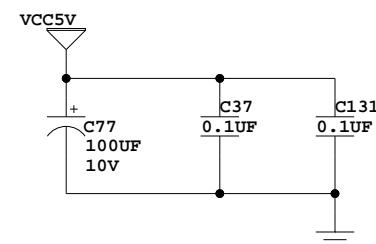
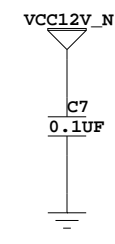
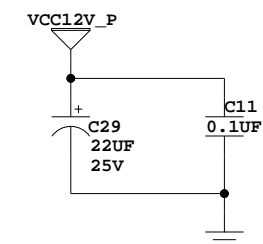


SIGNAL=GND; PA50, PA51, PB50, PB51

VCC12V_P;PA02
 VCC12V_N;PB01
 VCC5V;PA05, PB05, PB06, PA08
 VCC5V;PA61, PB61, PA62, PB62
 VCC3V3;PA21, PB25, PA27, PB31, PA33, PB36
 VCC3V3;PA39, PB41, PB43, PA45, PA53, PB54

VCCIO VCC3V3;PA10, PA16, PB19, PB59, PA59

GND;PB03, PB15, PB17, PA18, PB22, PA24
 GND;PB28, PA30, PB34, PA35, PA37, PB38
 GND;PA42, PB46, PA48, PB49, PA56, PB57



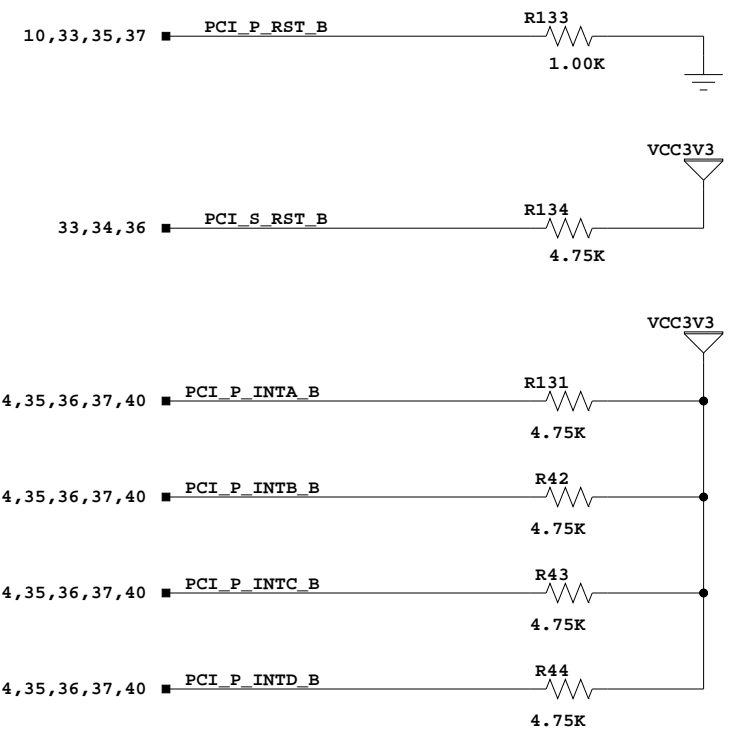
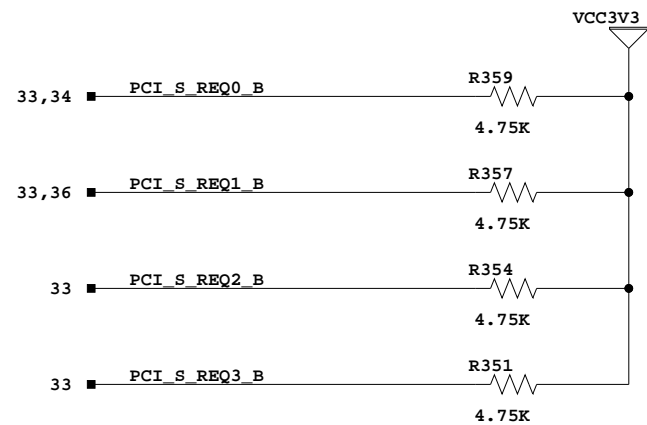
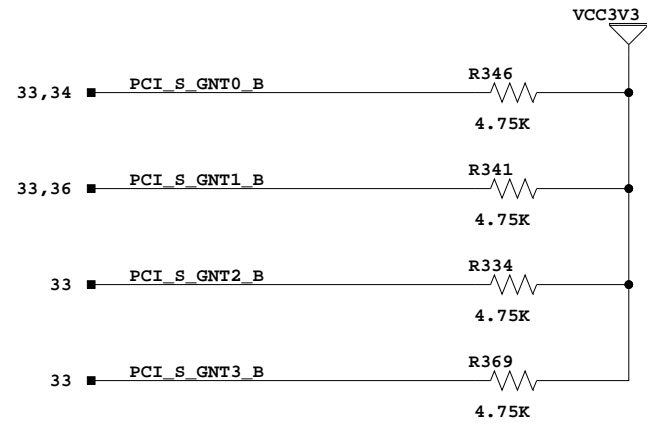
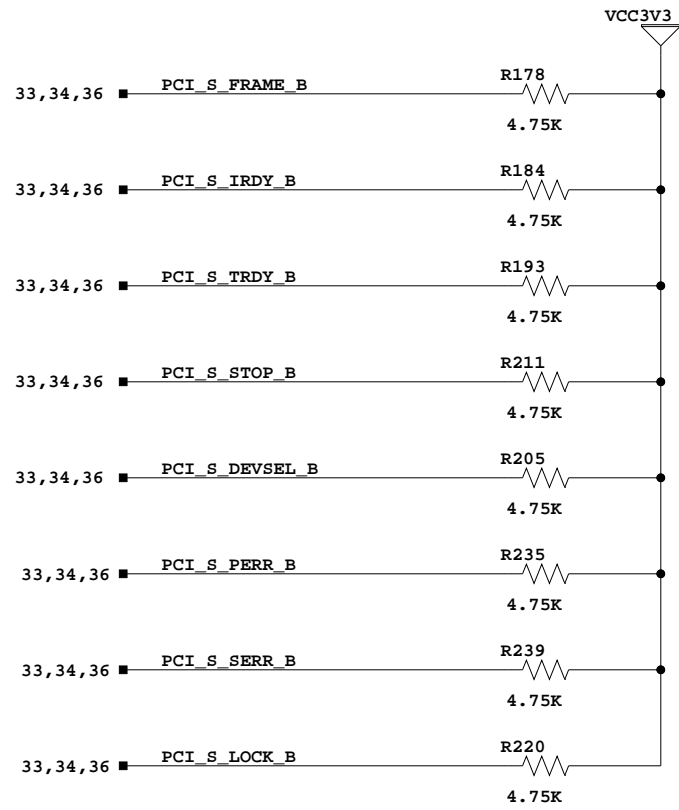
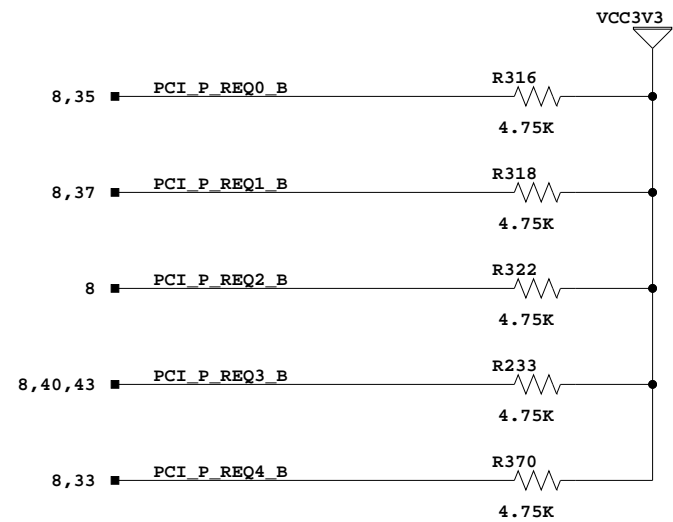
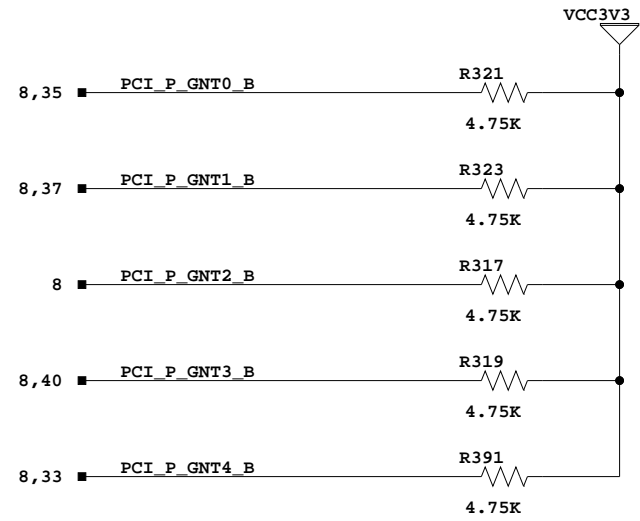
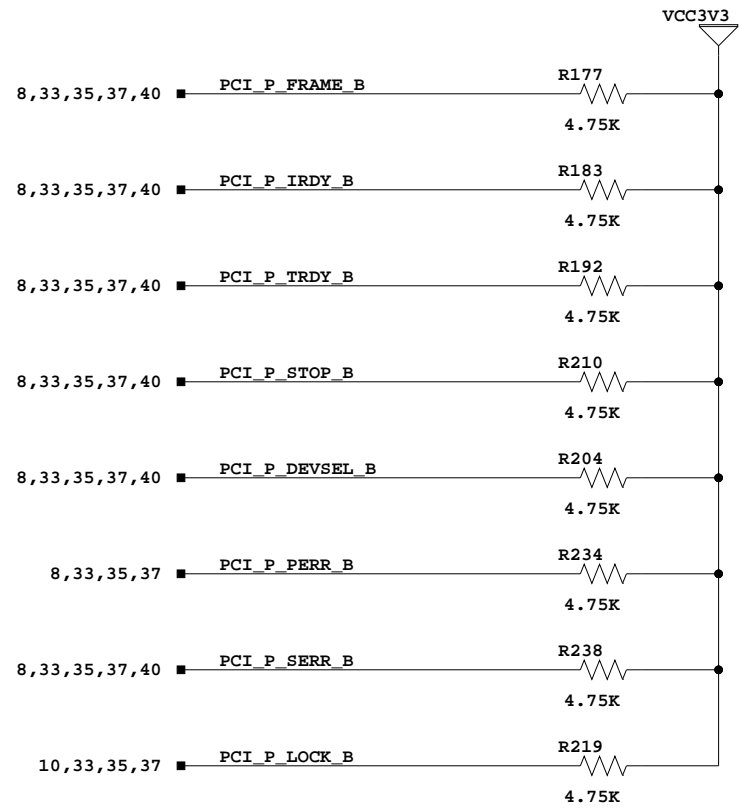
PCI SLOT 3, 3.3V, PRIMARY BUS



SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 PCI SLOT 3, 3.3V, PRIMARY BUS

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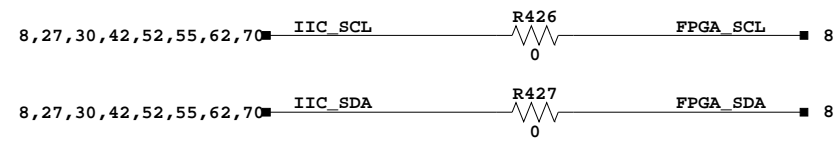
PCI BUS PULLUPS



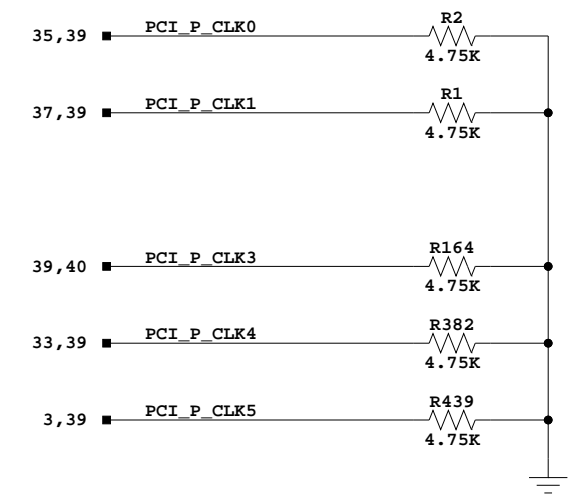
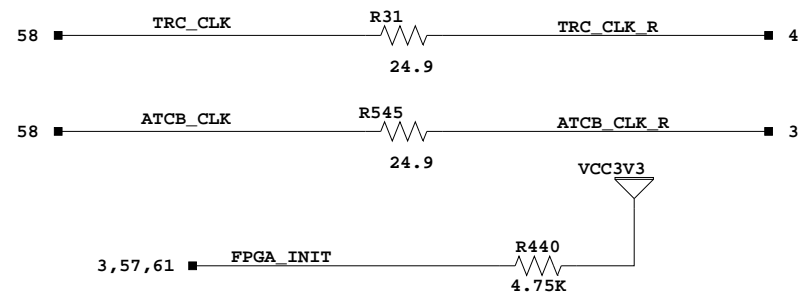
SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 PCI BUS PULLUPS

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
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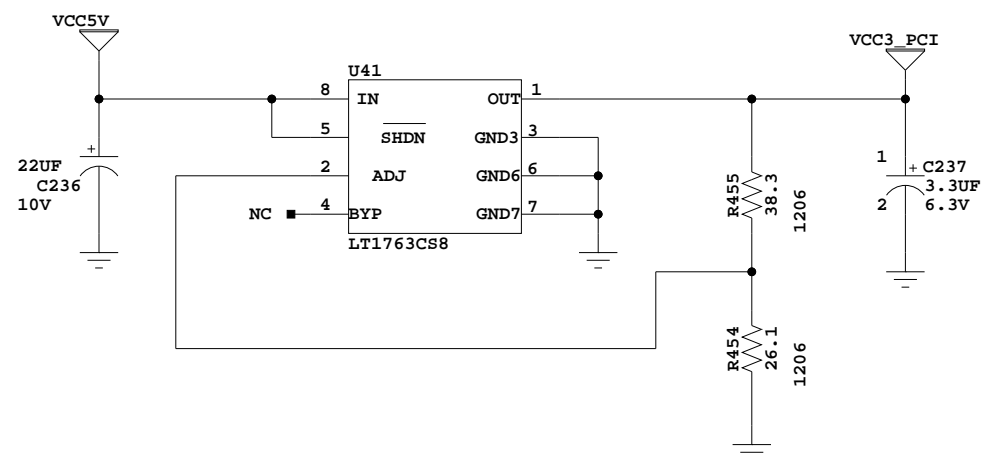
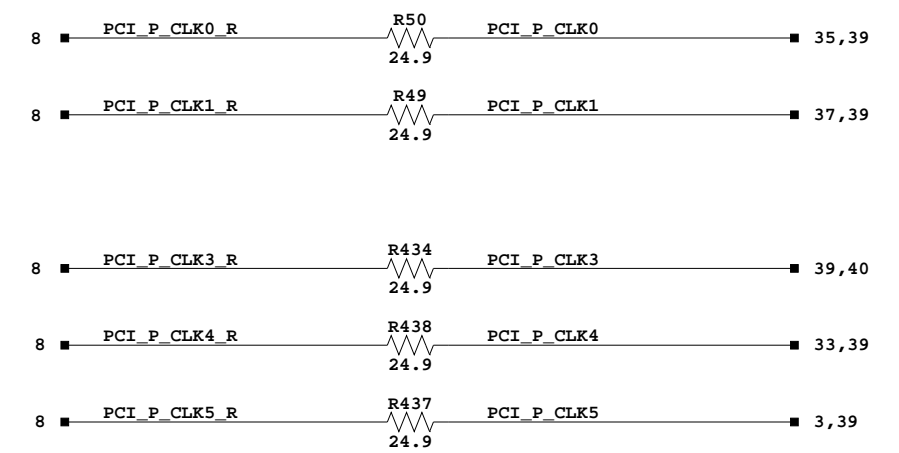


NOTE: TRC_CLK RESISTOR ALLOWS CLOCK TERMINATION
 TO BE ADJUSTED INDEPENDENTLY OF OTHER I/O.

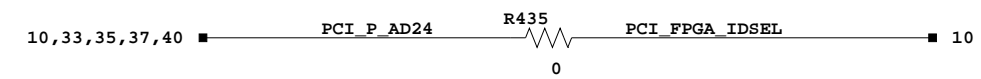


NOTE: THE PCI SPEC RECOMMENDS THAT
 CLOCKS BE PULLED LOW WHEN THE
 BUS IS NOT ACTIVELY CLOCKED.

NOTE: PCI_CLK RESISTORS ALLOW CLOCK TERMINATION
 TO BE ADJUSTED INDEPENDENTLY OF OTHER I/O.



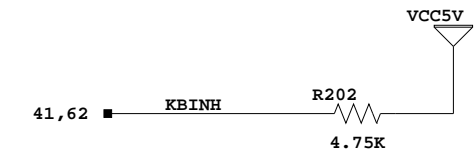
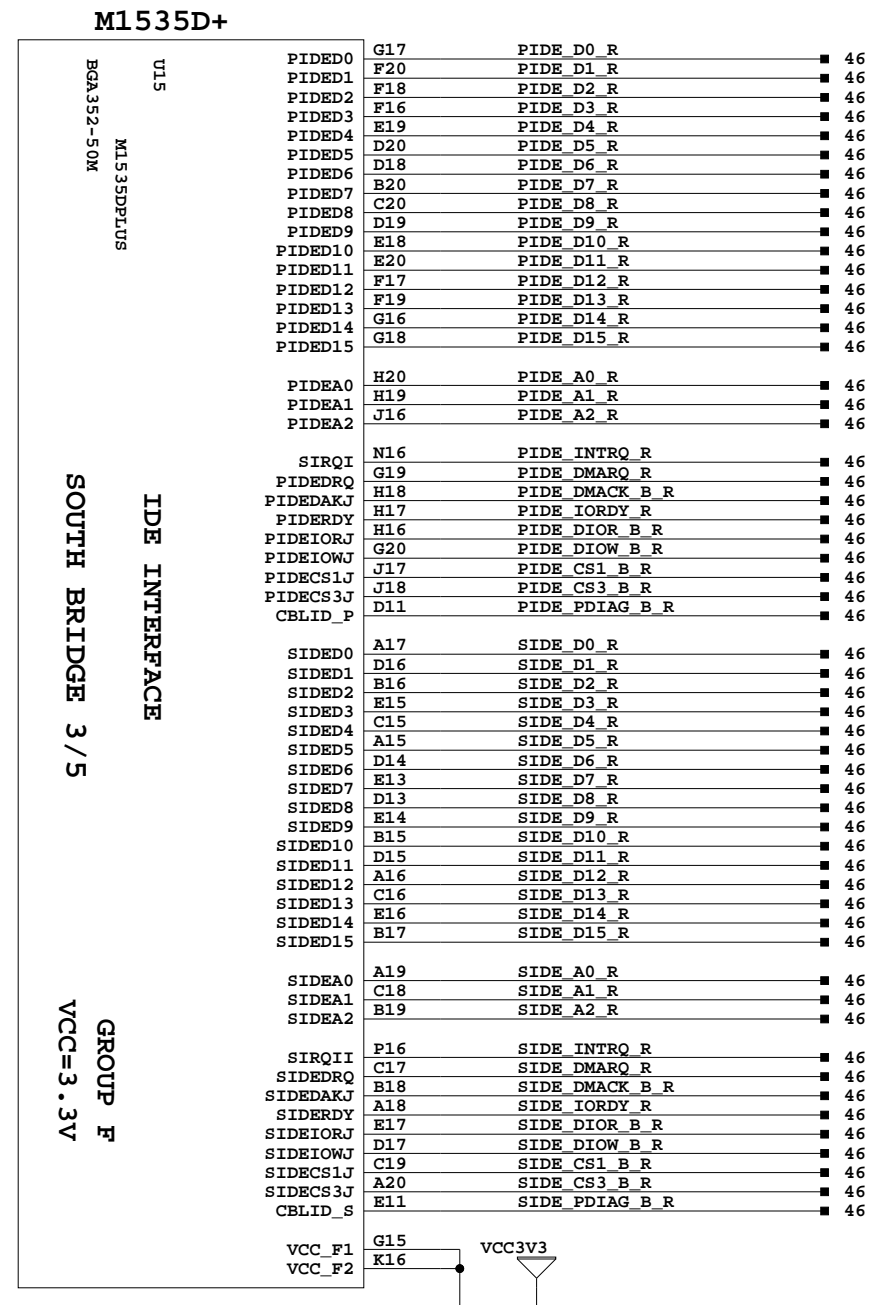
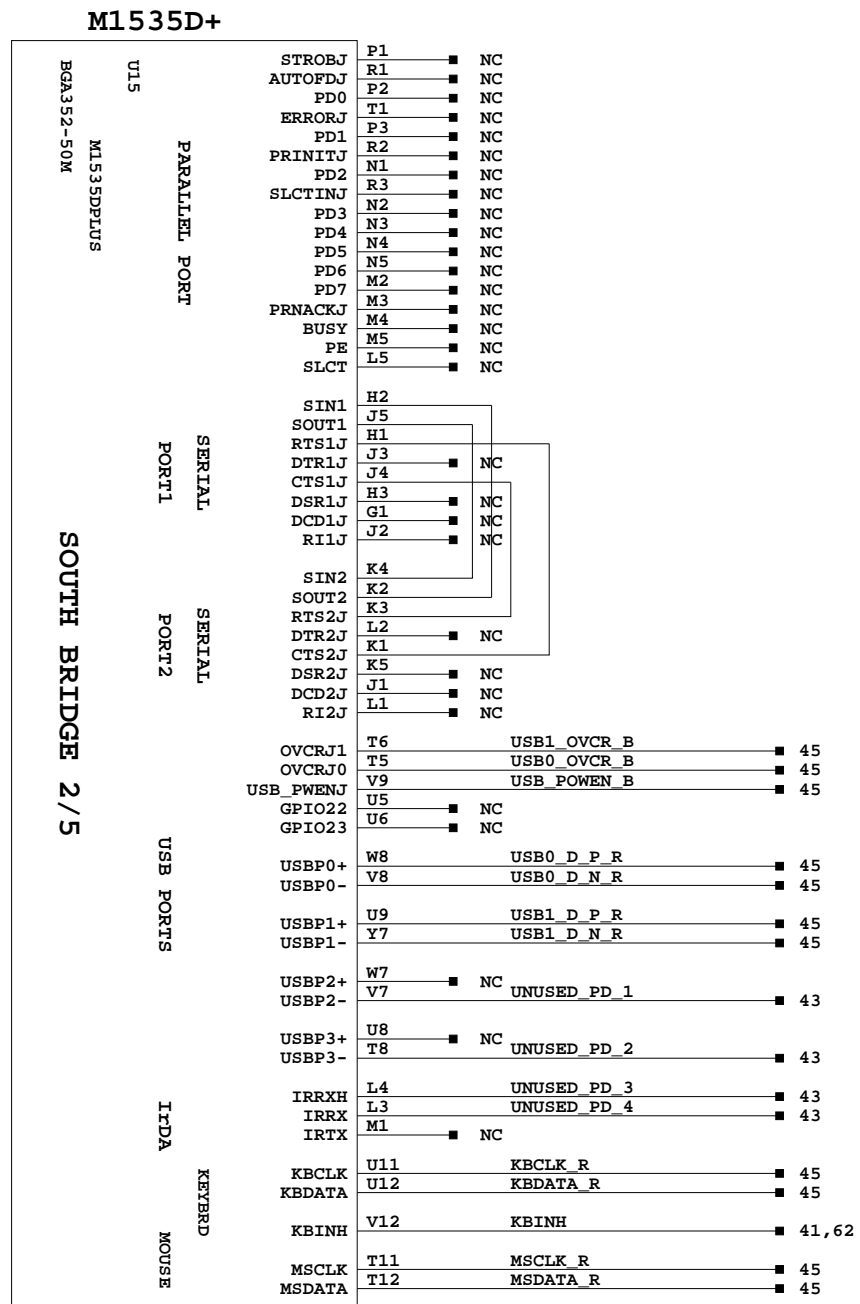
NOTE: THE COMPONENT VALUES FOR THIS REGULATOR ARE TAKEN
 FROM XAPP653. THIS DESIGN IS INTENDED TO SINK CURRENT
 THROUGH THE 1206 RESISTORS WHEN THE CLAMP DIODES ON
 THE FPGA ARE CONDUCTING DURING OVERSHOOT. THIS IS WHY
 THE VALUES ARE UNUSUAL RELATIVE TO THE LT1763 DATASHEET.



PCI SUPPLY AND TERMINATION



Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM PCI SUPPLY AND TERMINATION	
Date: 7-10-2008_10:19	Ver: C
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PCI SOUTH BRIDGE, PART 2-3



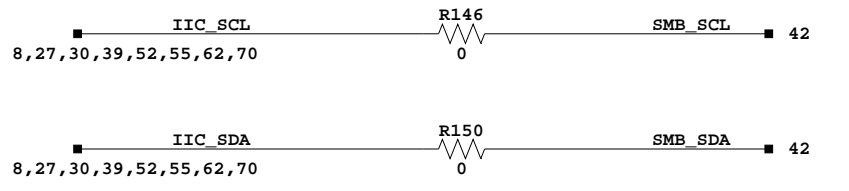
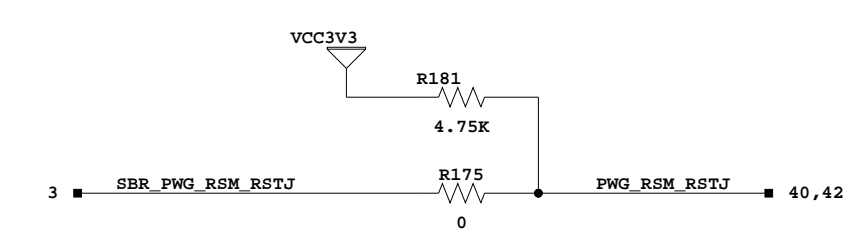
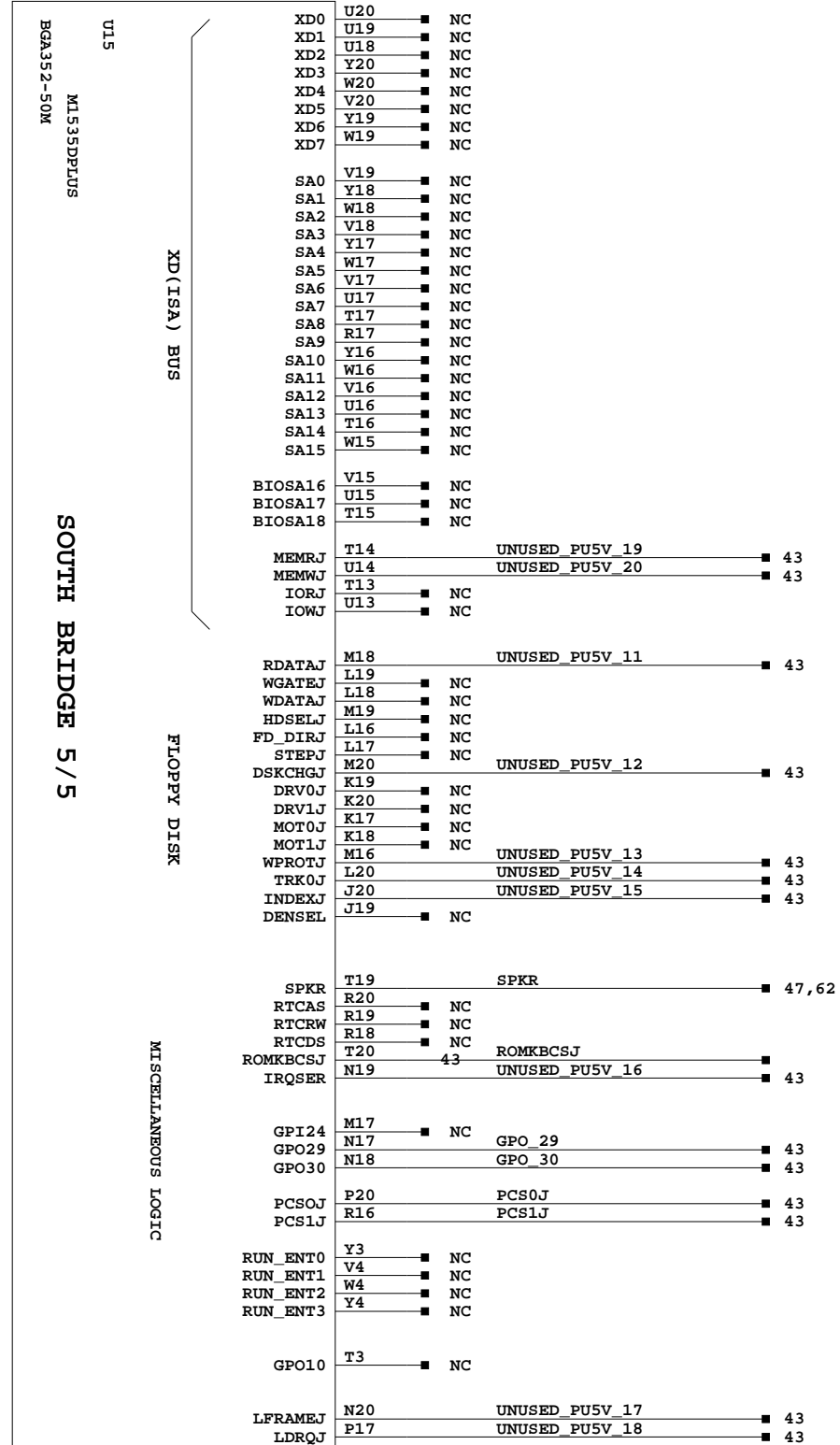
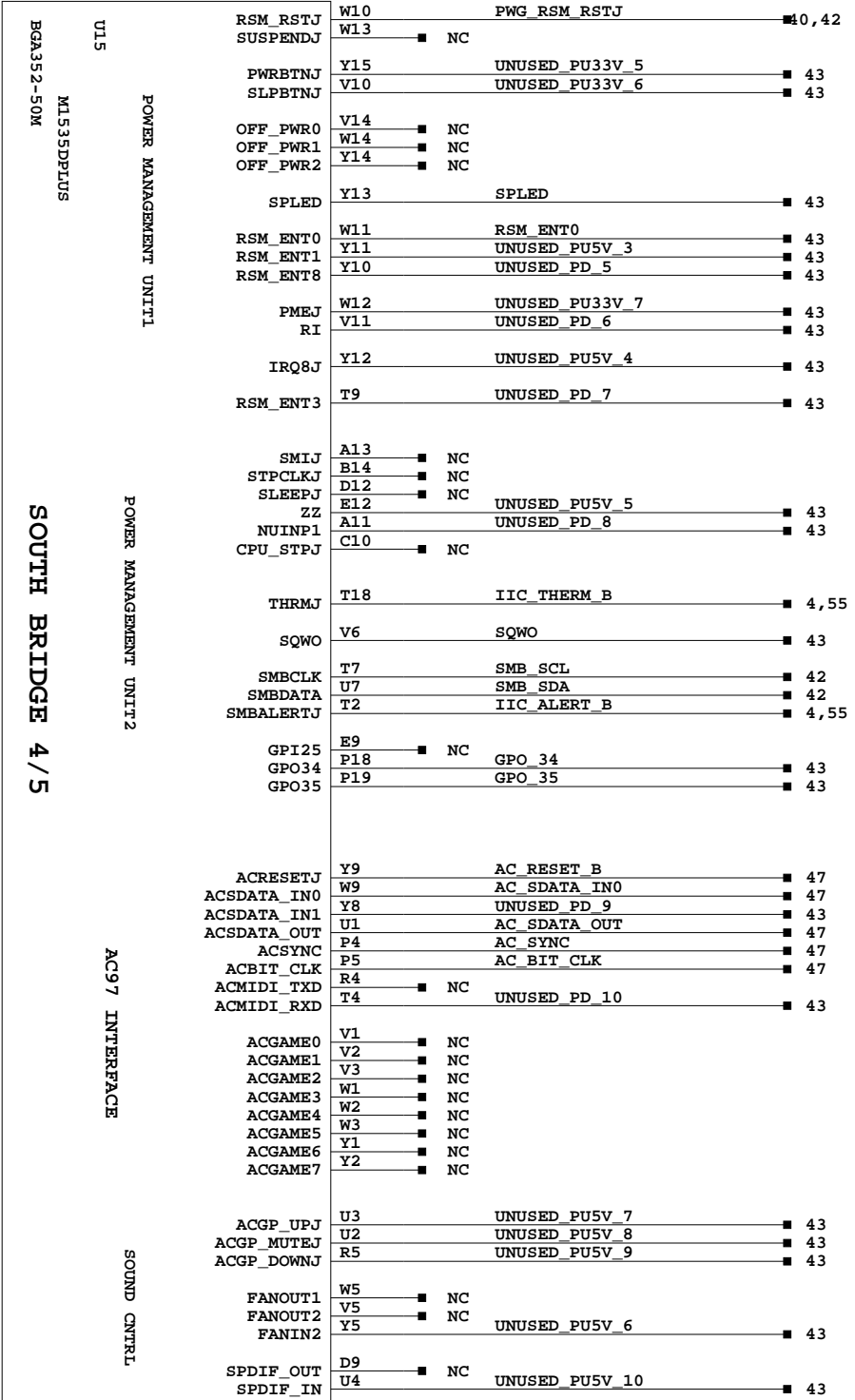
SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
PCI SOUTH BRIDGE, PART 2-3

Date:	7-10-2008_10:19	Ver:	C
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M1535D+

M1535D+



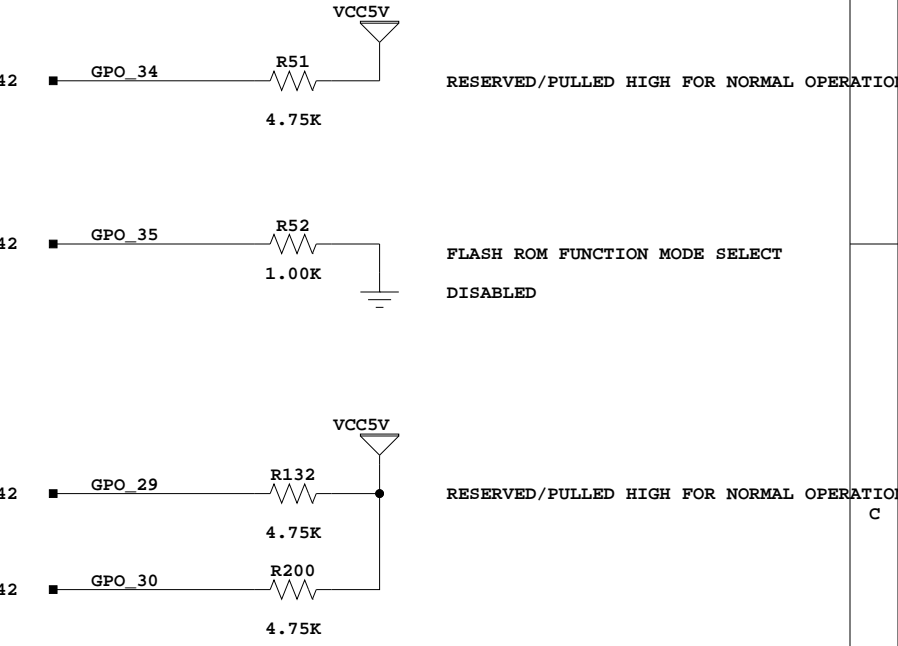
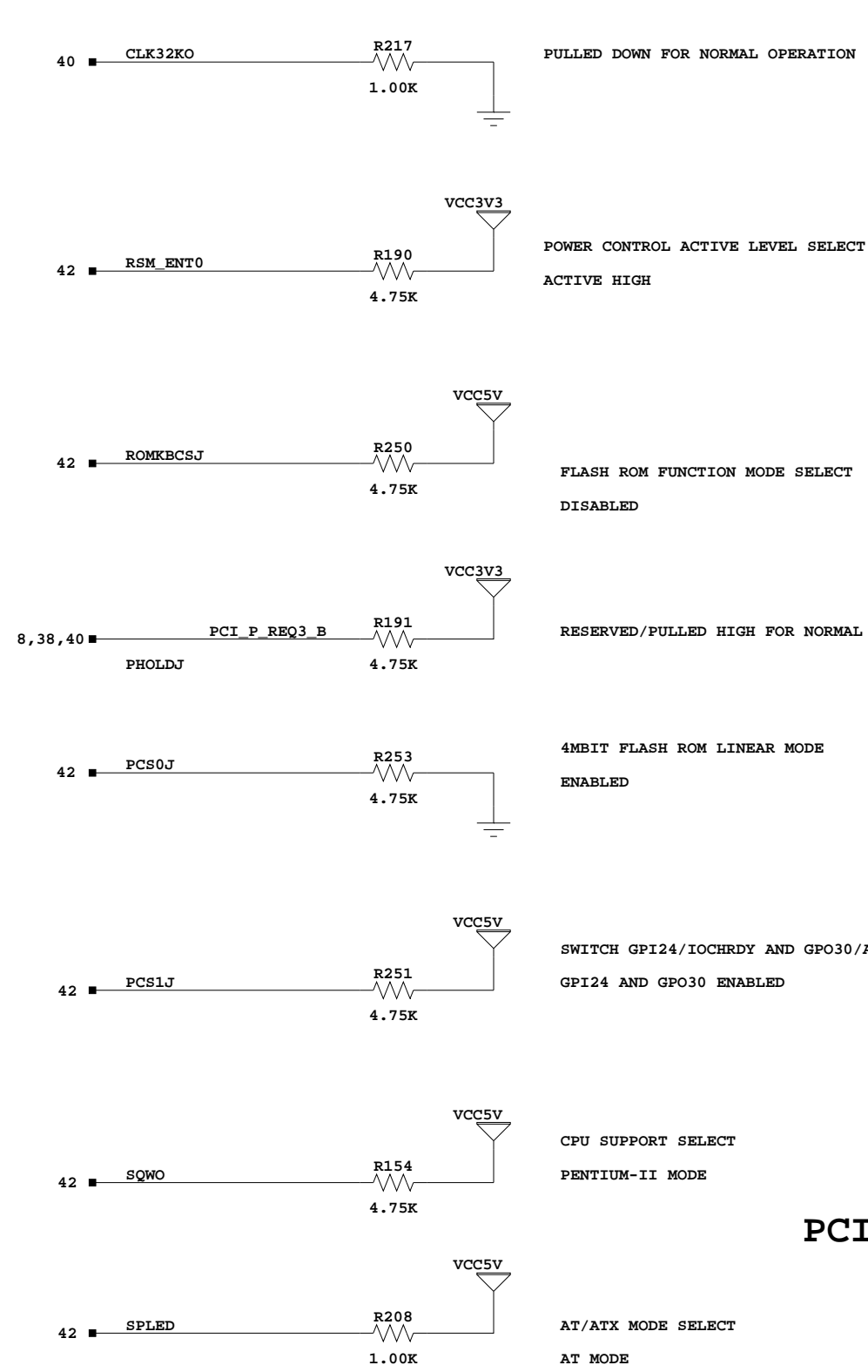
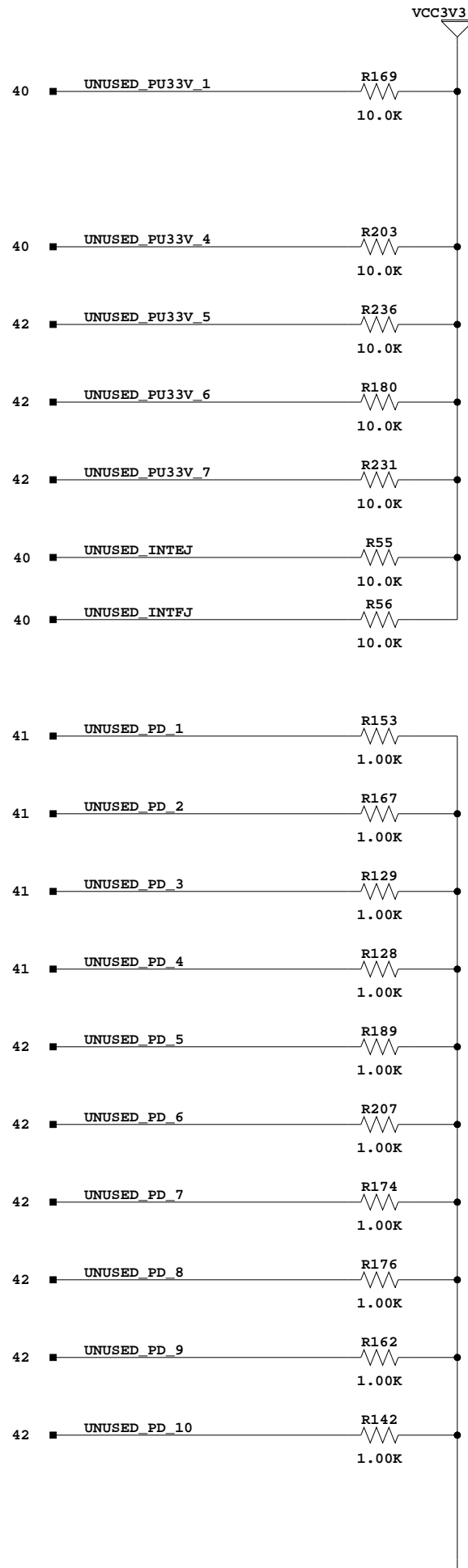
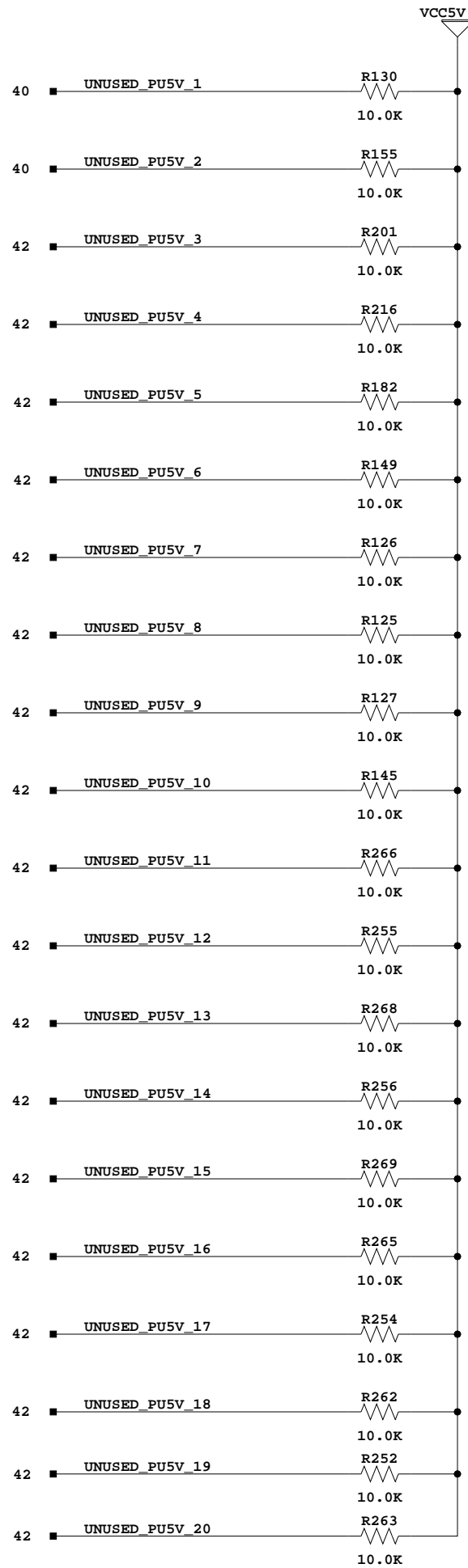
PCI SOUTH BRIDGE, PART 4-5



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
PCI SOUTH BRIDGE, PART 4-5

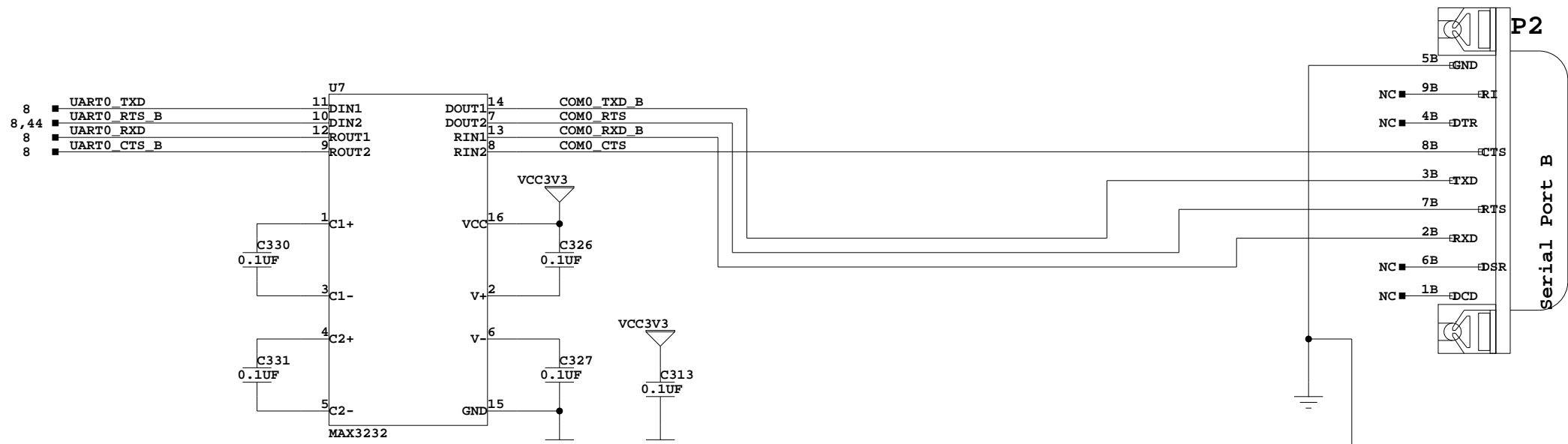
Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	42 of 70	Drawn By	BF



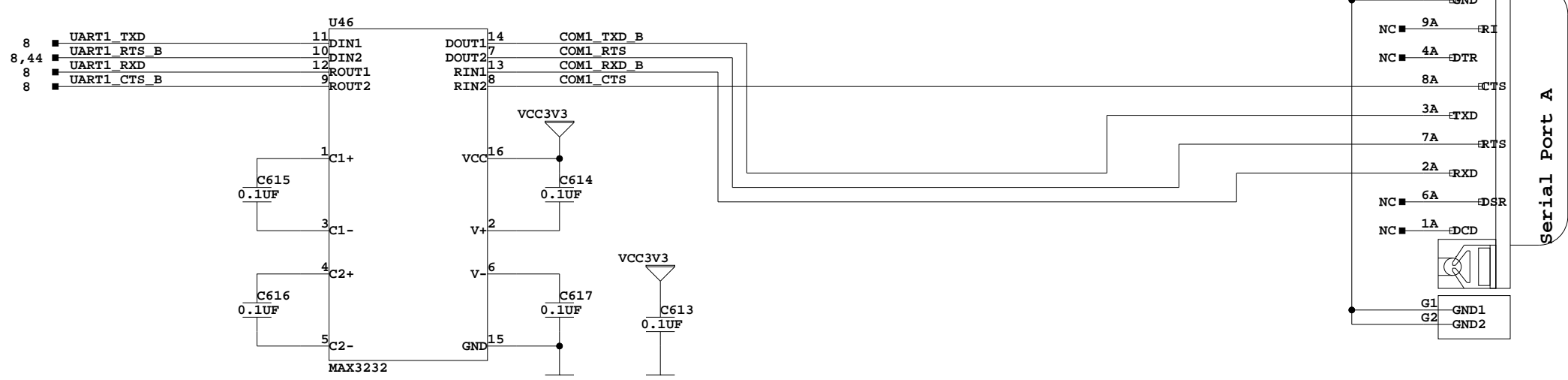
NOTE: AT MODE IS USED HERE TO DISABLE THE SOFTWARE FUNCTIONALITY OF THE SOUTH BRIDGE

PCI SOUTH BRIDGE, CONFIG and UNUSED

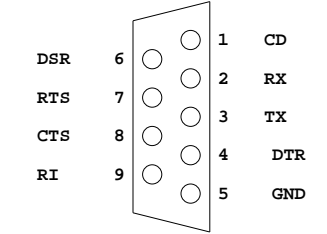
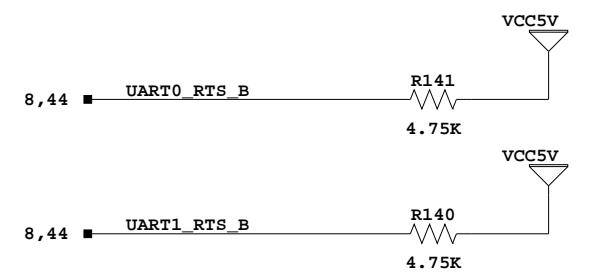
	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOM		
PCI SOUTH BRIDGE, UNUSED PIN RESISTORS		
Date:	7-10-2008_10:19	Ver: C
Sheet Size:	B	Rev: 01
Sheet	43 of 70	Drawn By BF



Silkscreen:
"COM 1"



Silkscreen:
"COM 2"



RS232 DTE PINOUT
CONNECTS TO PC WITH
F/F NULL MODEM CABLE.

LOOKING INTO DB9 PLUG

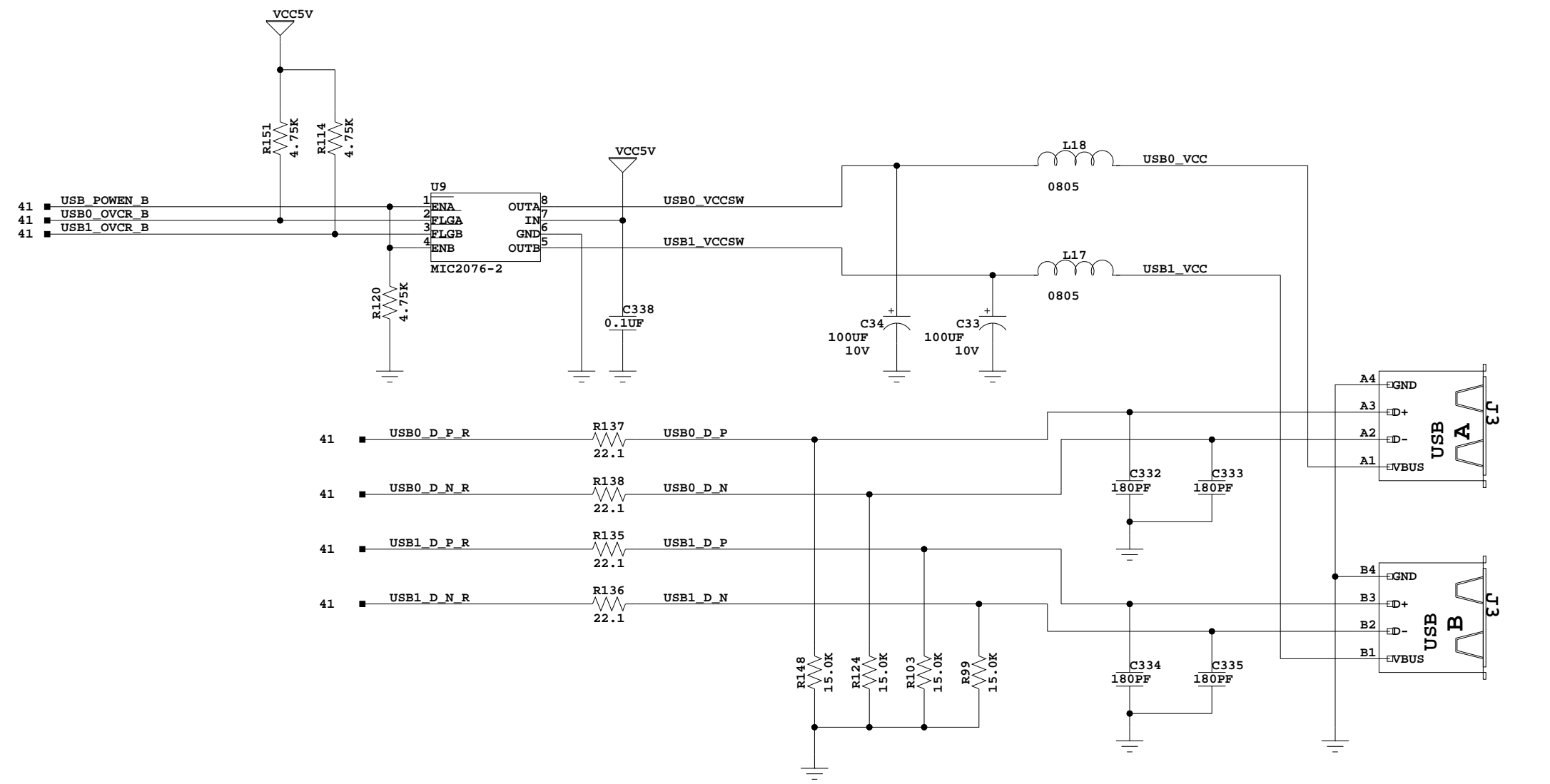
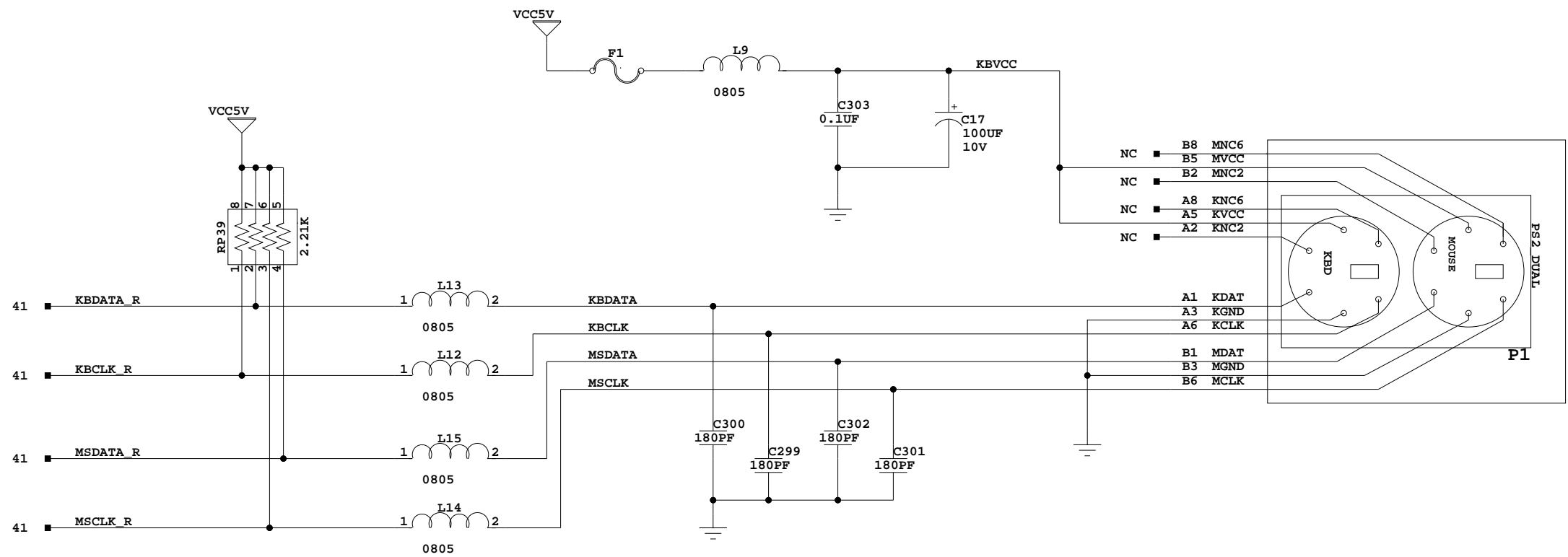
RS232 SERIAL PORT INTERFACE



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTRM
RS232 SERIAL PORT INTERFACE

Date:	7-10-2008_10:19	Ver:	C
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Sheet	44 of 70	Drawn By	BF



KBD/MOUSE AND USB INTERFACES



SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 KBD/MOUSE AND USB INTERFACES

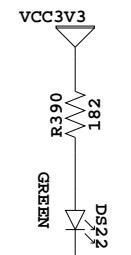
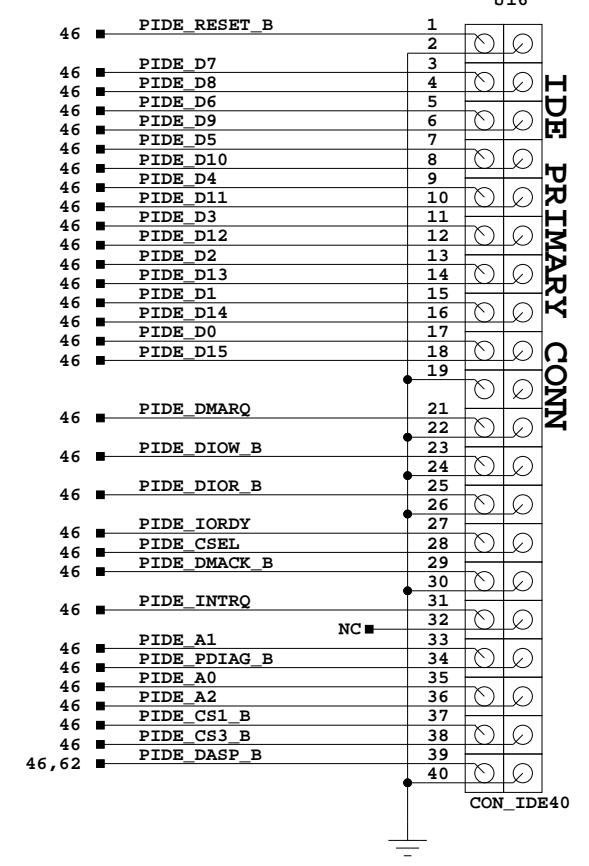
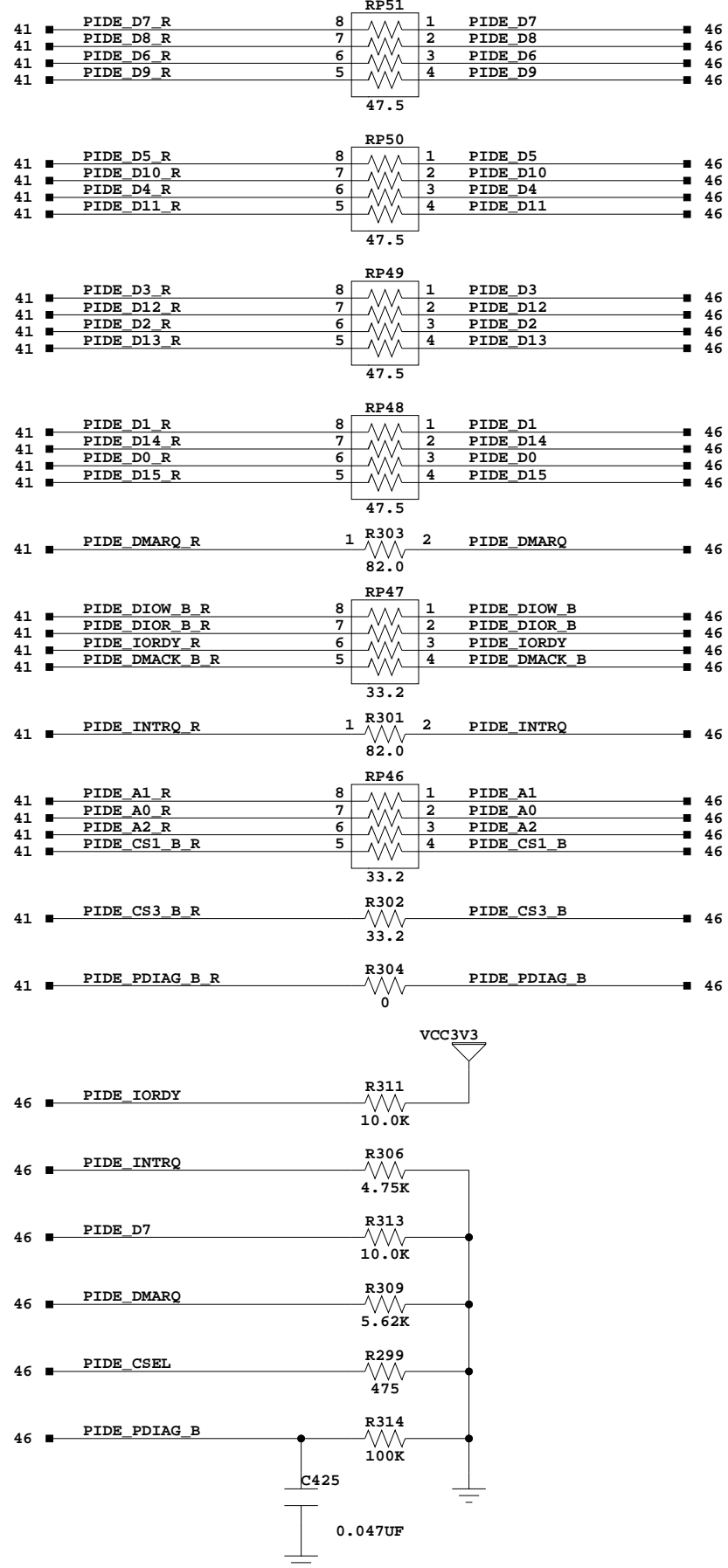
Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	45 of 70	Drawn By	BF

Pin 20 must be removed.
Silkscreen:
"IDE PRIMARY"

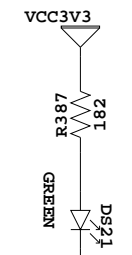
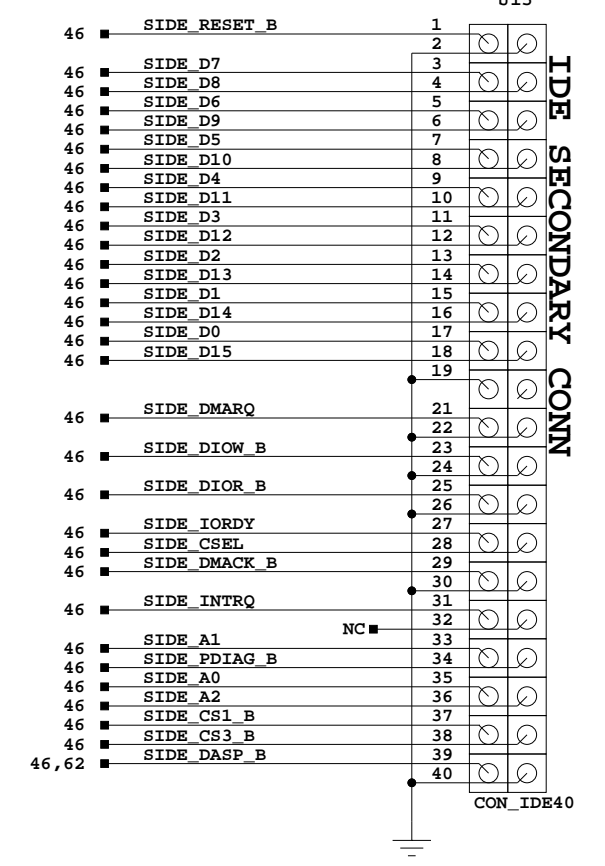
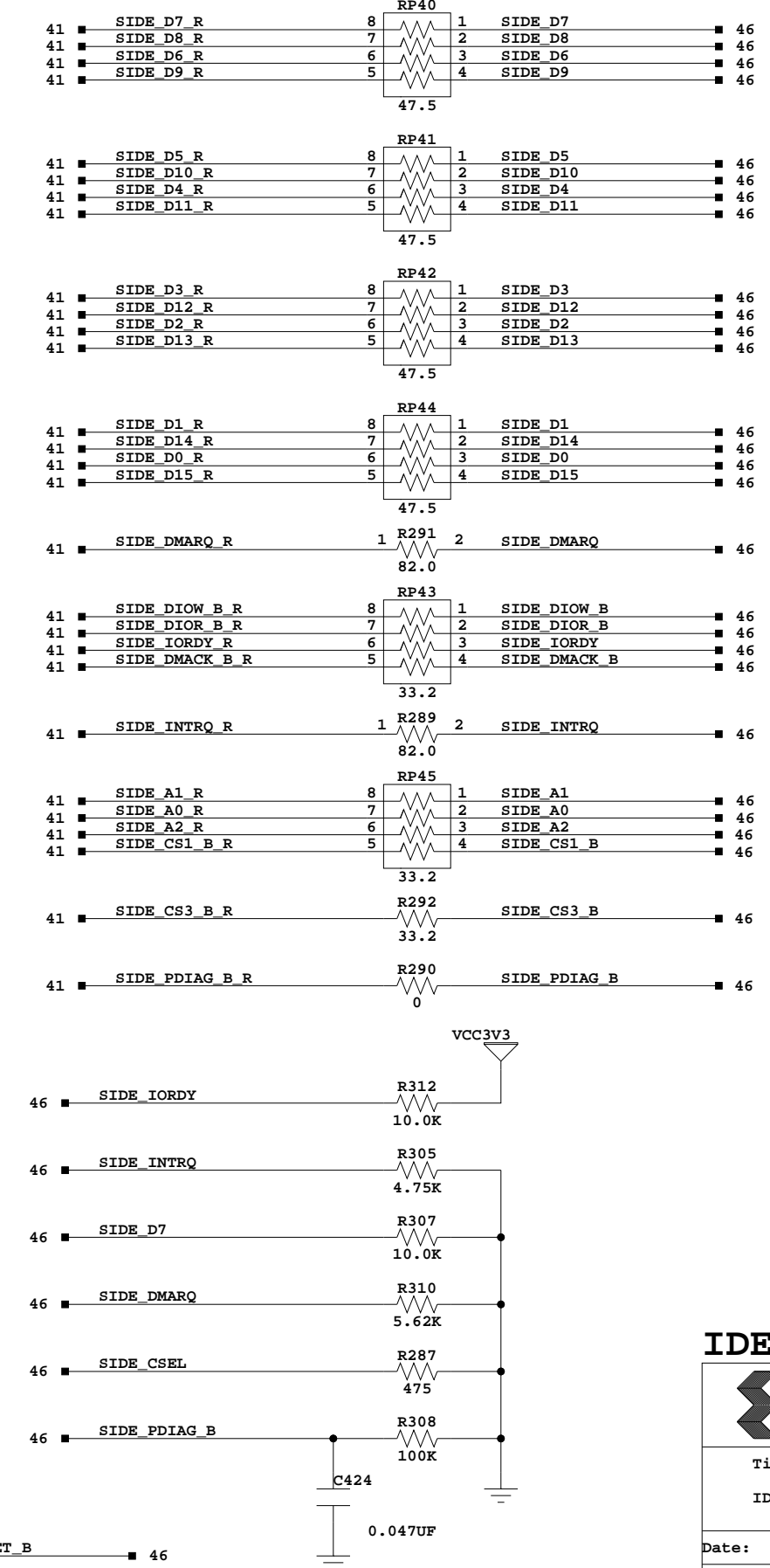
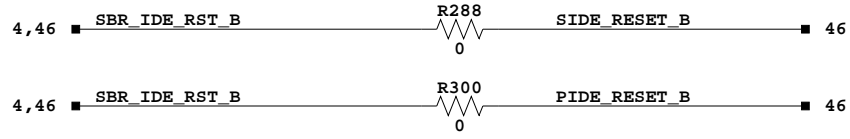
Mark Pin 1
Pin20=Key
J16

Pin 20 must be removed.
Silkscreen:
"IDE SECONDARY"

Mark Pin 1
Pin20=Key
J15



Silkscreen:
"IDE P LED"



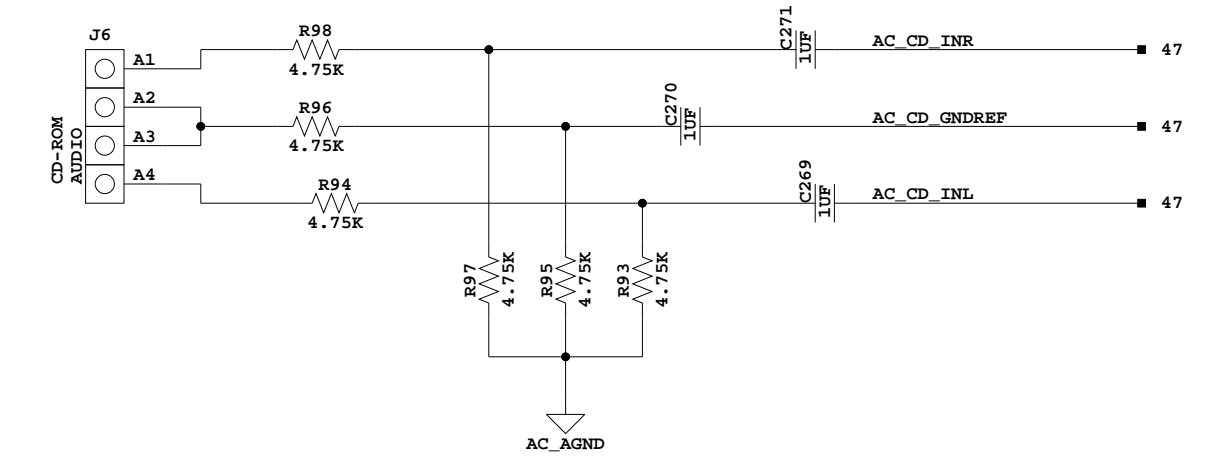
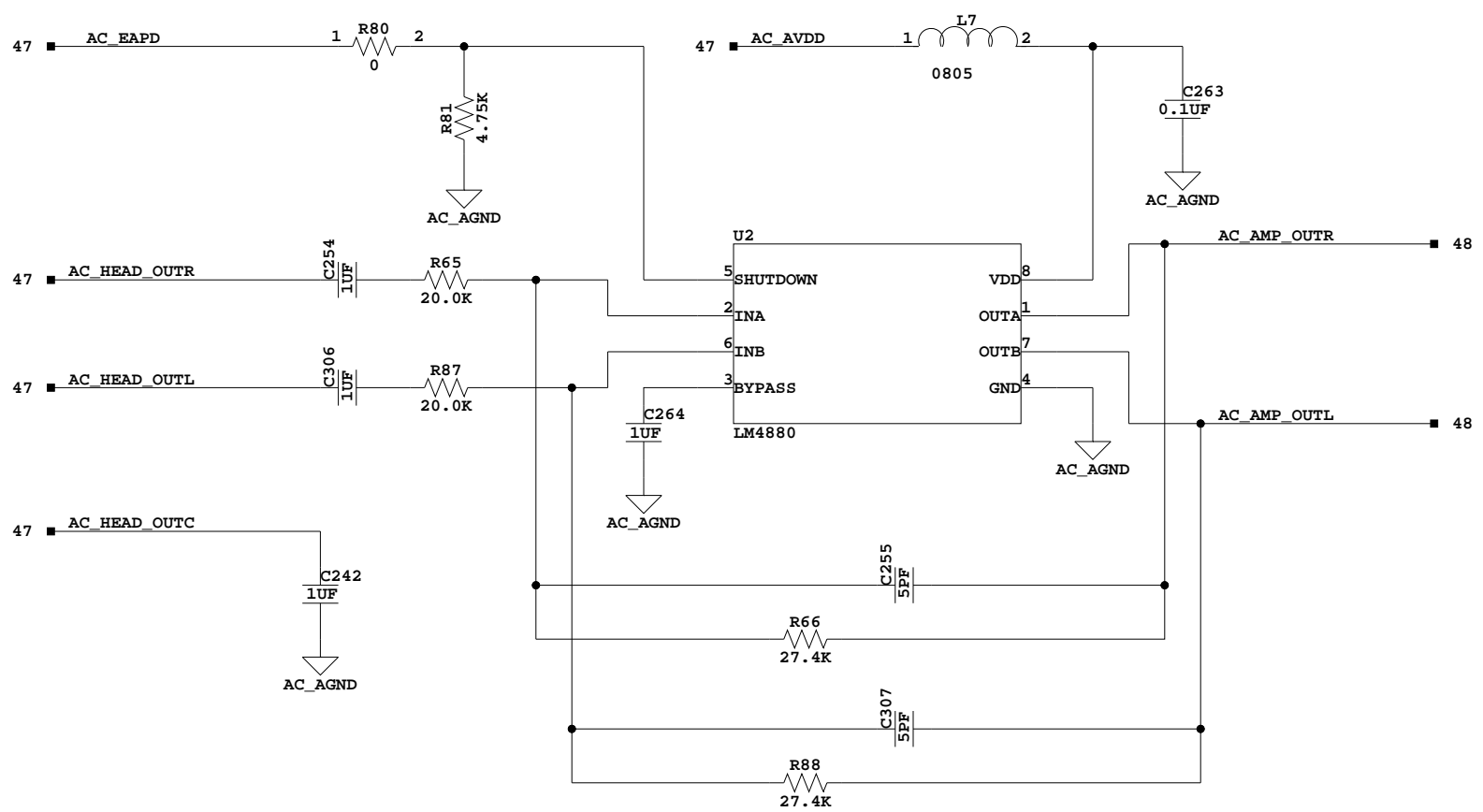
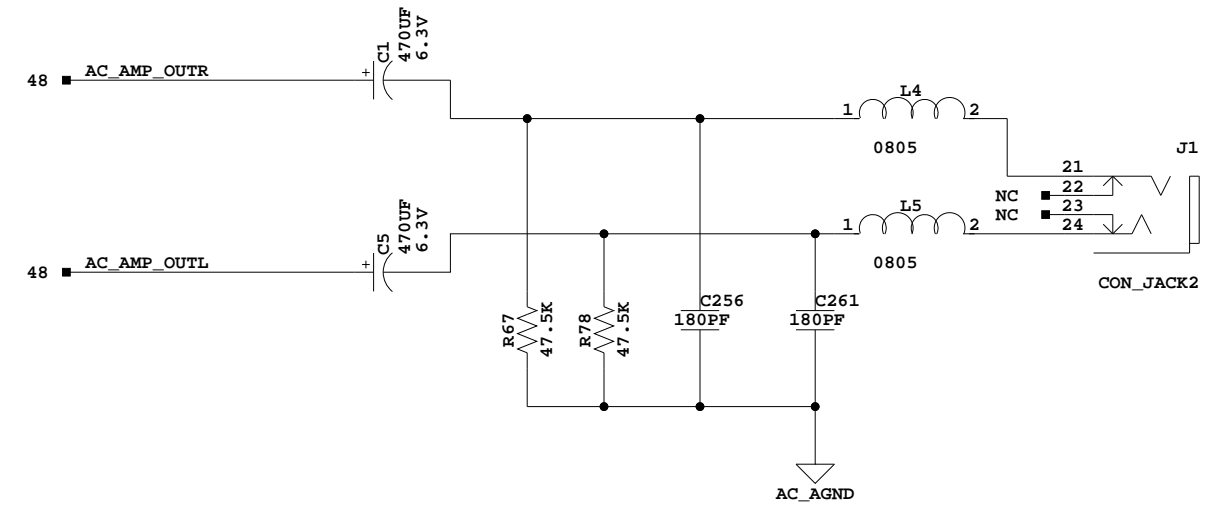
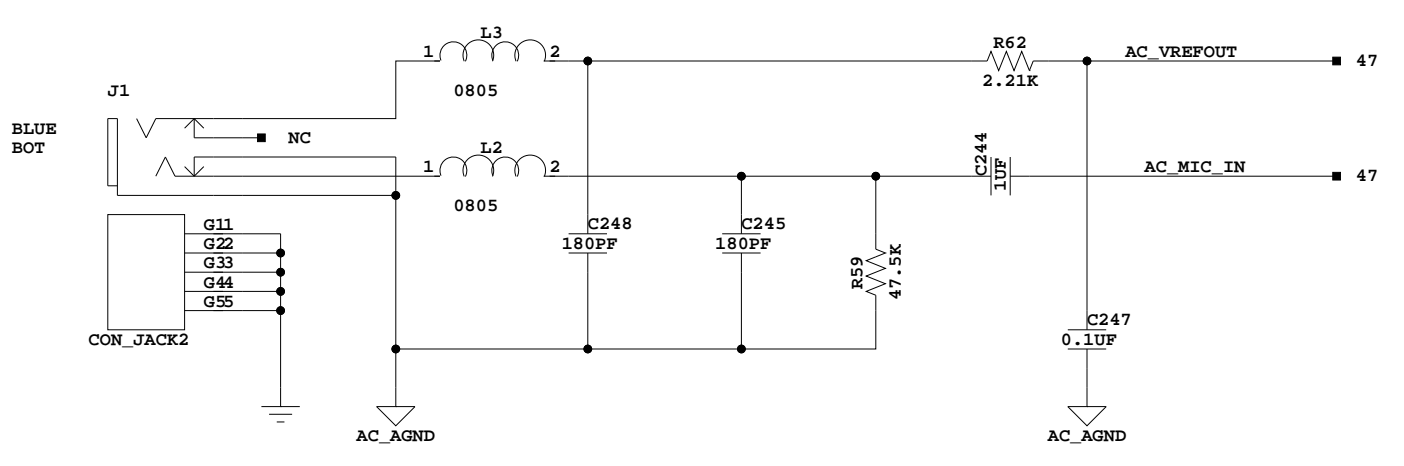
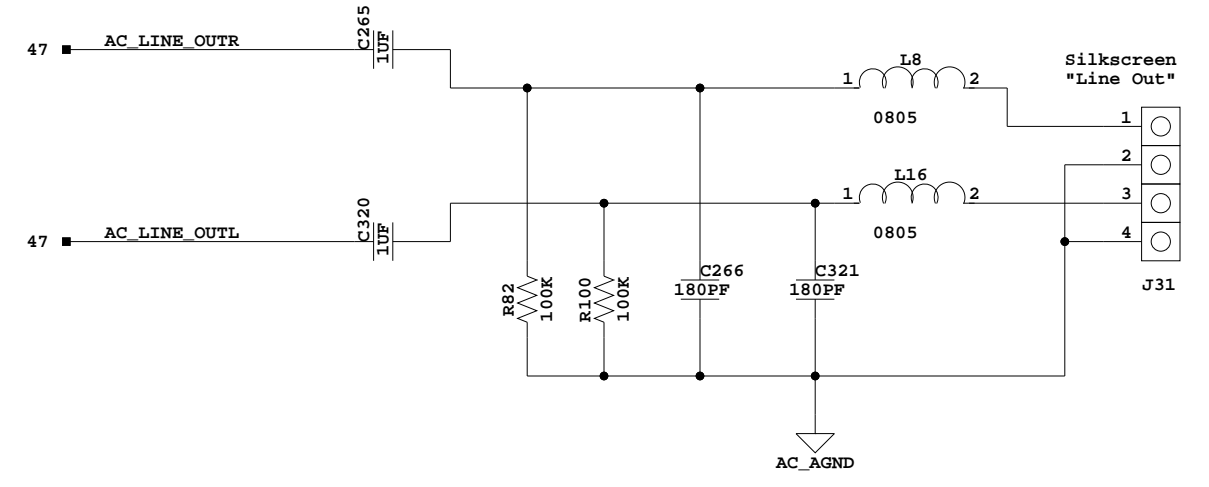
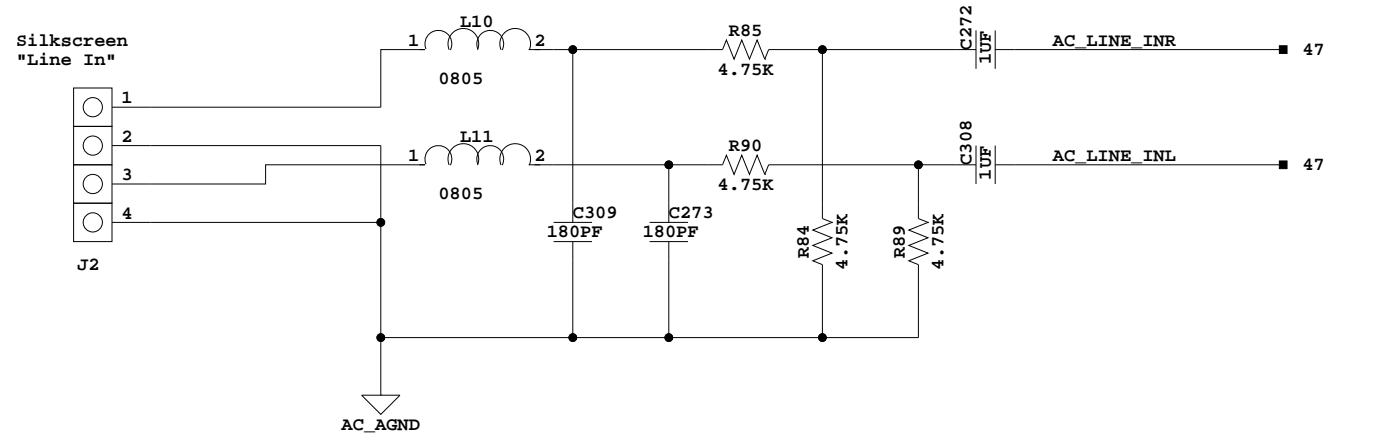
Silkscreen:
"IDE S LED"

IDE INTERFACES



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM IDE INTERFACES	
Date: 7-10-2008_10:19	Ver: C
Sheet Size: B	Rev: 01
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AC97 CONNECTORS

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
AC97 CONNECTORS

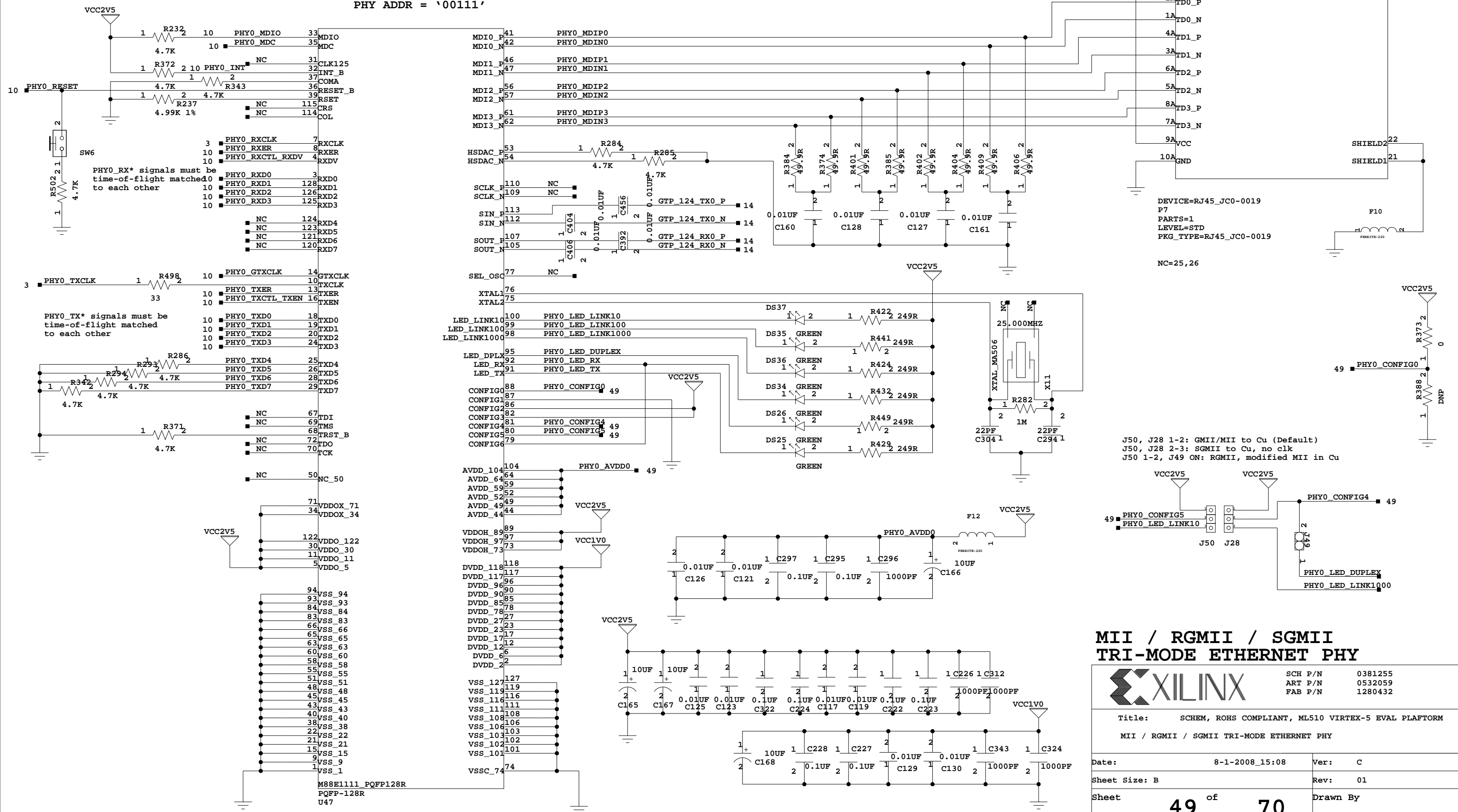
Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	48 of 70	Drawn By	BF

**SGMII:
GTP 124_0**

NOTE:
PHY ADDR = '00111'

NOTE:
BOTTOM SGMII

**10/100/1000
RJ45 AND
MAGNETICS**



DEVICE=RJ45_JC0-0019
P7
PARTS=1
LEVEL=STD
PKG_TYPE=RJ45_JC0-0019
NC=25,26

J50, J28 1-2: GMII/MII to Cu (Default)
J50, J28 2-3: SGMII to Cu, no clk
J50 1-2, J49 ON: RGMII, modified MII in Cu

**MII / RGMII / SGMII
TRI-MODE ETHERNET PHY**



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOM
MII / RGMII / SGMII TRI-MODE ETHERNET PHY

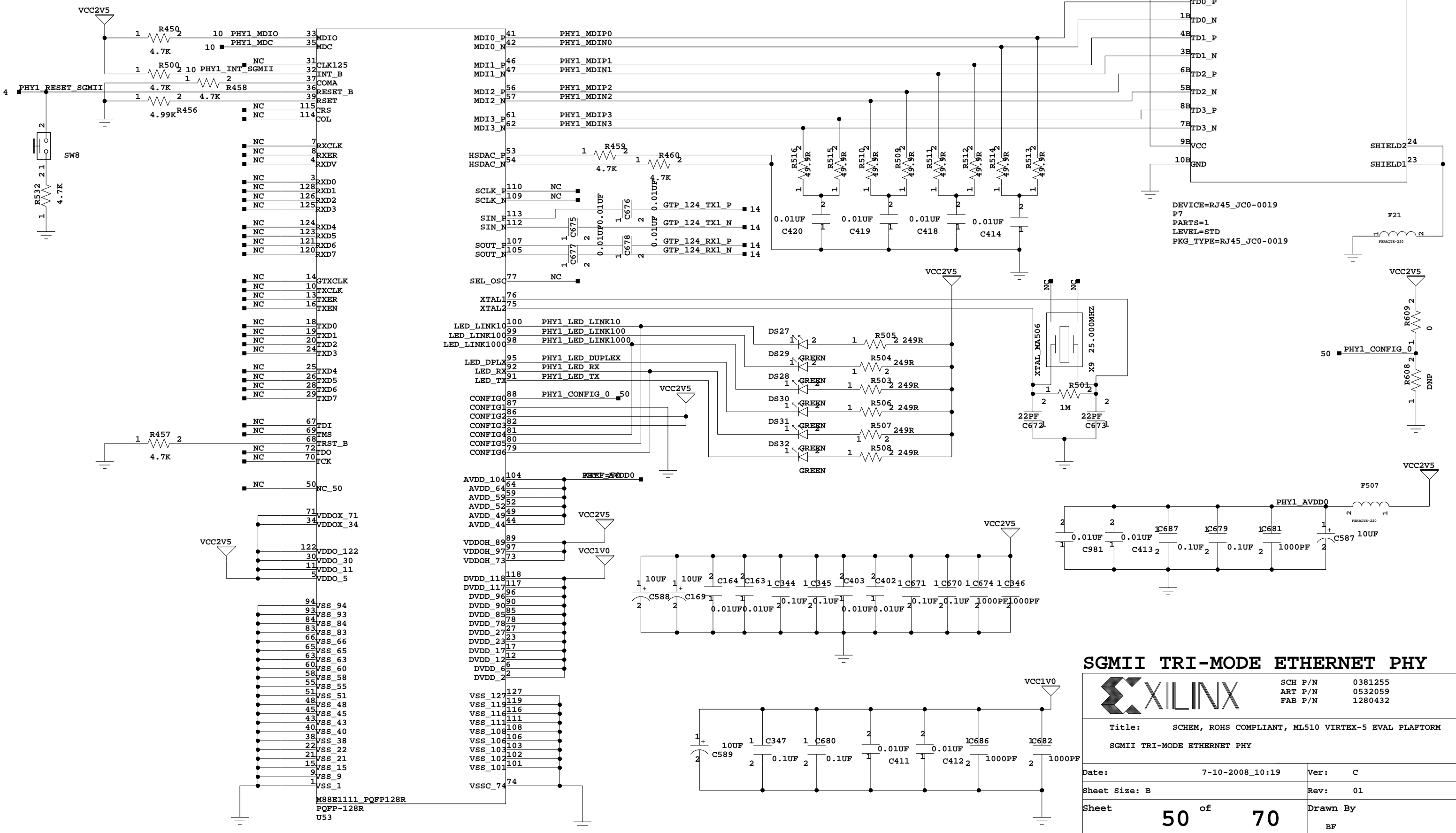
Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	49 of 70	Drawn By	BF

**SGMII:
GTP 124_1**

NOTE:
PHY ADDR = '00111'

NOTE:
BOTTOM SGMII

**10/100/1000
RJ45 AND
MAGNETICS**



DEVICE=RJ45_JC0-0019
P7
PARTS=1
LEVEL=STD
PKG_TYPE=RJ45_JC0-0019

SGMII TRI-MODE ETHERNET PHY



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
SGMII TRI-MODE ETHERNET PHY

Date: 7-10-2008_10:19	Ver: C
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SATA Host 1

GTP 120_1



SATA Host 2

GTP 120_0



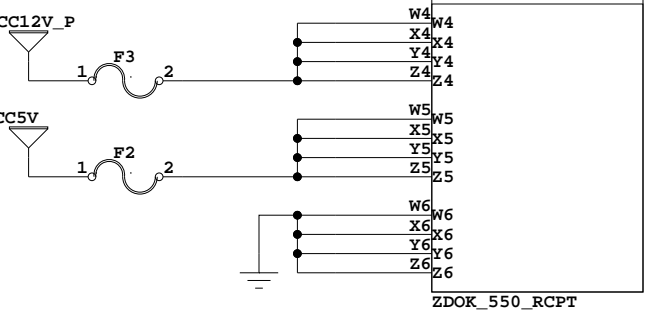
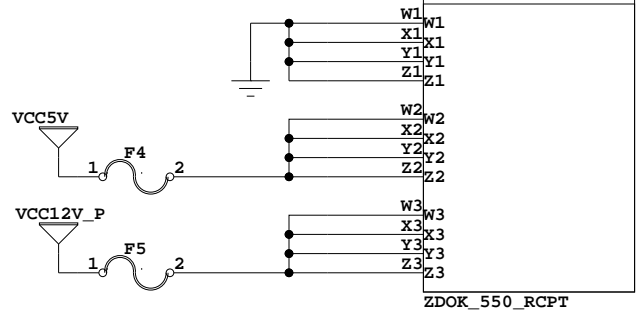
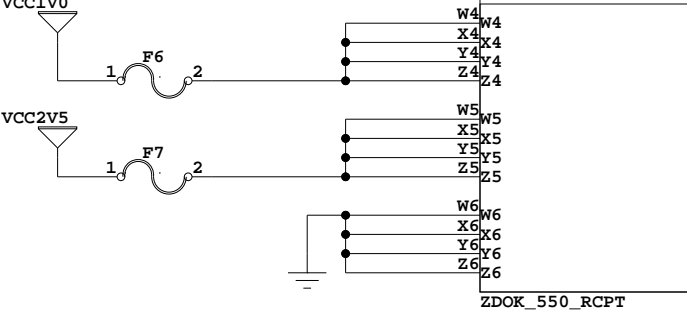
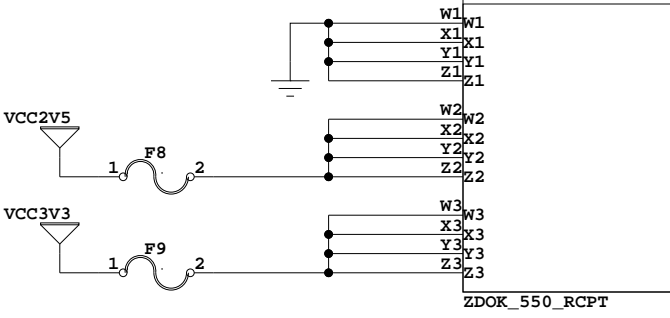
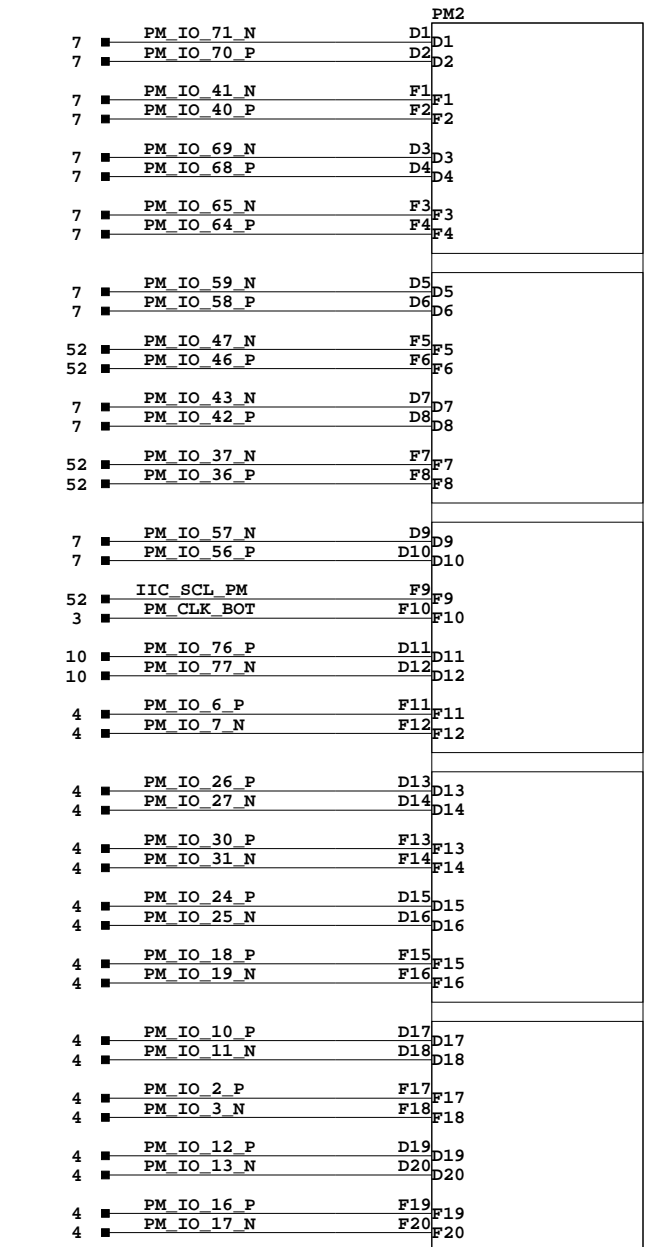
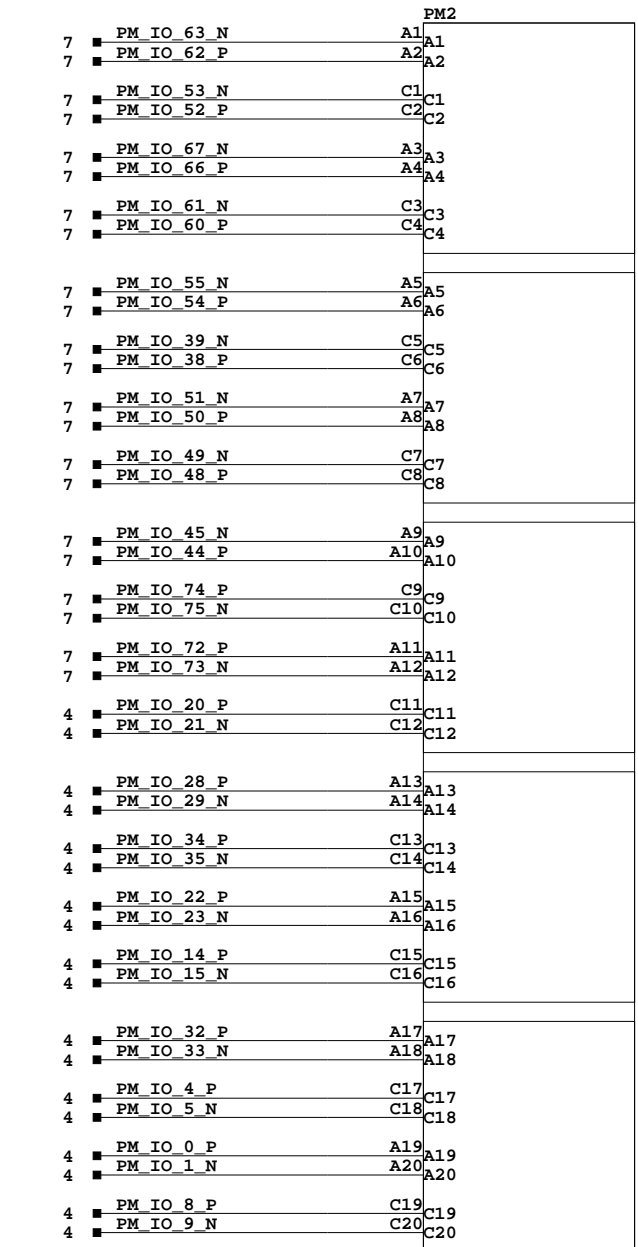
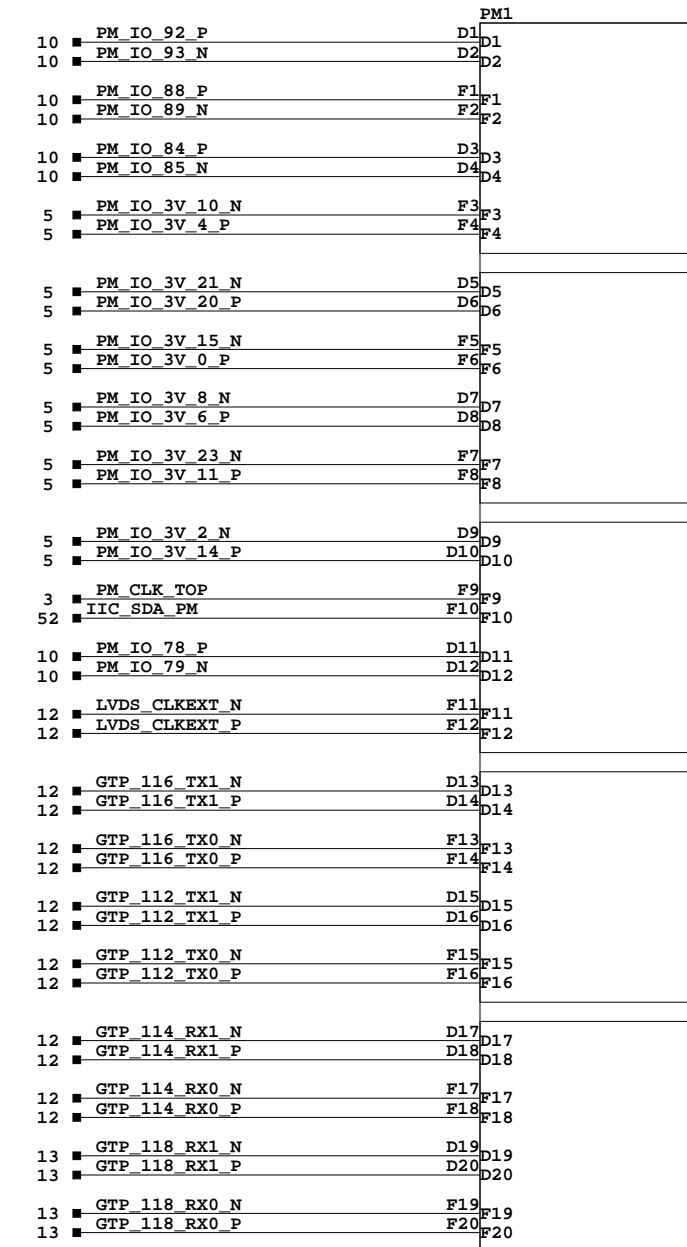
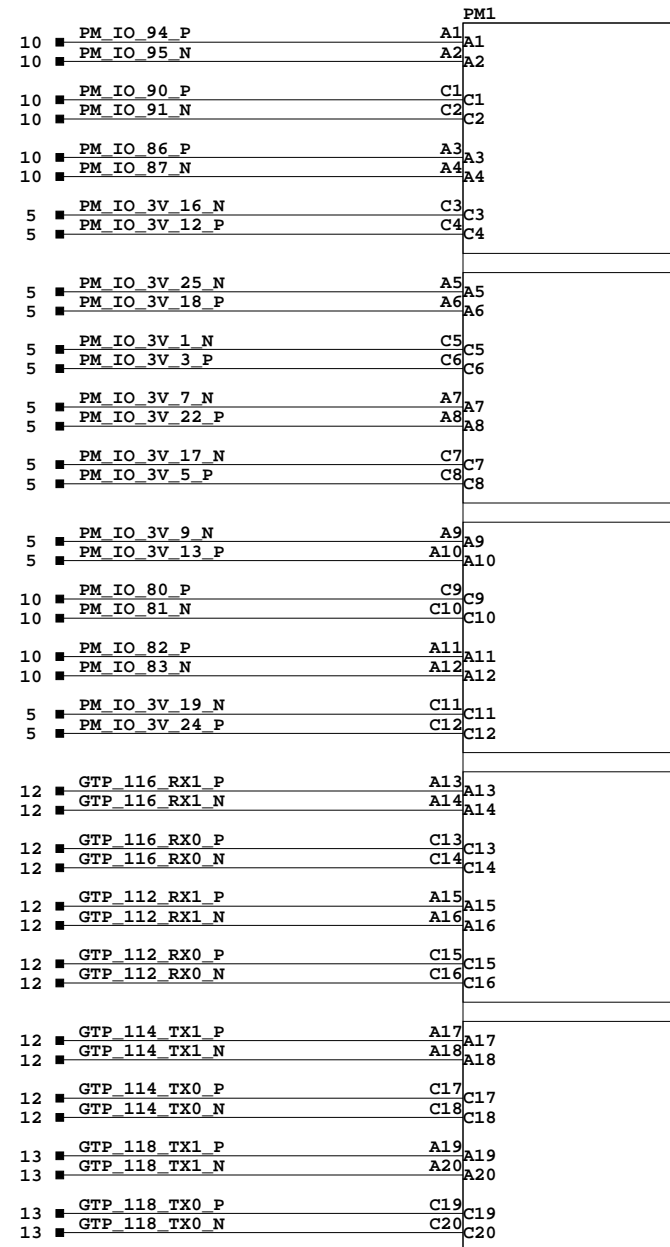
SATA INTERFACE



SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

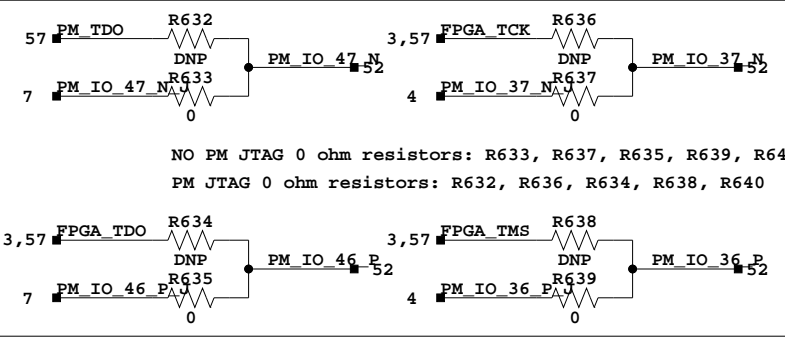
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 SATA INTERFACE

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
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GND;B1, B2, B3, B4, B5
 GND;B6, B7, B8, B9, B10
 GND;B11, B12, B13, B14, B15
 GND;B16, B17, B18, B19, B20
 GND;E1, E2, E3, E4, E5
 GND;E6, E7, E8, E9, E10
 GND;E11, E12, E13, E14, E15
 GND;E16, E17, E18, E19, E20

PM JTAG Resistors



GND;B1, B2, B3, B4, B5
 GND;B6, B7, B8, B9, B10
 GND;B11, B12, B13, B14, B15
 GND;B16, B17, B18, B19, B20
 GND;E1, E2, E3, E4, E5
 GND;E6, E7, E8, E9, E10
 GND;E11, E12, E13, E14, E15
 GND;E16, E17, E18, E19, E20

PERSONALITY MODULE CONNECTORS

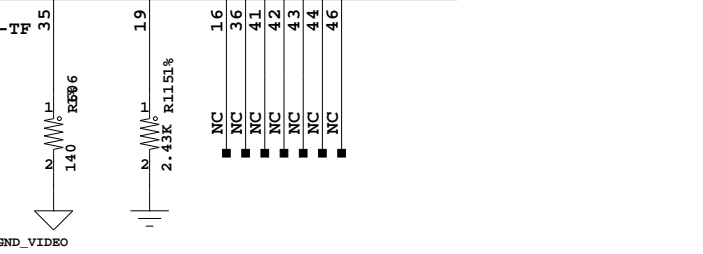
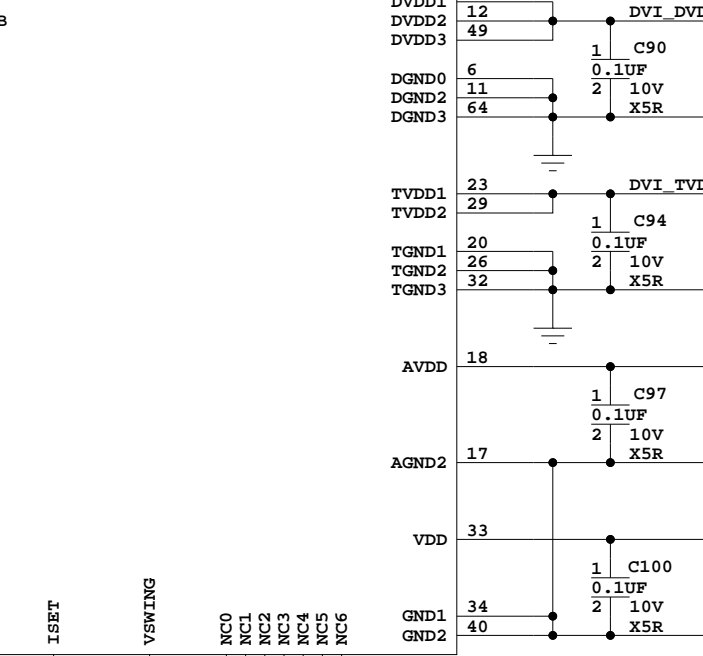
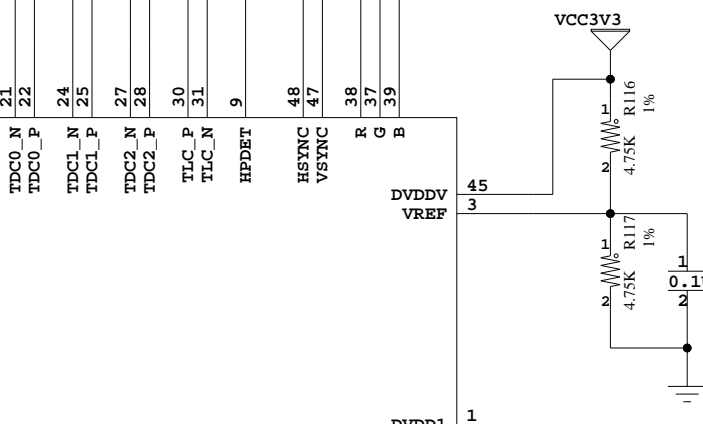
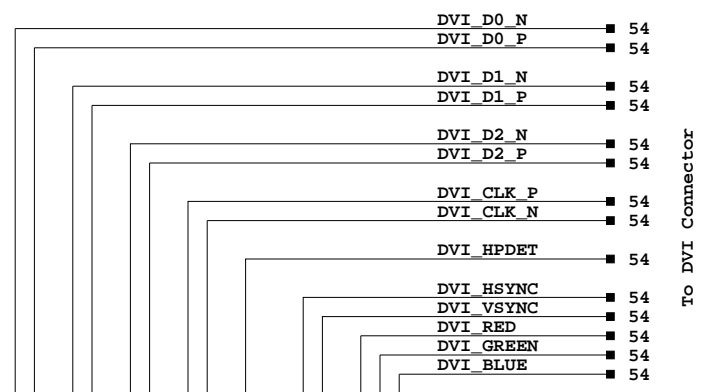
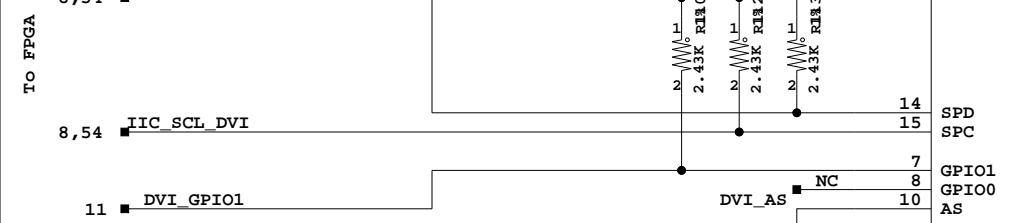
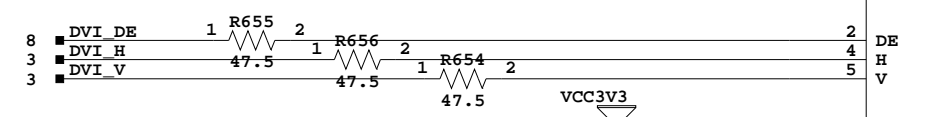
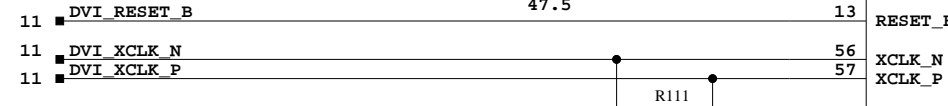
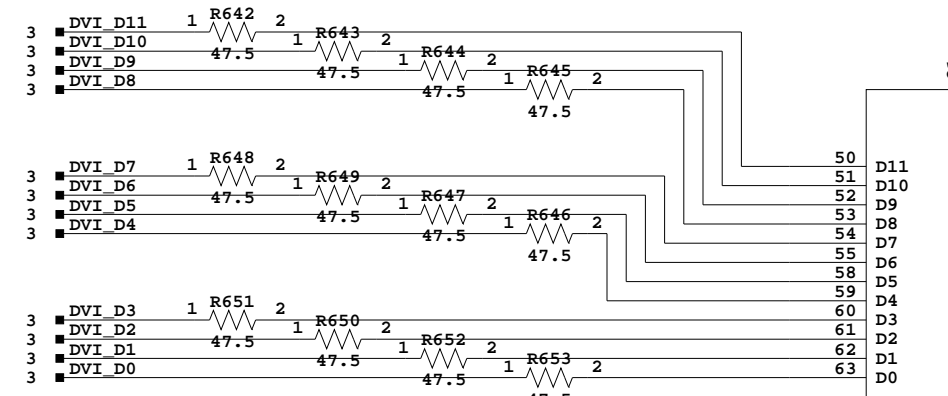


SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 PERSONALITY MODULE CONNECTORS

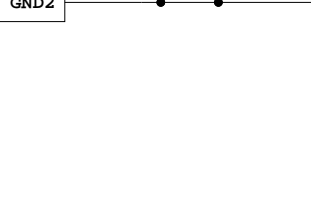
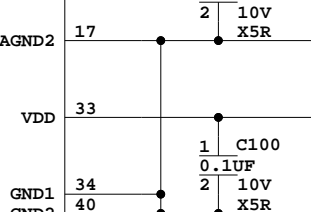
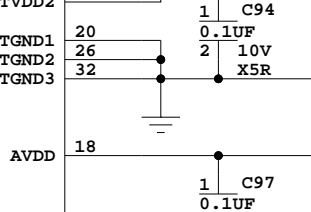
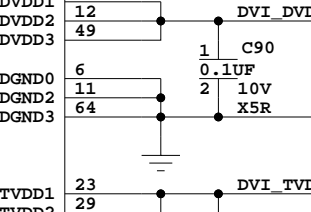
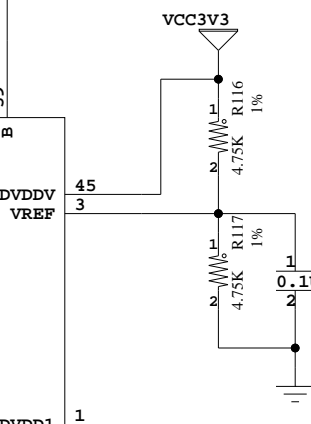
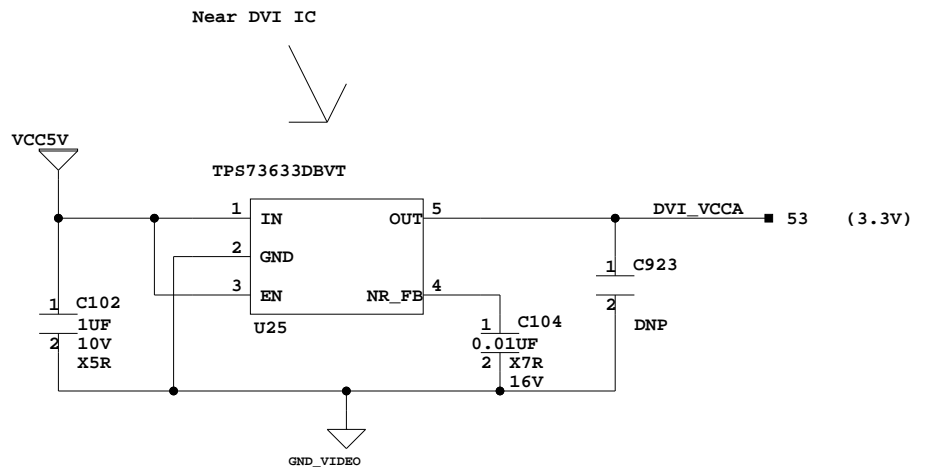
Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
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Place termination RPs near U37



IIC Address = 0x76

To DVI Connector



DVI CODEC



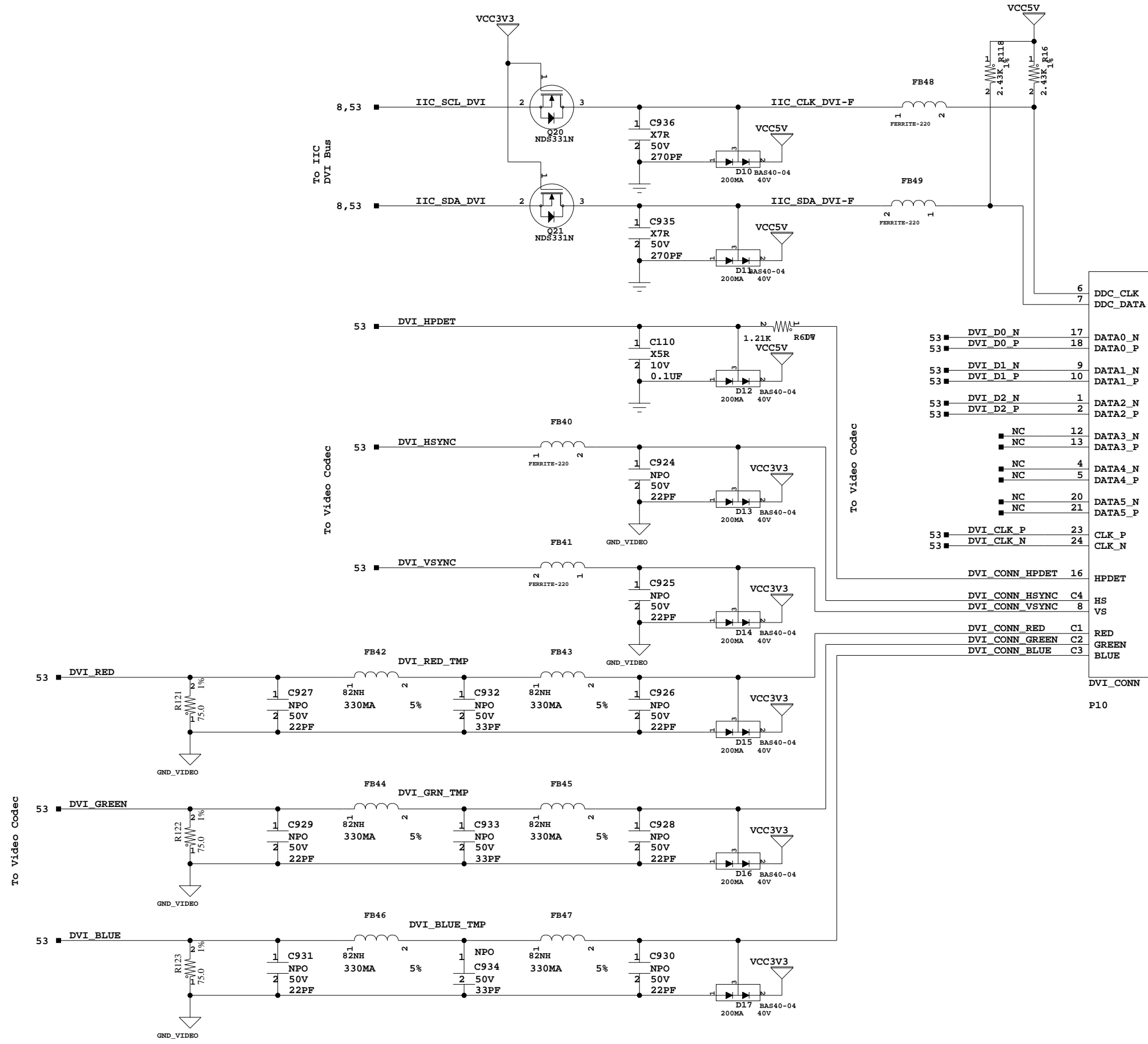
SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 DVI CODEC

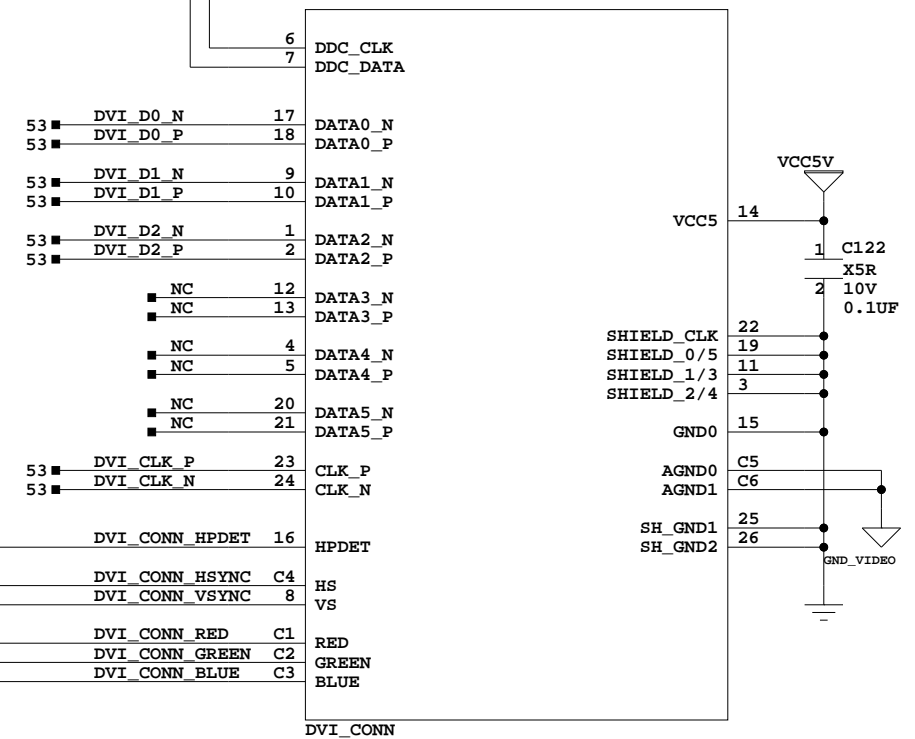
Date: 8-1-2008_15:08 Ver: C

Sheet Size: B Rev: 01

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DVI_CONN



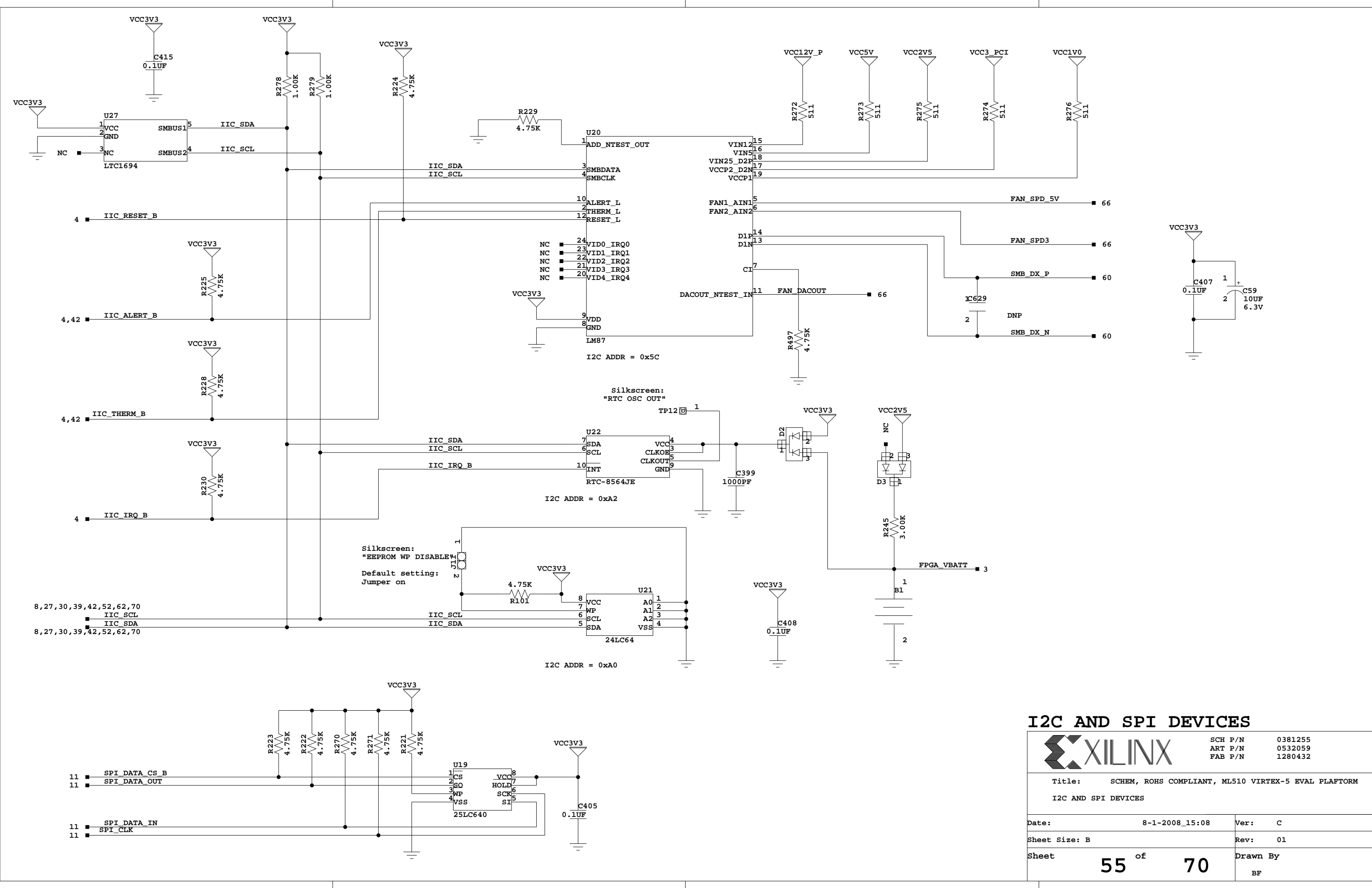
DVI VIDEO CONNECTOR




SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFRTORM
 DVI VIDEO CONNECTOR

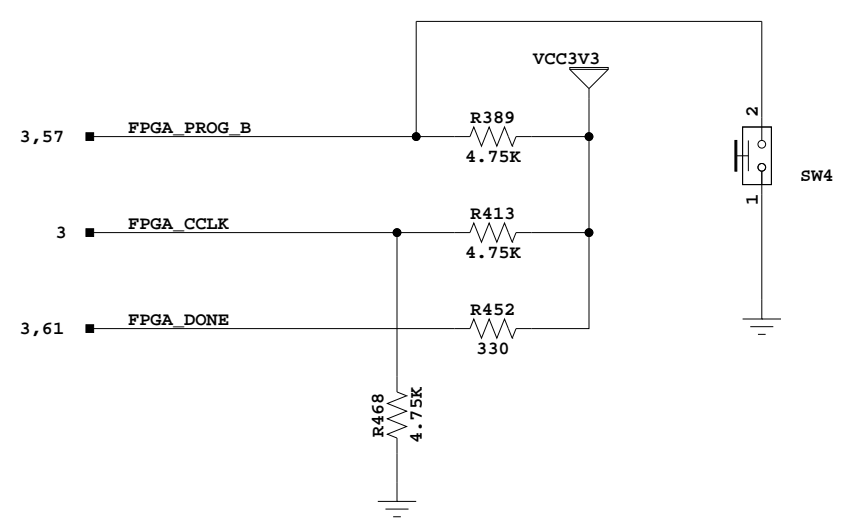
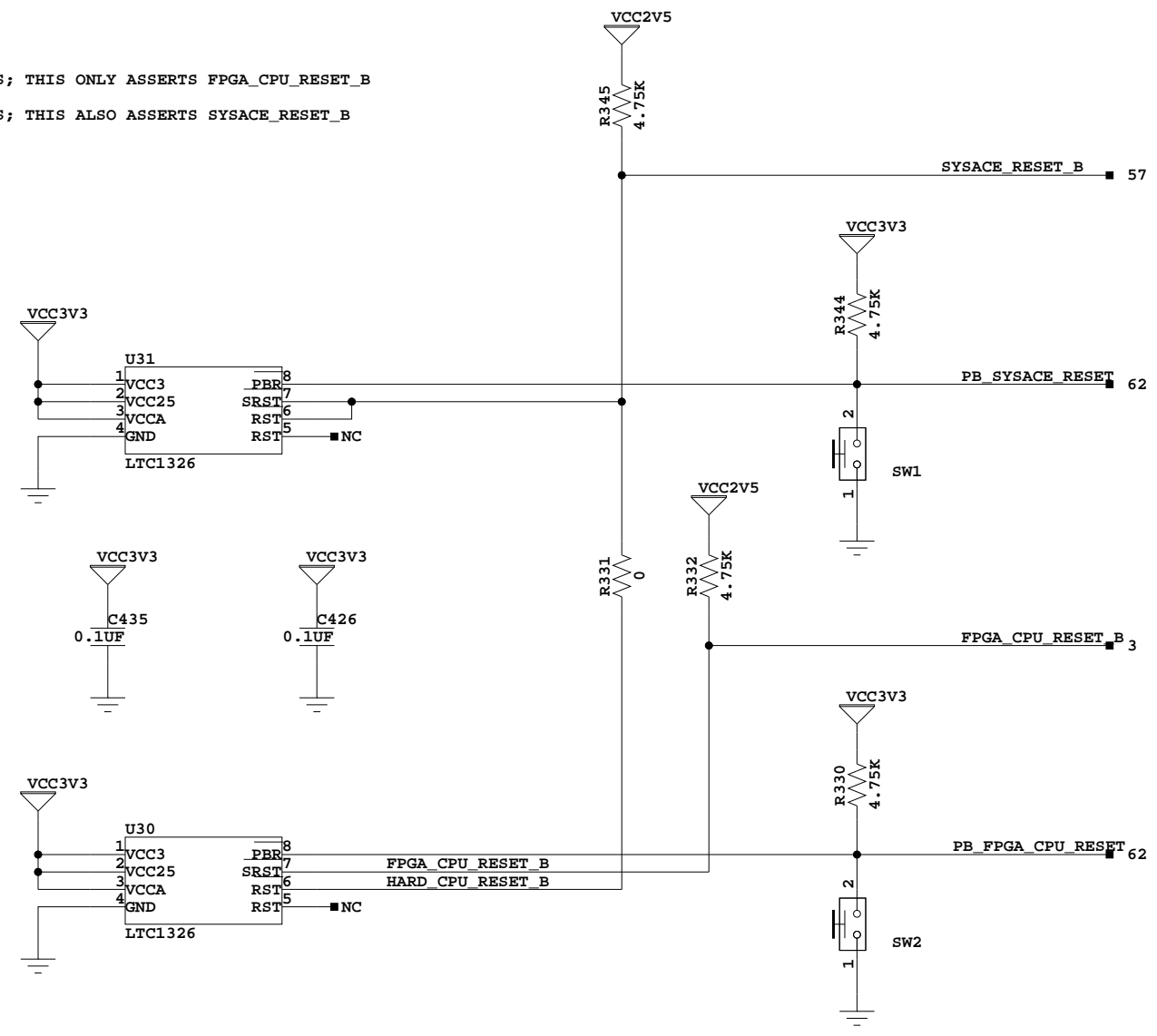
Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	54 of 70	Drawn By	BF



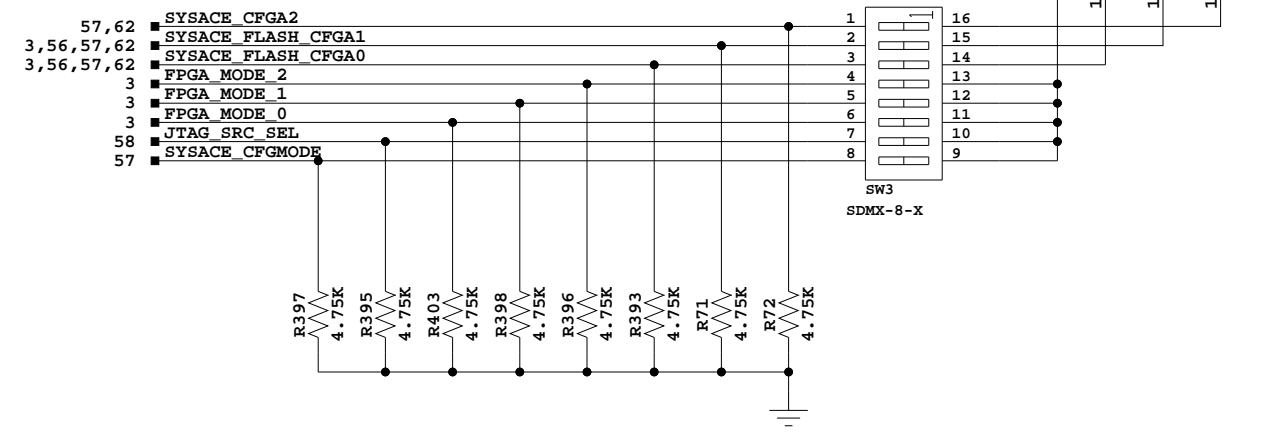
I2C AND SPI DEVICES

		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM I2C AND SPI DEVICES			
Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	55 of 70	Drawn By	BF

IF SW2 PRESSED < 2S; THIS ONLY ASSERTS FPGA_CPU_RESET_B
 IF SW2 PRESSED > 2S; THIS ALSO ASSERTS SYSACE_RESET_B

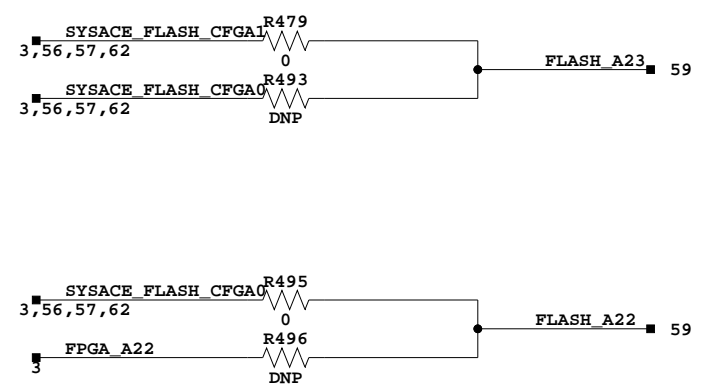


Strong pullups required because RS drives 0
 During Fallback configuration mode



BPI Flash Addressing Scheme					
	FPGA (U37) BPI Addr Pin	Schematic Net Name	Net Connection After Jumpering	Parallel Flash (U43) Addr Pin	
4 x 64 Mbit Revisions	RS1 (U37.AK12)	SYSAC_FLASH_CFG1	FLASH_A23	R479-0ohm; R493-DNP	A24 (U43.26)
	RS0 (U37.AK13)	SYSAC_FLASH_CFG0	FLASH_A22	R495-0ohm; R496-DNP	A23 (U43.9)
	A22 (U37.AK14)	FPGA_A22	no connect		no connect
2 x 128 Mbit Revisions	RS1 (U37.AK12)	SYSAC_FLASH_CFG1	no connect	R479-DNP; R493-0ohm	no connect
	RS0 (U37.AK13)	SYSAC_FLASH_CFG0	FLASH_A23	R495-DNP; R496-0ohm	A24 (U43.26)
	A22 (U37.AK14)	FPGA_A22	FLASH_A22		A23 (U43.9)
Any Address Mode	A[21:0] (U37)	FLASH_A[21:0]	FLASH_A[21:0] N/A		A[22:1] (U43)

Note: See the ML510 User Guide for more details about BPI Flash



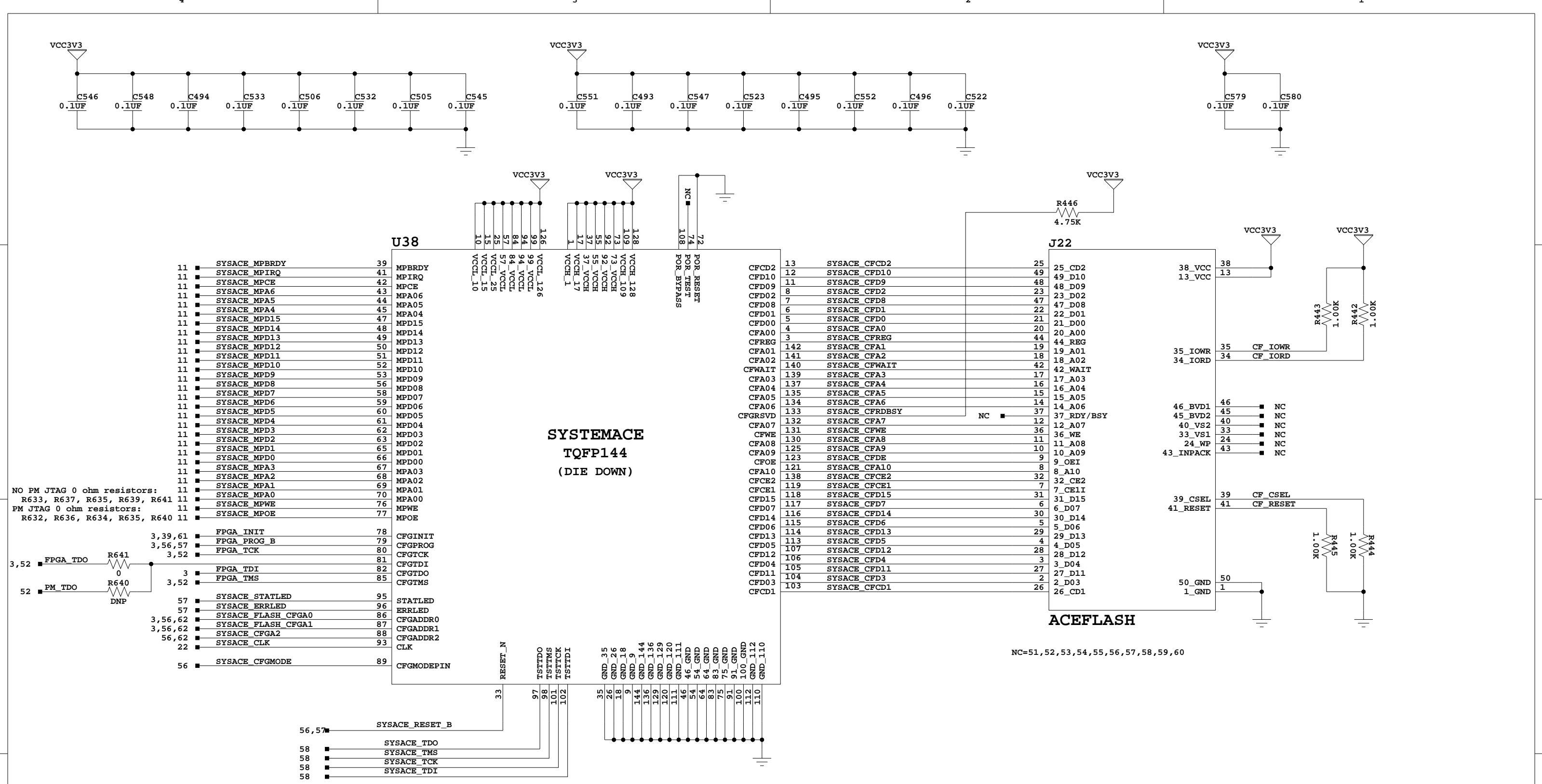
FPGA CONFIG, RESET, AND MISC I/O



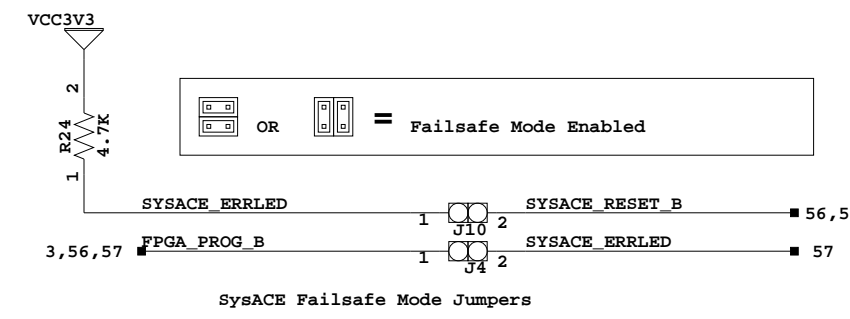
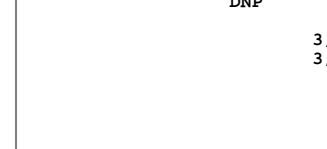
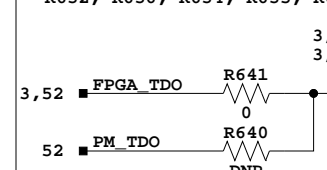
SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 FPGA CONFIG, RESET, AND MISC I/O

Date:	7-10-2008_10:19	Ver:	C
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NO PM JTAG 0 ohm resistors:
R633, R637, R635, R639, R641
PM JTAG 0 ohm resistors:
R632, R636, R634, R635, R640



SYSTEM ACE AND COMPACT FLASH



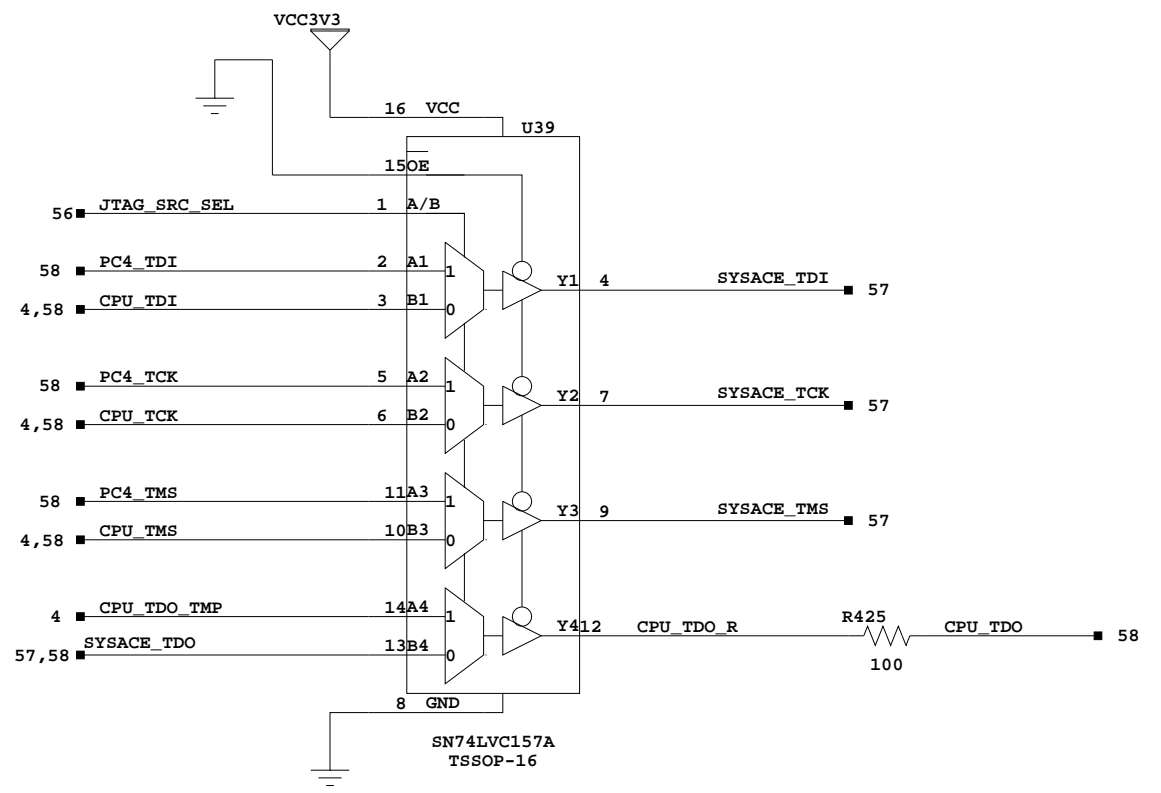
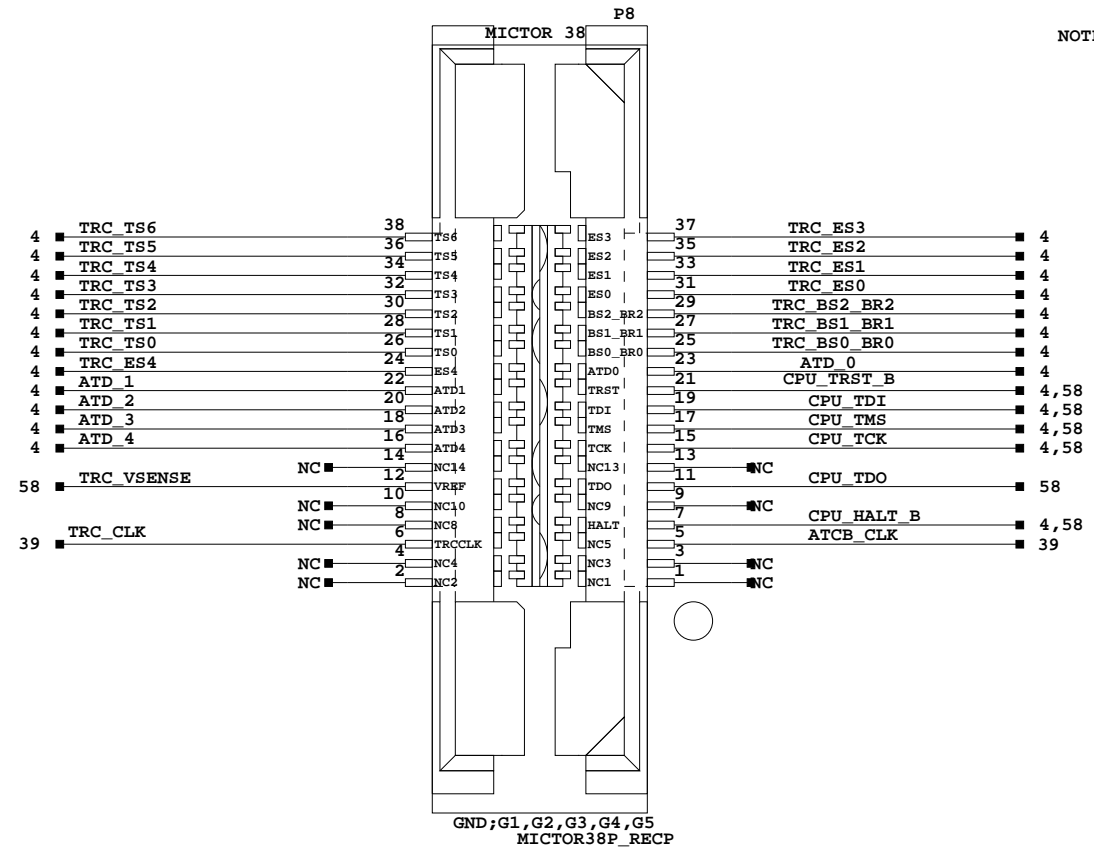
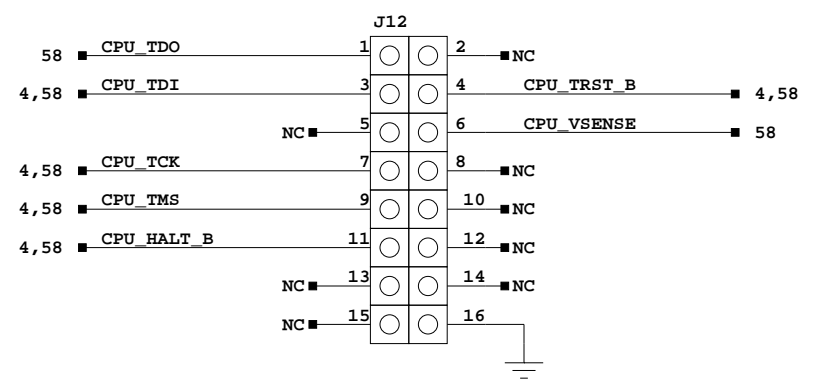
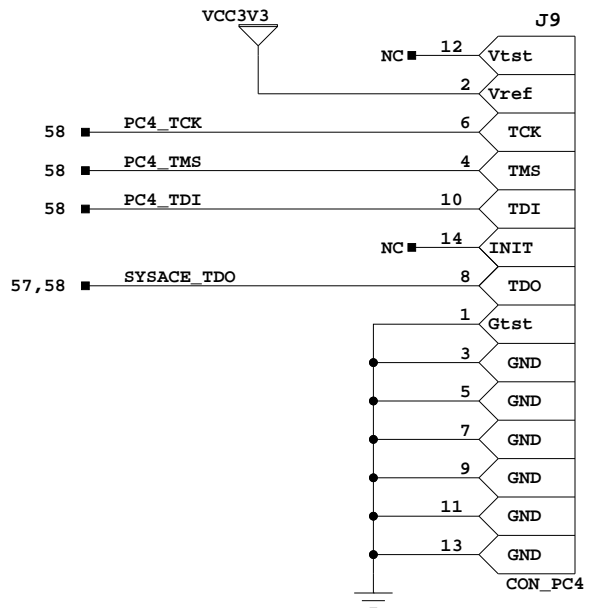
SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOM
SYSTEM ACE AND COMPACT FLASH

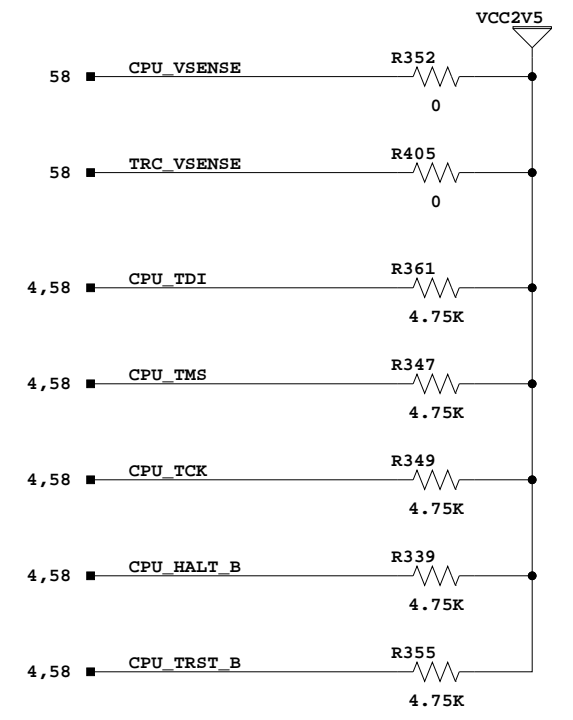
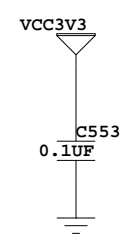
Date: 7-10-2008_10:19 Ver: C

Sheet Size: B Rev: 01

Sheet 57 of 70 Drawn By BF



NOTE: THIS MUX INTRODUCES AN IMPLICIT 2.5V TO 3.3V LEVEL-SHIFT FOR THE CPU JTAG SIGNALS. THE SERIES RESISTOR ON CPU_TDO IS INTENDED TO PROVIDE PROTECTION FOR A 2.5V JTAG PROBE.



JTAG, DEBUG, TRACE CONNECTORS

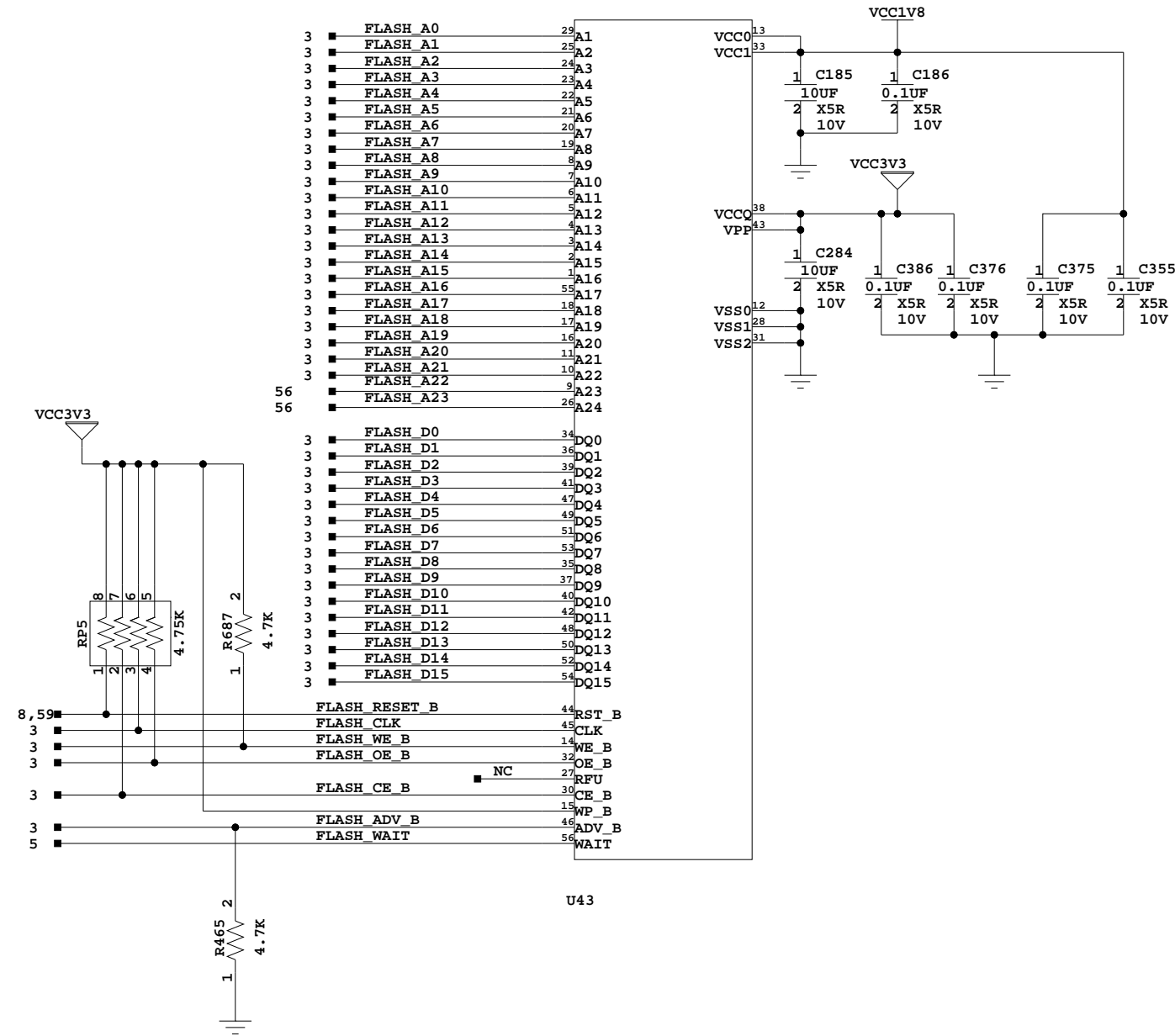


SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

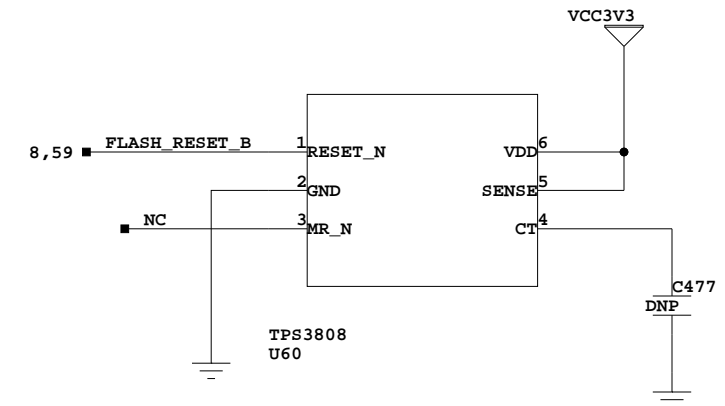
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
JTAG, DEBUG, TRACE CONNECTORS

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	58 of 70	Drawn By	BF

Silkscreen:
"Strata FLASH"
"256 MBit"



Programmable-Delay Supervisor Circuit



$$\langle \text{Cap Value in nF} \rangle = (((\langle \text{DELAY in S} \rangle) - (0.5 * 0.001)) * 175)$$

SYNC. SRAM FLASH

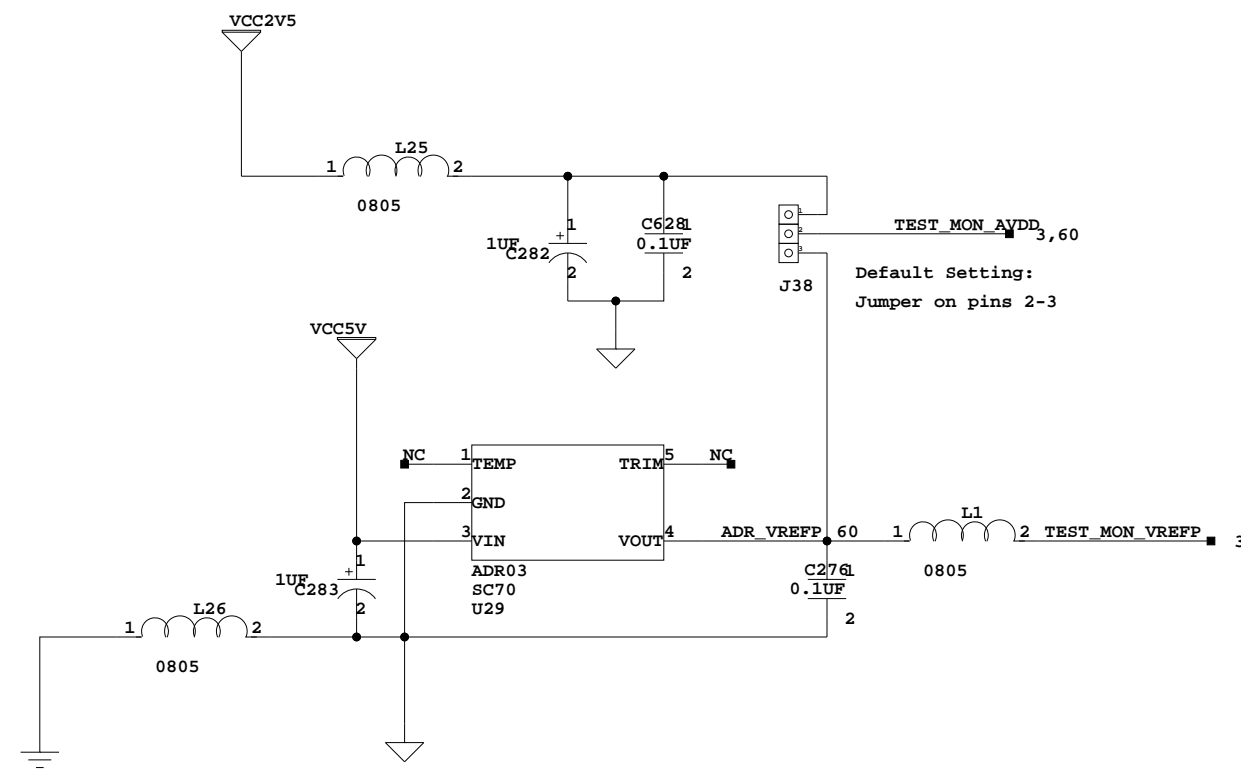


SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

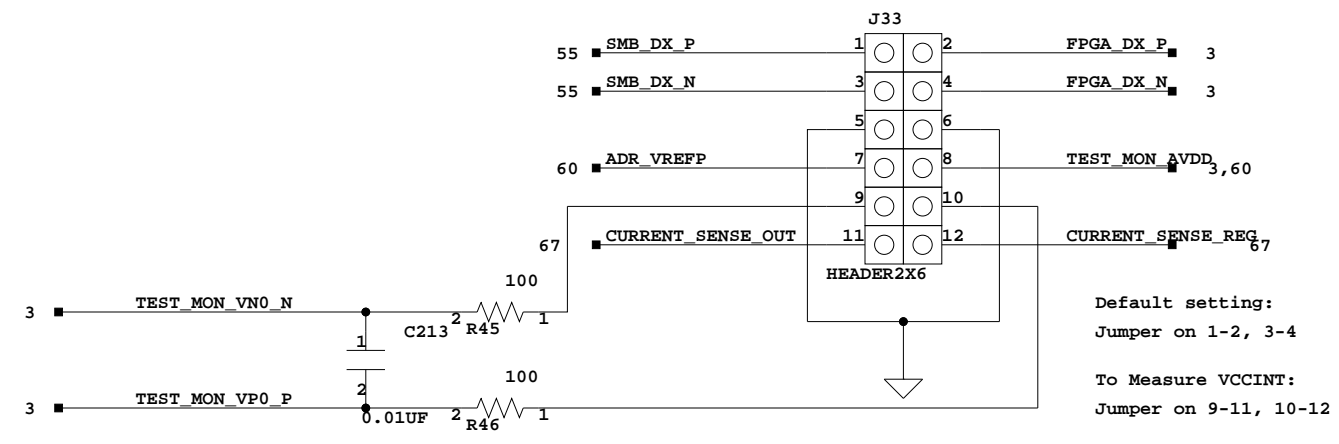
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFRTORM

SYNC. SRAM FLASH

Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	59 of 70	Drawn By	BF



System Monitor Header for probing



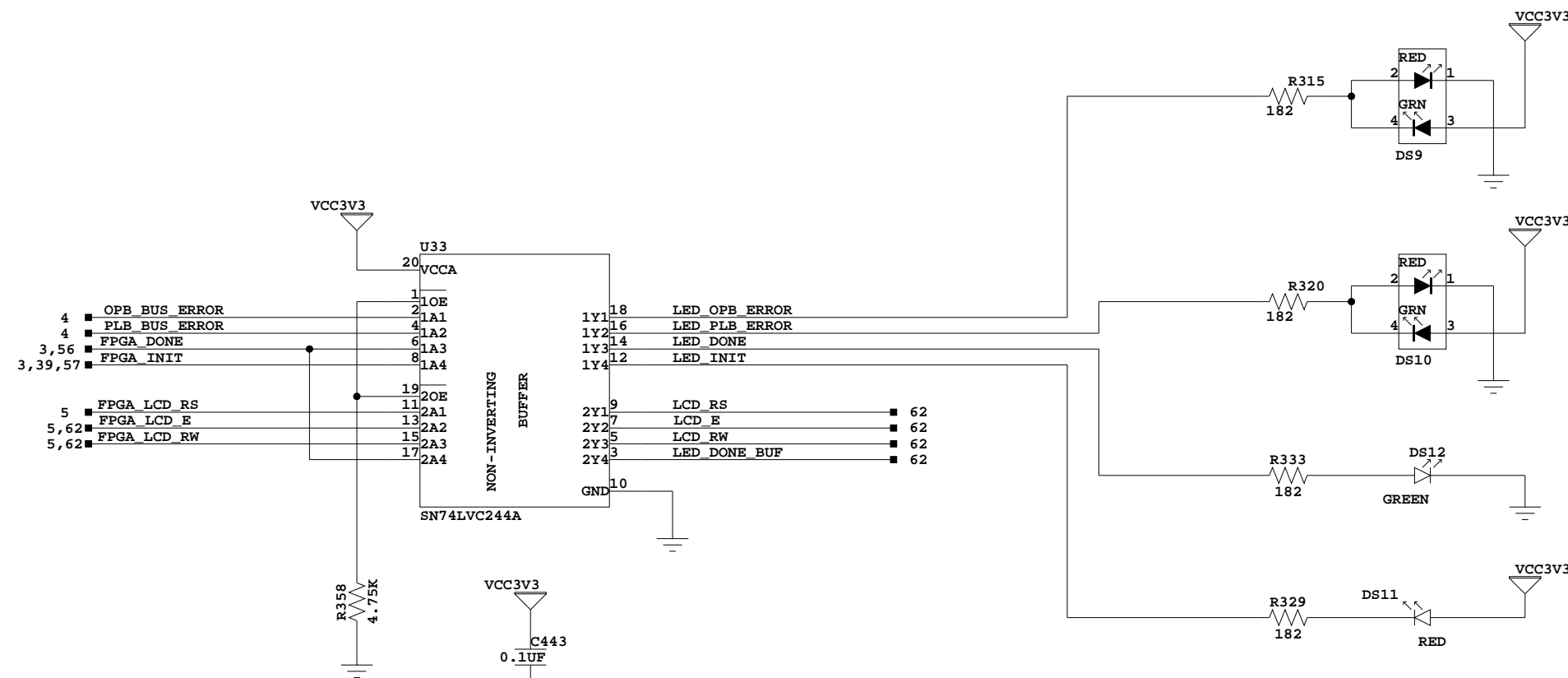
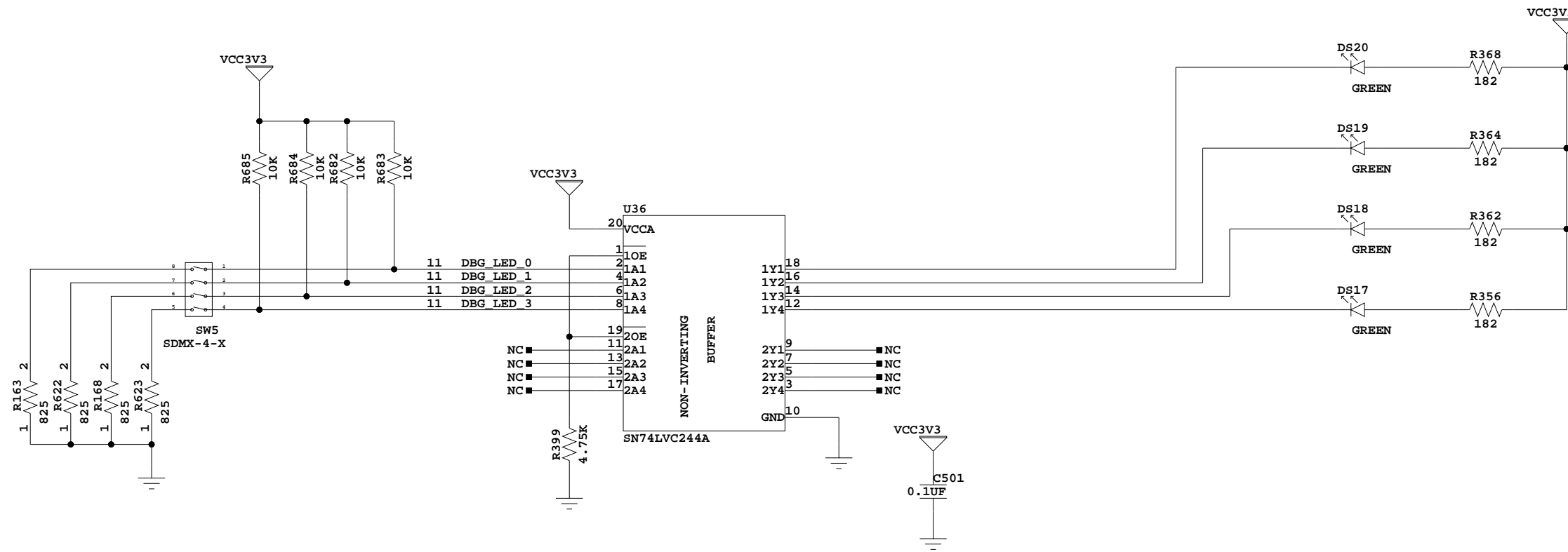
place 100 ohm resistors and 0.01 cap near FPGA

SYSMON HEADER / AVDD VREFP SUPPLY

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 SYS MONITOR HEADER / FPGA AVDD VREFP SUPPLY

Date:	8-1-2008_15:09	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	60 of 70	Drawn By	BF

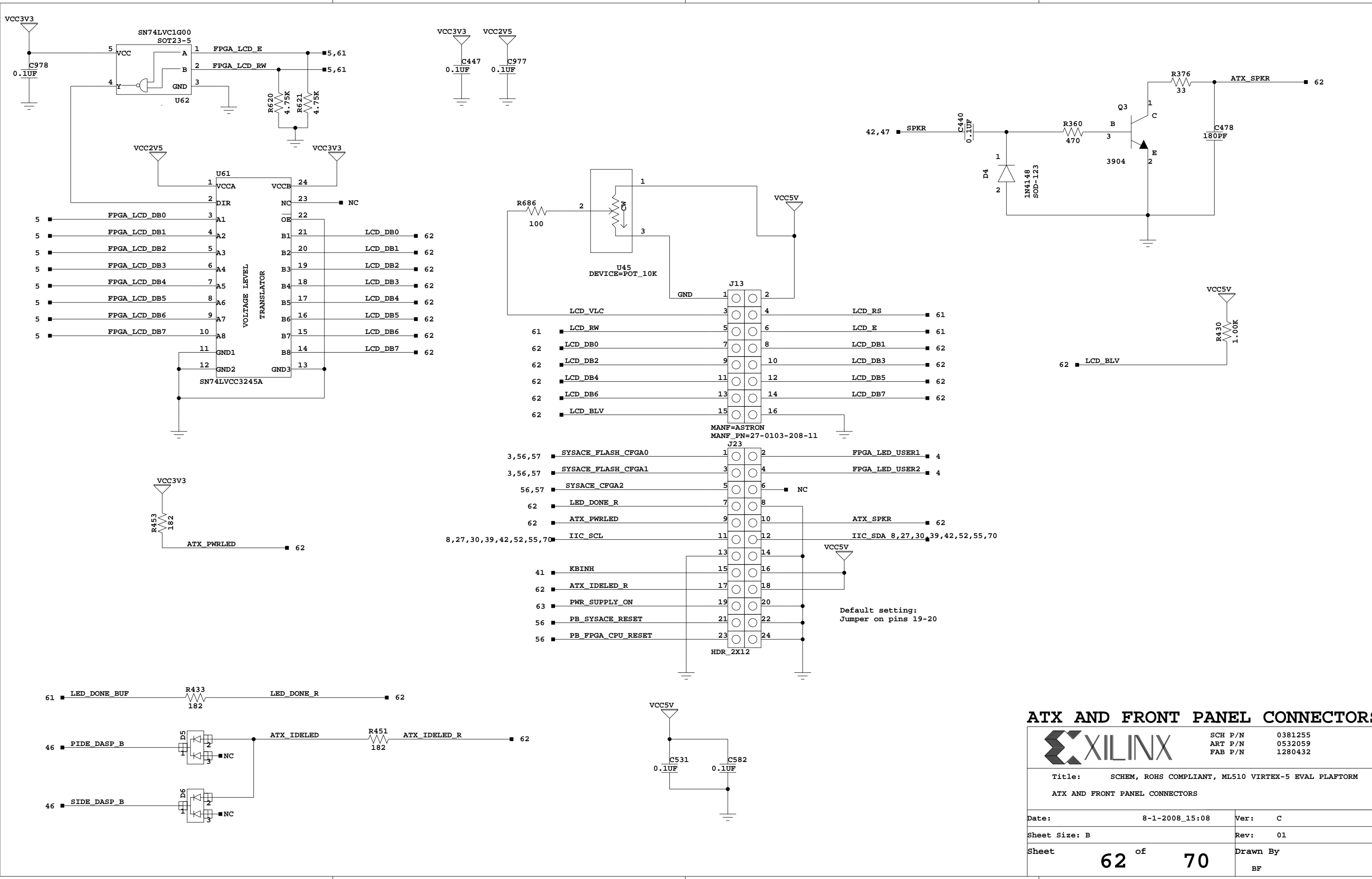


DEBUG AND STATUS LEDS



SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOMR DEBUG AND STATUS LEDS	
Date: 8-1-2008_15:08	Ver: C
Sheet Size: B	Rev: 01
Sheet 61 of 70	Drawn By BF



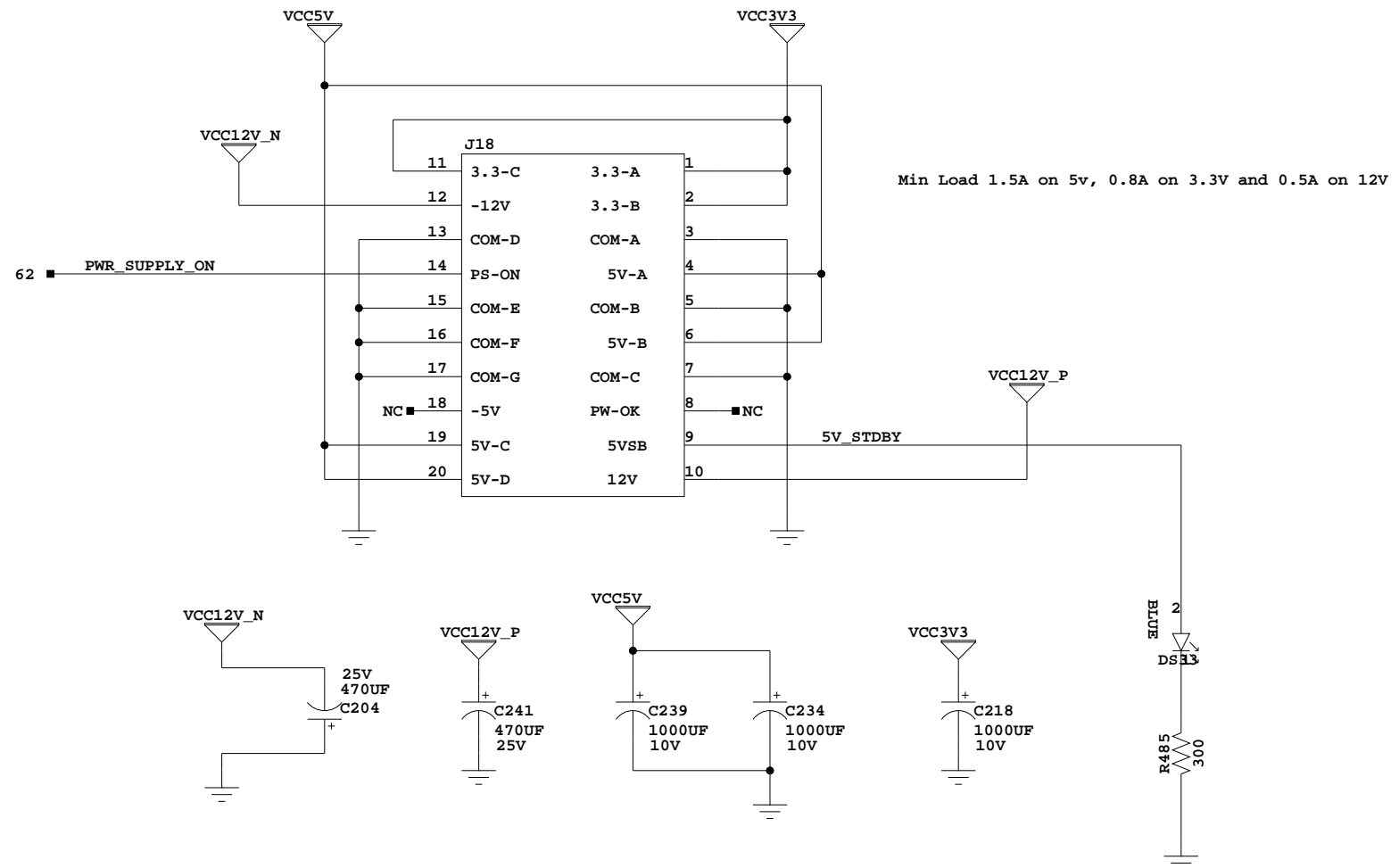
ATX AND FRONT PANEL CONNECTORS



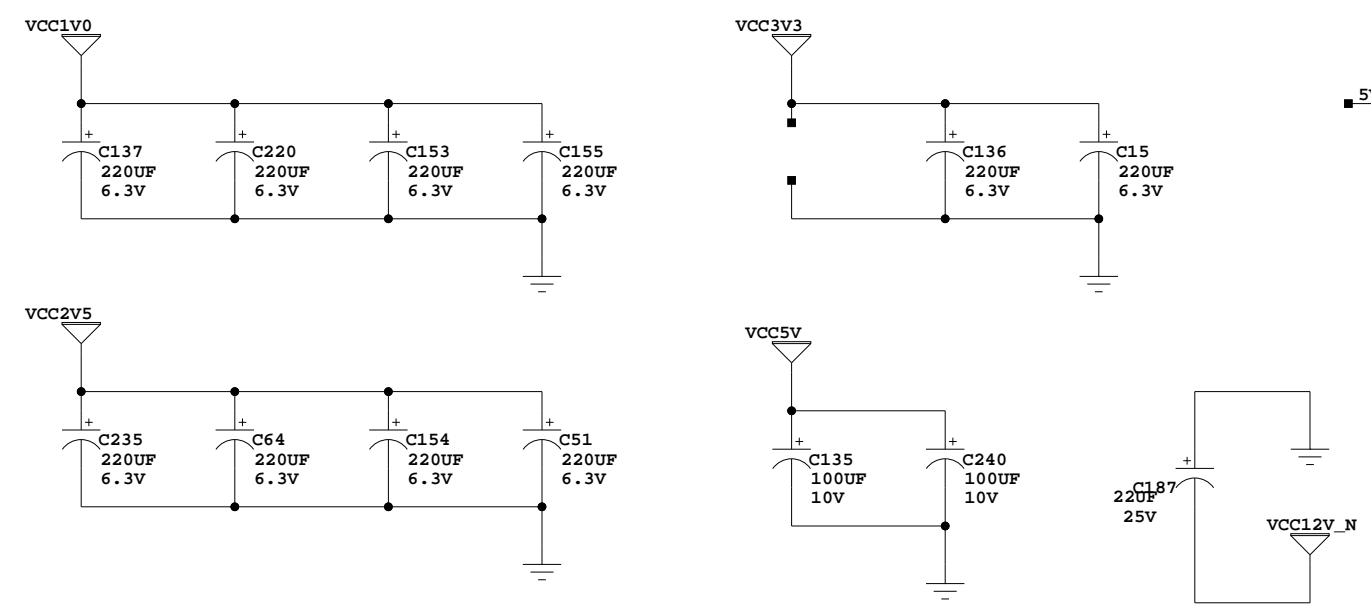
SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 ATX AND FRONT PANEL CONNECTORS

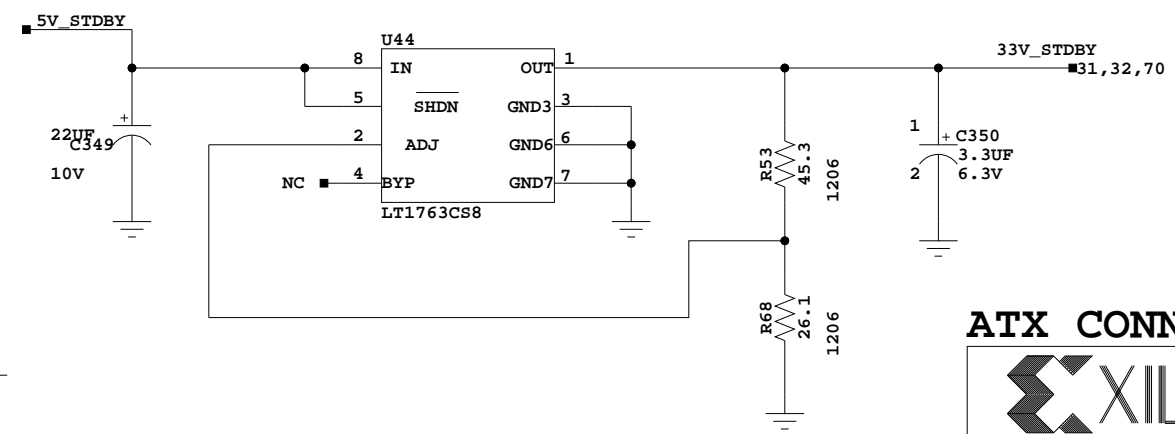
Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	62 of 70	Drawn By	BF



ATX Power Connector



BULK CAPS DISTRIBUTED AROUND BOARD.

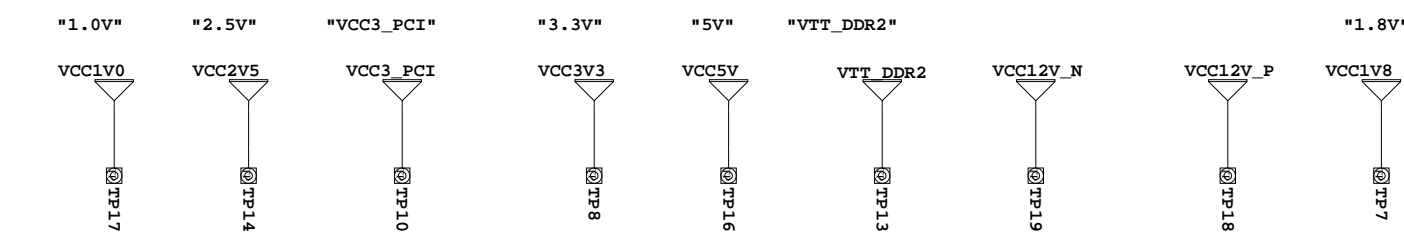
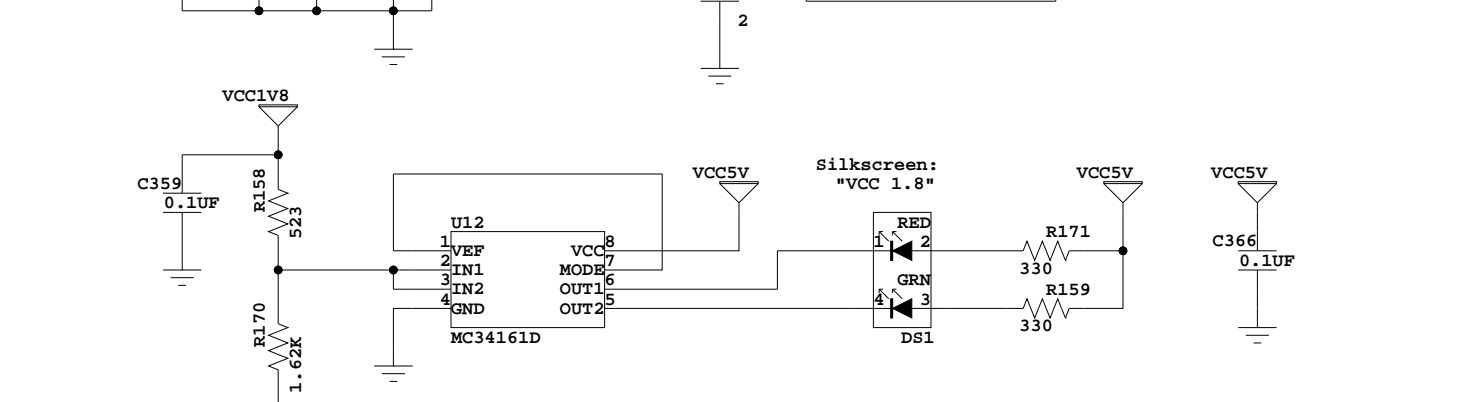
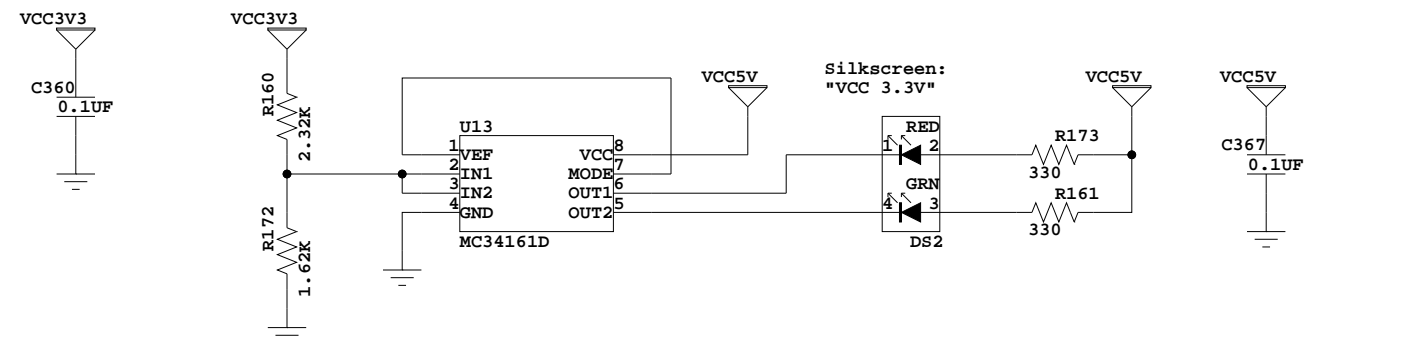
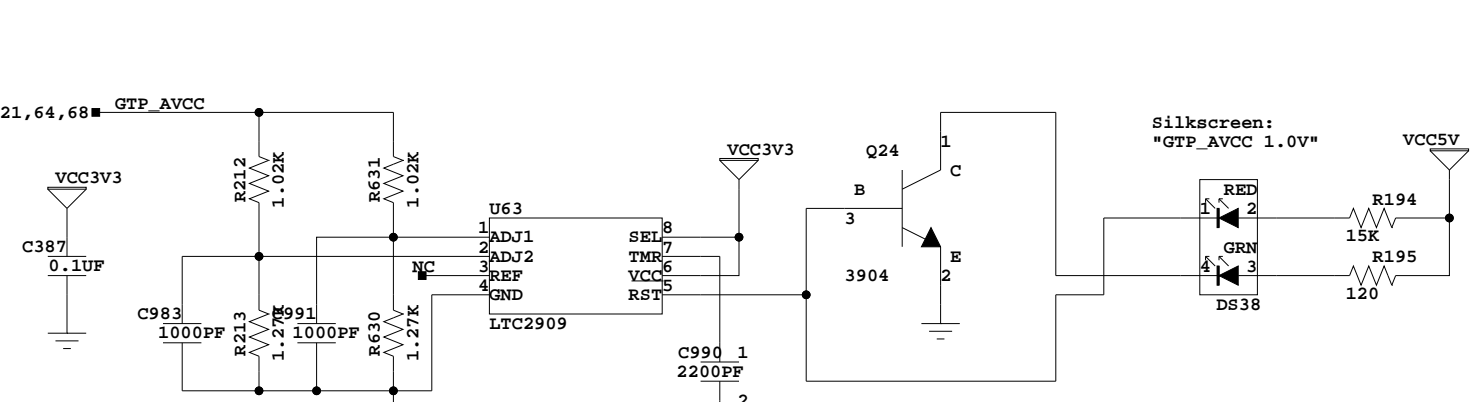
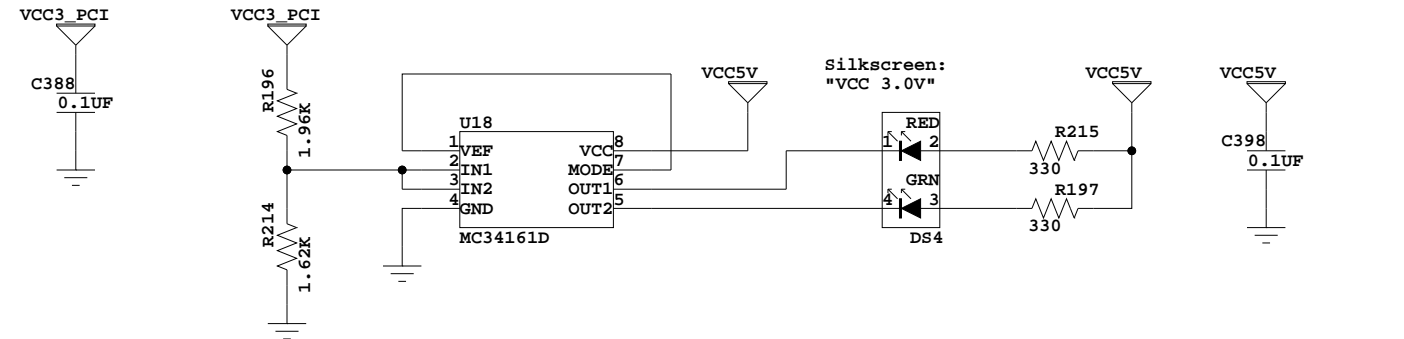
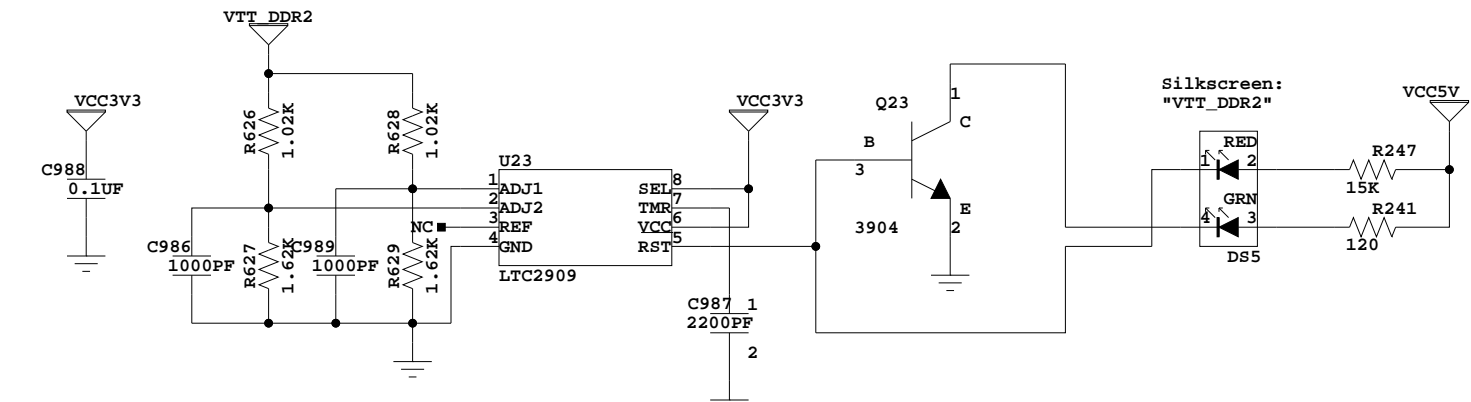
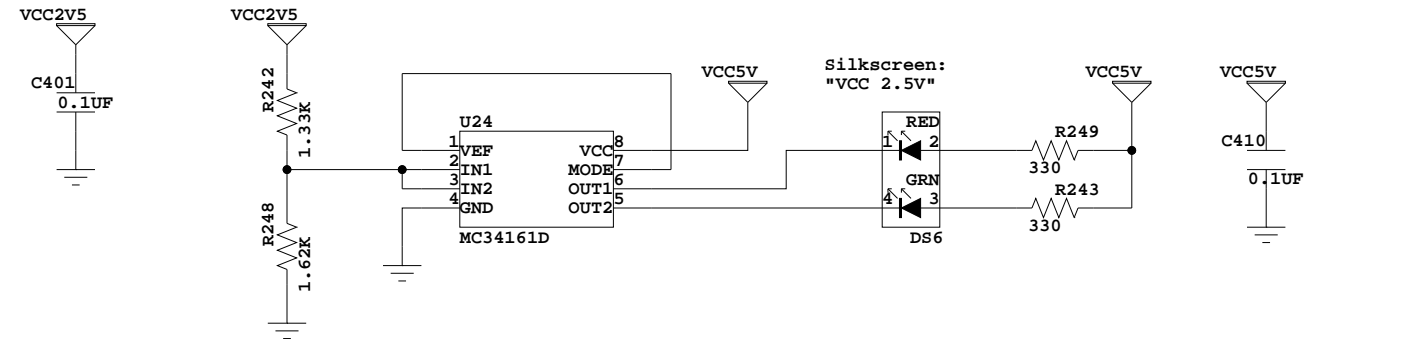
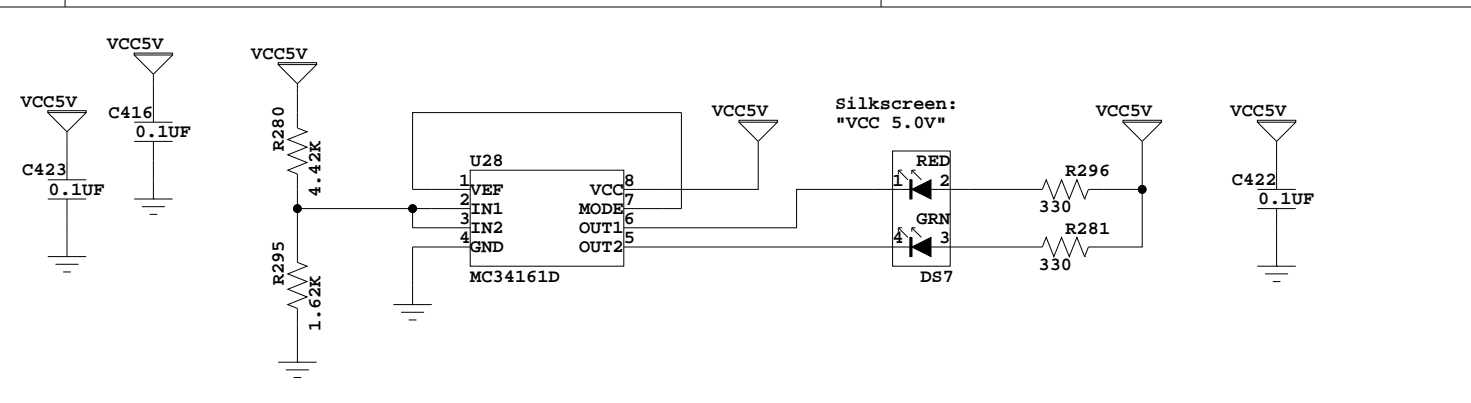
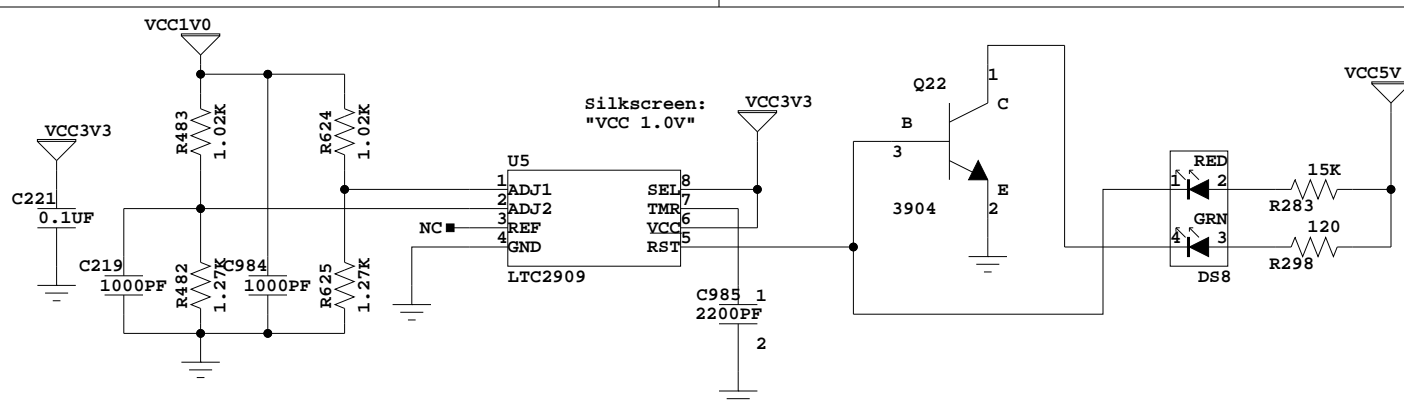


ATX CONNECTOR, PWR TOGGLE

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
ATX CONNECTOR, PWR TOGGLE AND HEADER

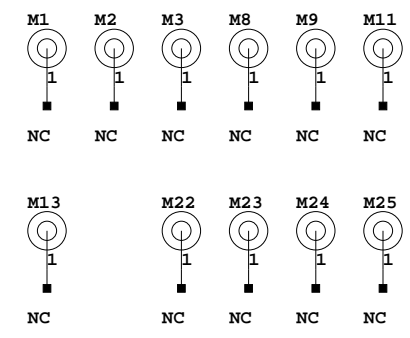
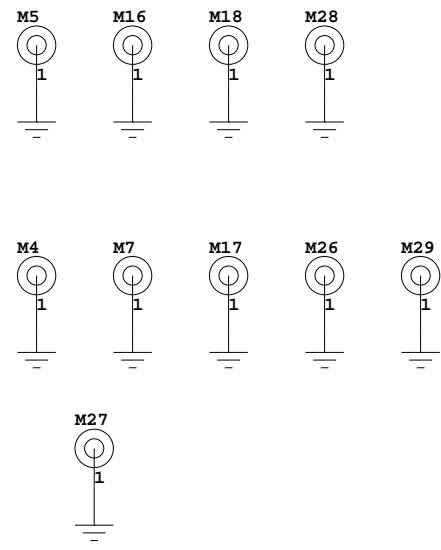
Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	63 of 70	Drawn By	BF



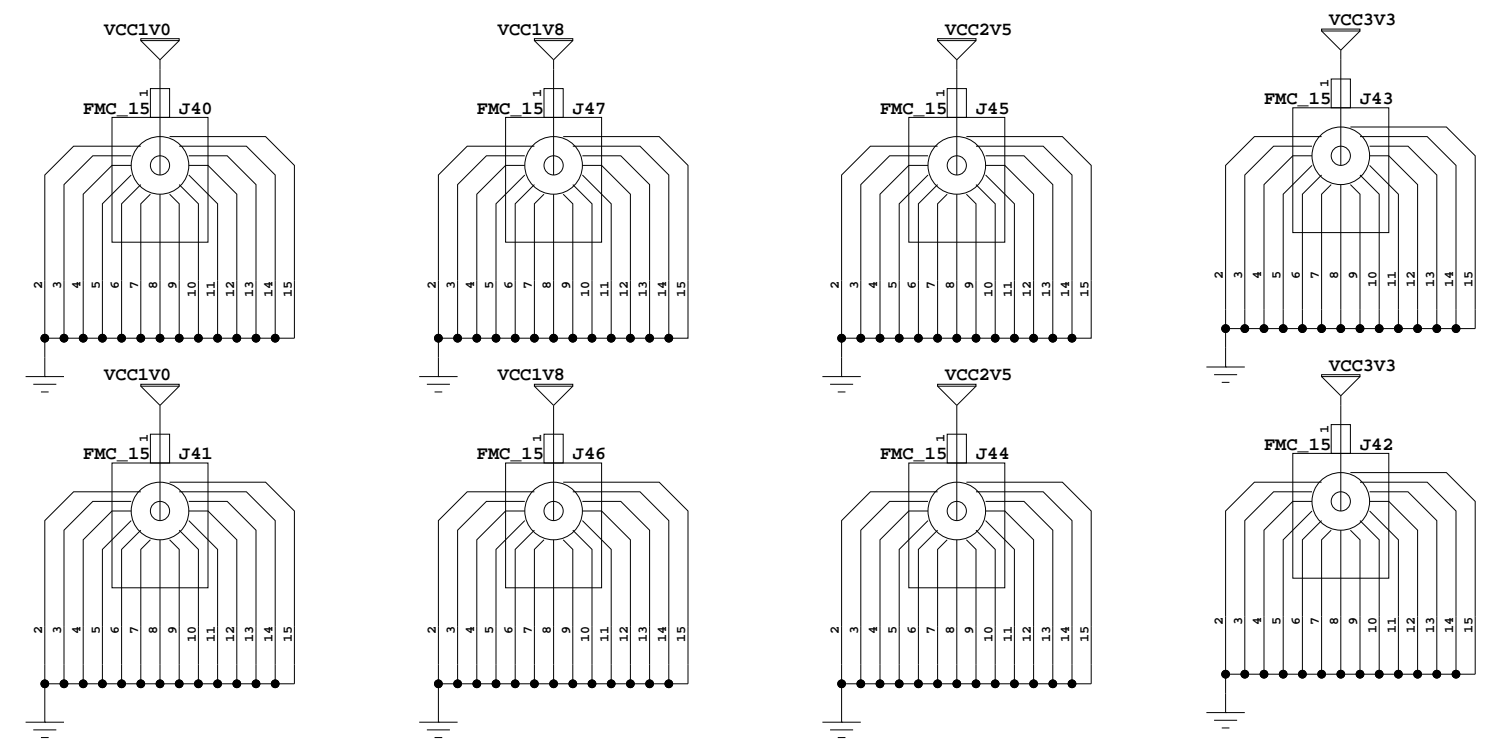
POWER SUPPLY MONITORS AND LEDS

		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM			
POWER SUPPLY MONITORS AND LEDS			
Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	64 of 70	Drawn By	BF

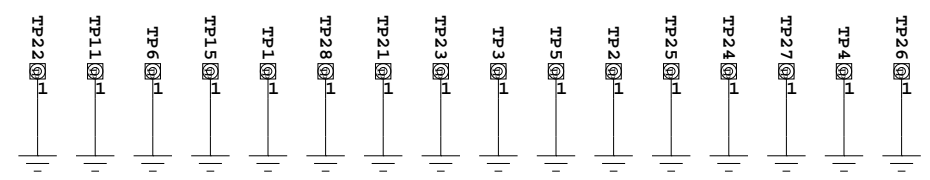
Mounting holes for ATX Form Factor



FMC connectors for power supply testing



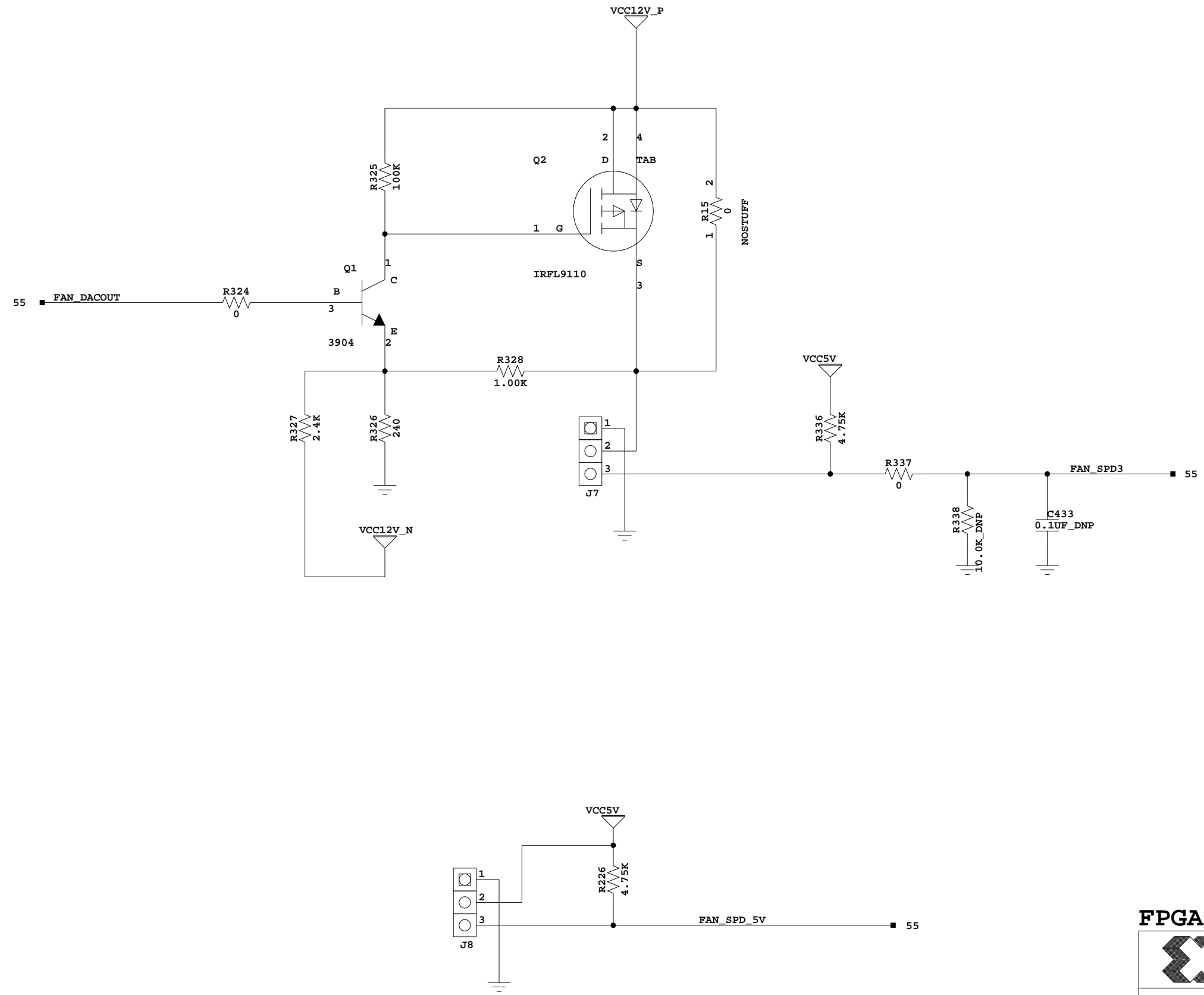
Spread out on the board.



Silkscreen:
"GND"

ATX MOUNTING HOLES / TEST POINTS

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTRM ATX MOUNTING HOLES AND TEST POINTS		
Date:	8-1-2008_15:08	Ver: C
Sheet Size:	B	Rev: 01
Sheet	65 of 70	Drawn By BF



FPGA FAN SWITCH AND TACH

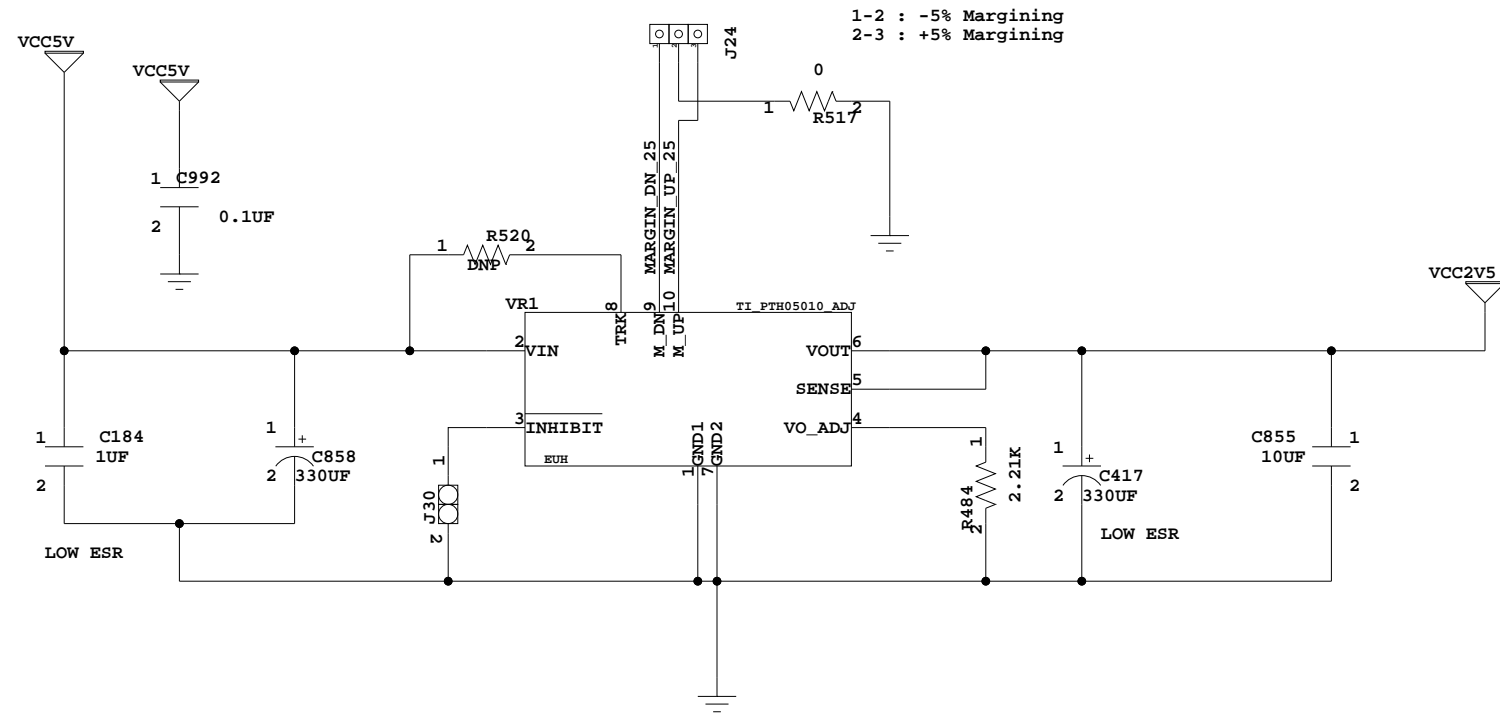


SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 FPGA FAN SWITCH AND TACH

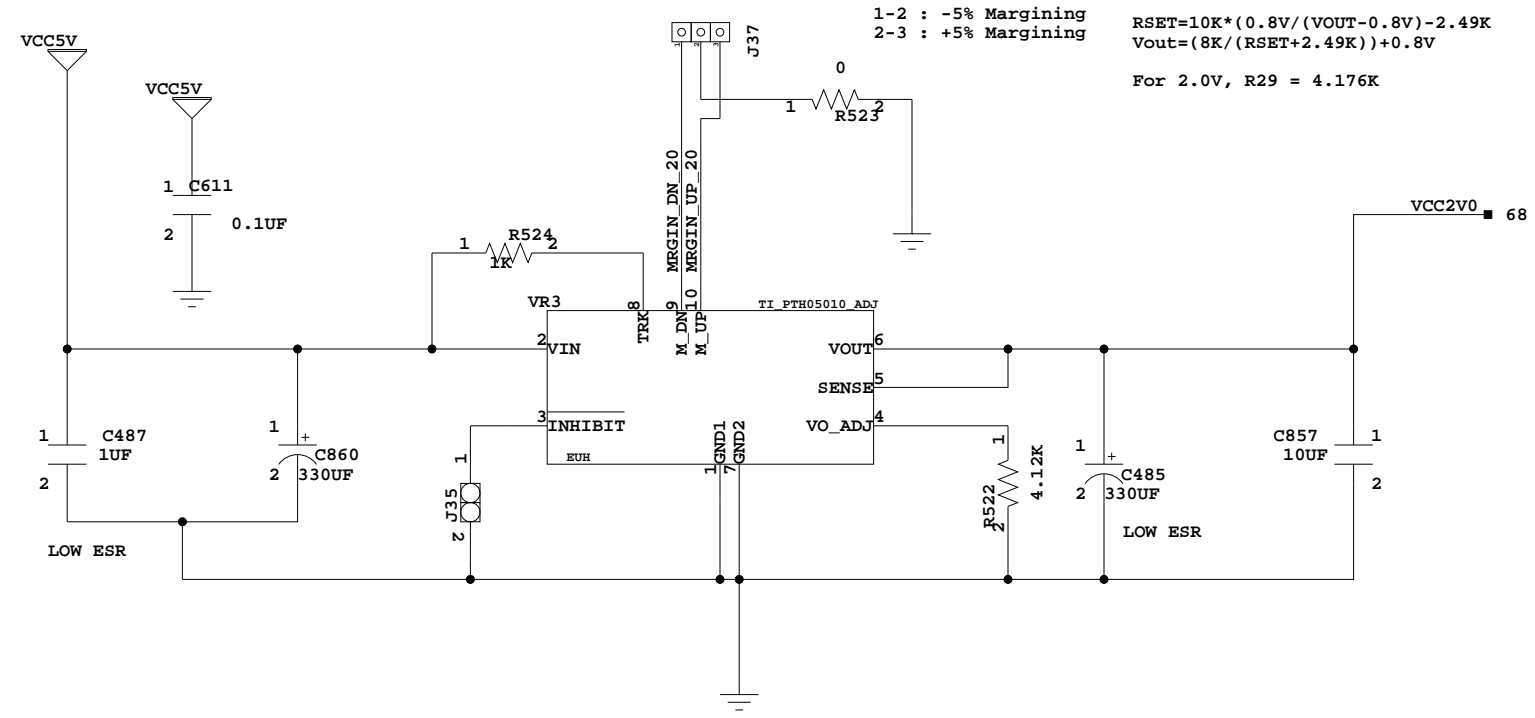
Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
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2.5V Supply @15A



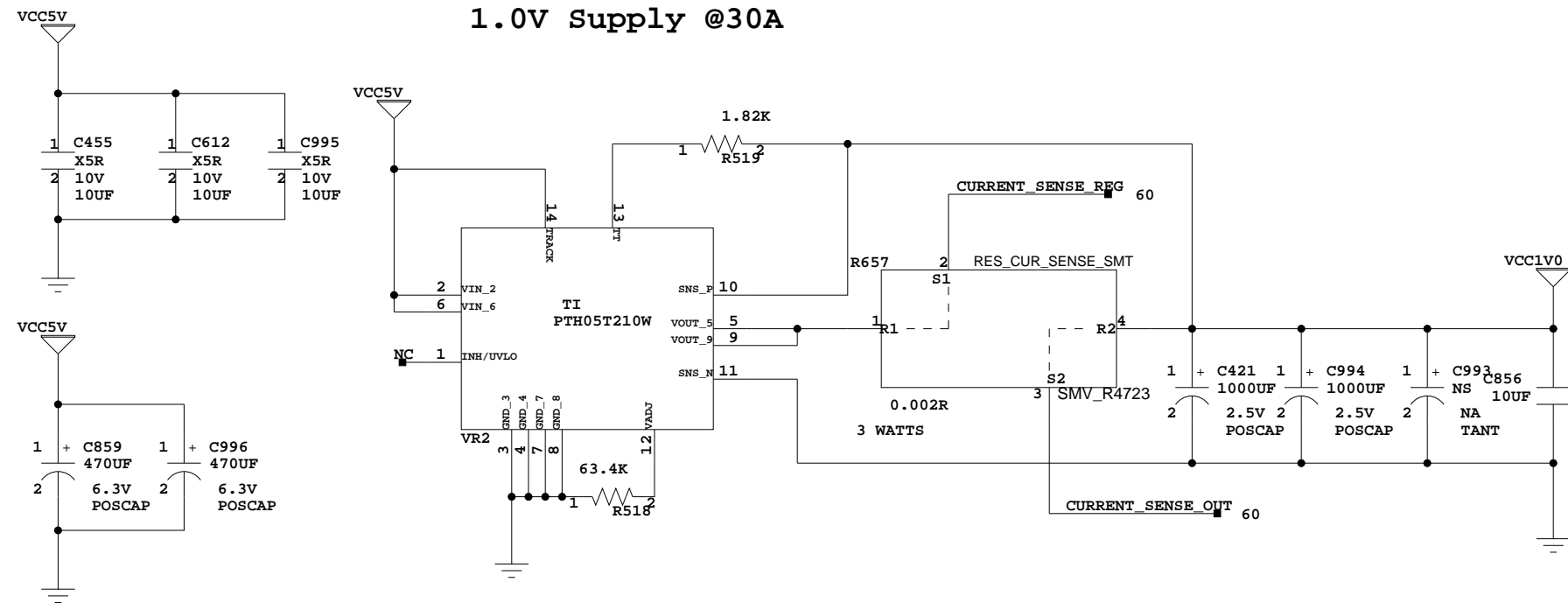
1-2 : -5% Margining
2-3 : +5% Margining

2.0V Supply @15A



1-2 : -5% Margining
2-3 : +5% Margining
 $RSET=10K*(0.8V/(VOUT-0.8V))-2.49K$
 $Vout=(8K/(RSET+2.49K))+0.8V$
For 2.0V, R29 = 4.176K

1.0V Supply @30A



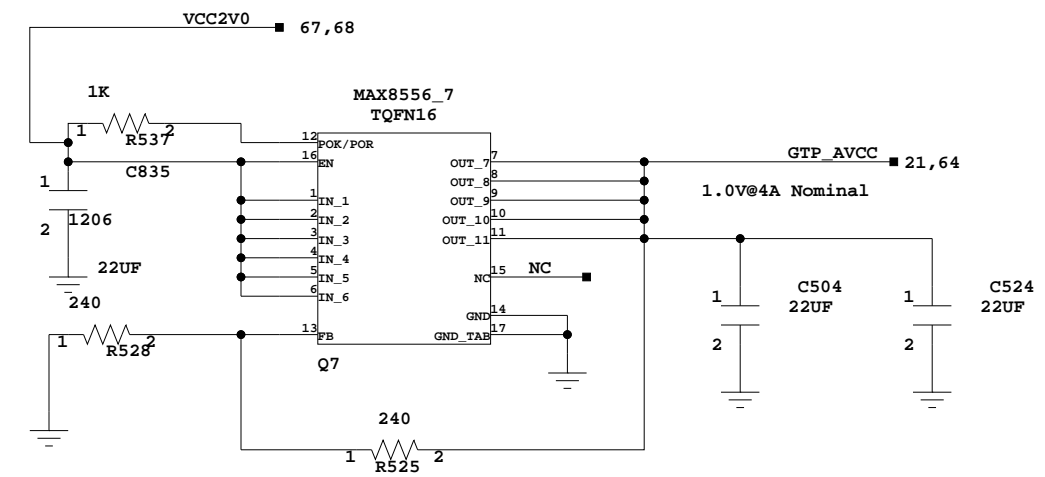
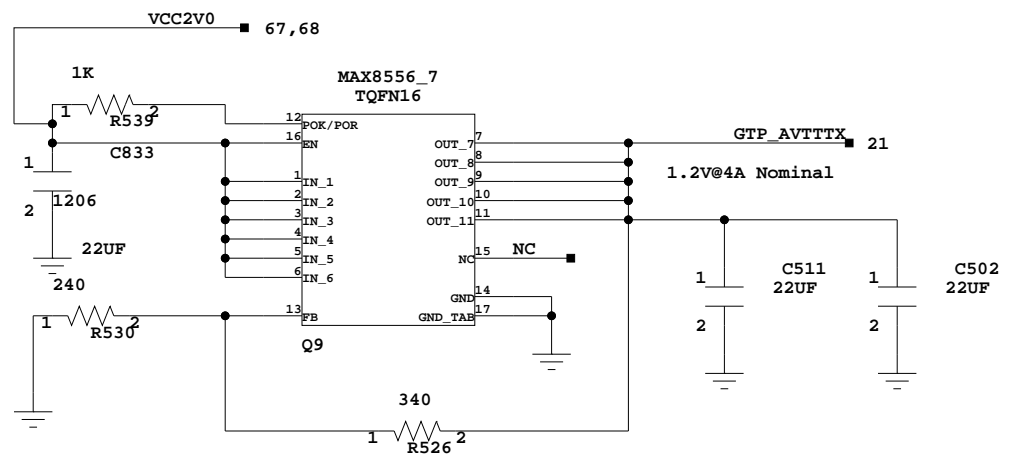
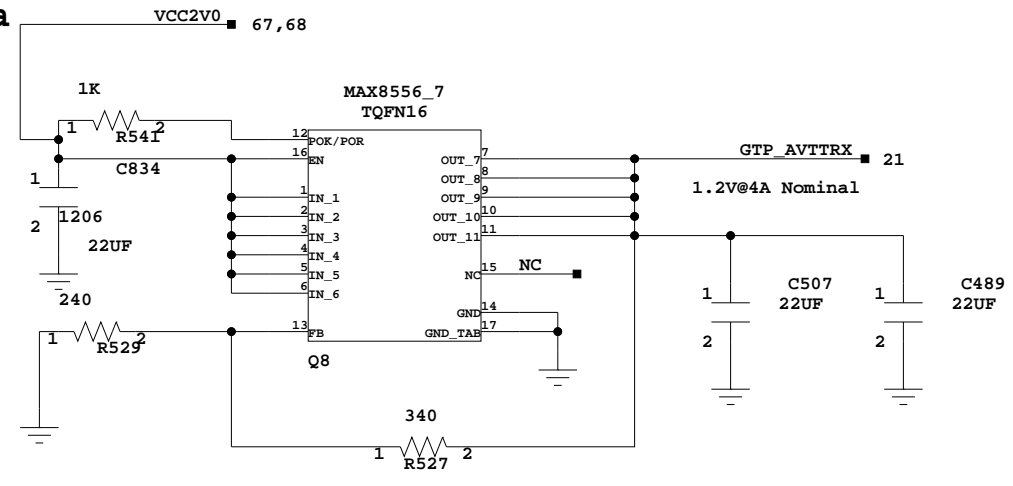
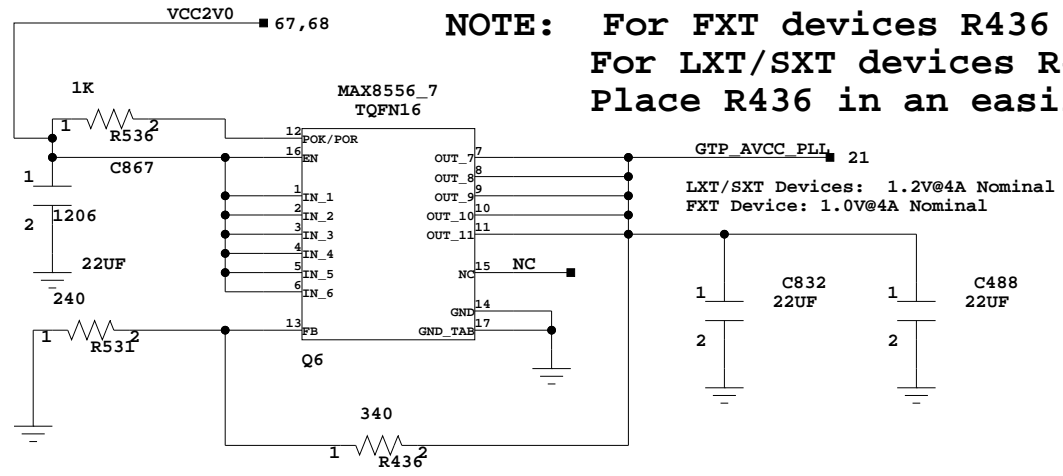
FPGA CORE AND IO VOLTAGE

XILINX SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTRM
FPGA CORE AND IO VOLTAGE

Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	67 of 70	Drawn By	BF

**NOTE: For FXT devices R436 must be 240 ohms
 For LXT/SXT devices R436 should be 340 ohms
 Place R436 in an easily accessible area**



$$R2 = R1 * \left\{ \left(\frac{V_{out}}{0.5} \right) - 1 \right\}$$

GTP POWER SUPPLIES



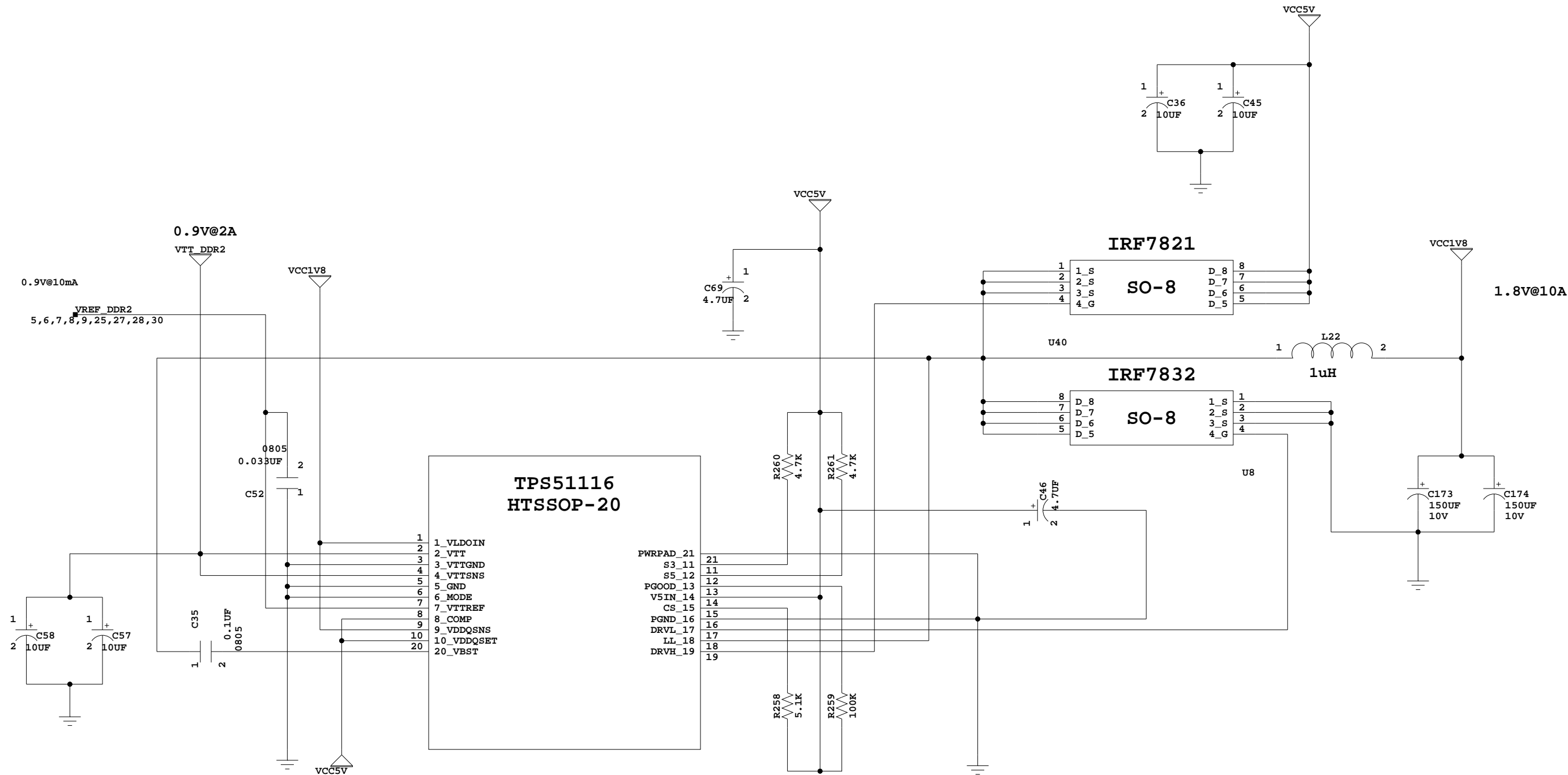
SCH P/N 0381255
 ART P/N 0532059
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
 GTP POWER SUPPLIES

Date: 8-1-2008_15:08 Ver: C

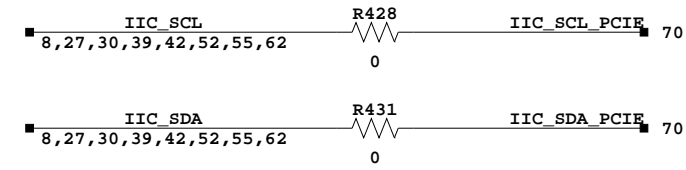
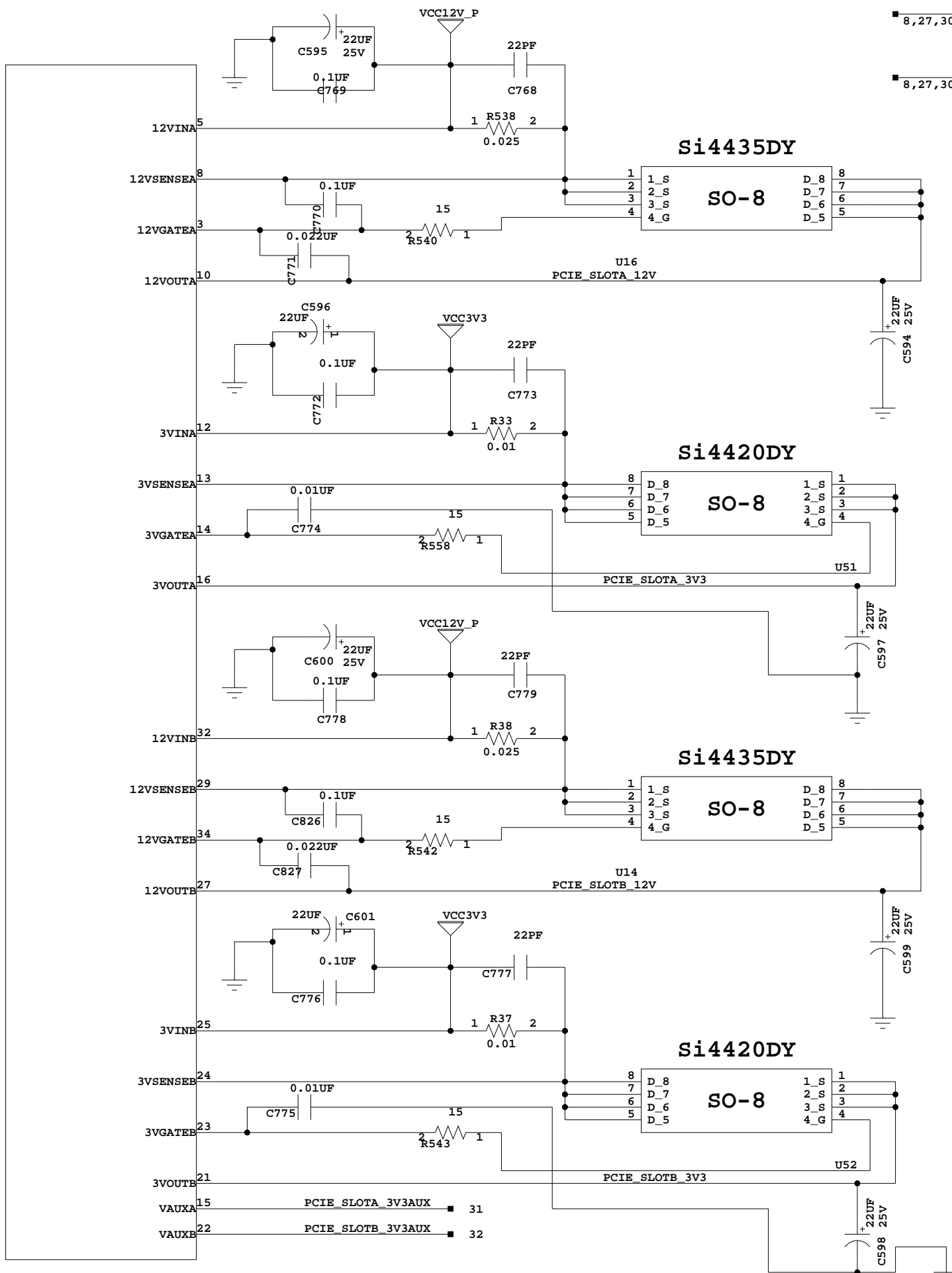
Sheet Size: B Rev: 01

Sheet 68 of 70 Drawn By BF

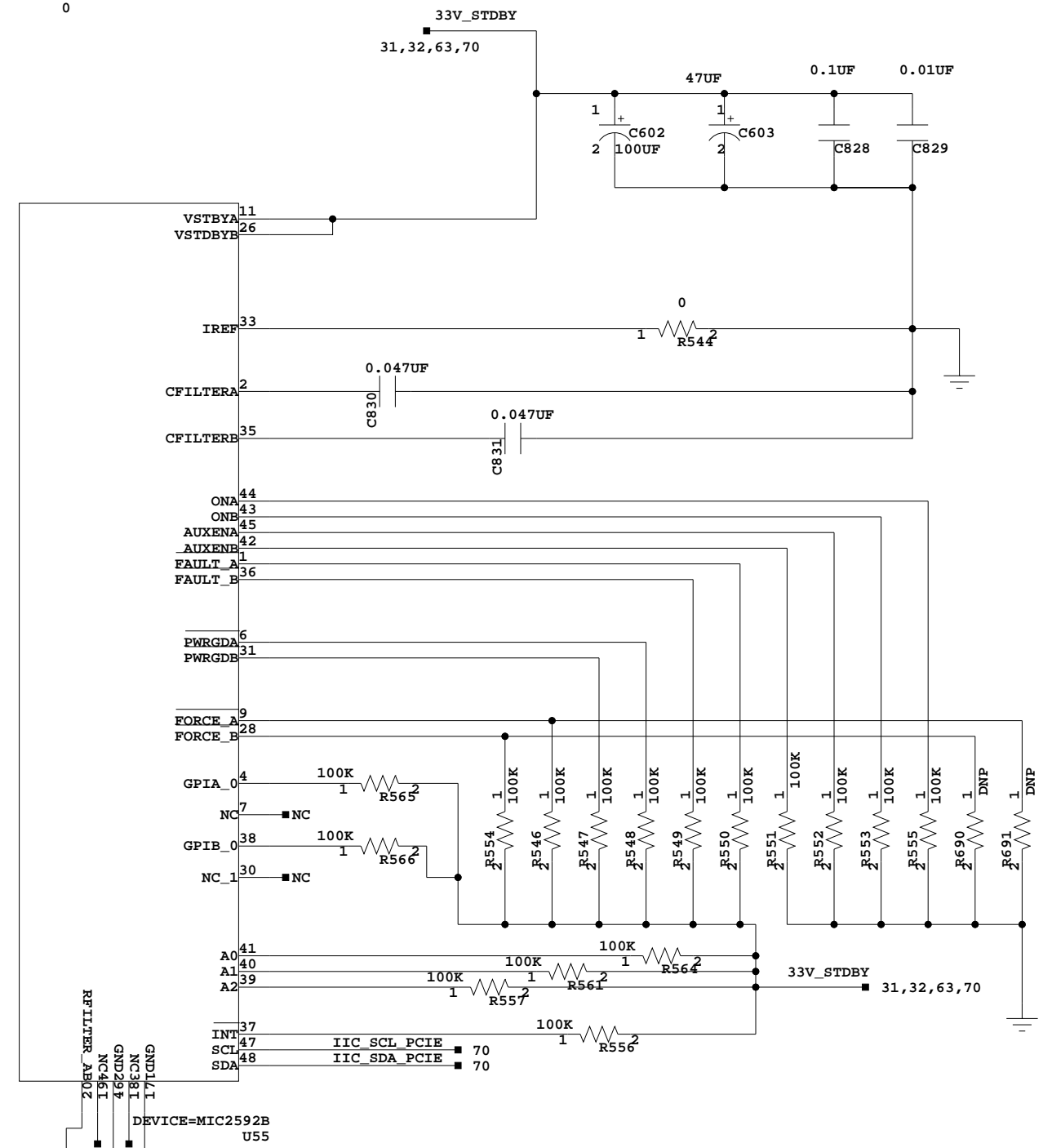


DDR2 POWER SUPPLY

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM DDR2 POWER SUPPLY		
Date:	8-1-2008_15:08	Ver: C
Sheet Size:	B	Rev: 01
Sheet	69 of 70	Drawn By BF



I2C ADDR = 0x8E
Make sure IIC Address is set correctly



PCI-E PWR MGMT CONTROLLER



SCH P/N 0381255
ART P/N 0532059
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM
PCI-E PWR MGMT CONTROLLER

Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	70 of 70	Drawn By	BF

DEVICE=MIC2592B
U55