Product Not Recommended for New Designs

Virtex-II Pro ML324 and ML325 Platform

User Guide

UG063 (v1.2) May 30, 2006

XILINX®

P/N 0402276-03

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/07/04	1.0	Initial Xilinx release.
05/24/06	1.1	Corrected pin numbers in Table 7, page 14. Added revision number extensionto P/N on title page.
05/30/06	1.2	Updated “About This Guide.”

Table of Contents

Preface: About This Guide

Guide Contents 5
Additional Resources 5
Conventions 5
Typographical 5
Online Document 6

Virtex-II Pro ML324 and ML325 Platform

Package Contents 7
CD-ROM Contents 7
Conventions 8
Introduction 8
Features 8
Detailed Description 10
1. Power Switch 11
2. Power Supply Jacks 12
3. FPGA Configuration 12
4. Oscillator Sockets 13
5. Single-Ended SMA Clocks 13
6. Differential Oscillators 14
7. Differential SMA Clock 14
8. User LEDs (Active High) 15
9. User DIP Switches (Active High) 16
10. User Push Buttons (Active High) 17
11. BERT Headers 17
12. Recovered Clock Monitor Headers 19
13. Program Switch (Active Low) 20
14. Reset Switch (Active Low) 20
15. DONE LED 20
16. INIT LED 20
17. Config Address DIP Switch 20
18. RocketIO Transceiver Pins 21
19. RS-232 Port Pins 22
20. SDRAM Connection 23

XILINX®

Preface

About This Guide

This document describes the features and operation of the Virtex™-II Pro ML324 and ML325 prototype and demonstration boards.

Guide Contents

This manual contains the following chapter:

- "Virtex-II Pro ML324 and ML325 Platform"

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/literature.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**

Convention	Meaning or Use	Example
Italic font	Variables in a syntax statement for which you must supply values	**ngdbuild** *design_name*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **bus[7:0]**, they are required.	**ngdbuild** [*option_name*] *design_name*
Braces { }	A list of items from which you must choose one or more	**lowpwr** ={**on**|**off**}
Vertical bar |	Separates items in a list of choices	**lowpwr** ={**on**|**off**}
Vertical ellipsis . . .	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN' . . .
Horizontal ellipsis ...	Repetitive material that has been omitted	**allow block** *block_name loc1 loc2 ... locn;*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Platform FPGA User Guide.*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Virtex-II Pro ML324 and ML325 Platform

Package Contents

- Xilinx Virtex™-II Pro ML324 or ML325 platform (referred to as the "ML32x platform")
- User guide
- Four SMA-to-SMA coax cable assemblies
- CD-ROM
- CompactFlash (CF) memory for System ACE™ solution
- RS-232 cable
- Power supply

CD-ROM Contents

- User guide in PDF format
- Example design file for demonstration of the RocketIO™ transceivers
- System ACE files (`*.ace`) for each part type supported by the board
- Full schematics of the board in both PDF format and ViewDraw schematic format
- PC board layout in Pads PCB format
- Gerber files in `*.pho` and `*.pdf` for the PC board (There are many free or shareware Gerber file viewers available on the Internet for viewing and printing these files)

Conventions

The voltage range names used on the ML32*x* platform differs from those shown in the *Virtex-II Pro Platform FPGAs: Complete Data Sheet* (DS083) at http://direct.xilinx.com/bvdocs/publications/ds083.pdf

They correspond as shown in Table 1:

Table 1: **Voltage Range Names**

Data Book	Board		Data Book	Board
VCCAUX	VAUX		VCCO	VCCO
VCCAUXRX	AVCCAUX		VTRX	VT_RX
VCCAUXTX	AVCCAUX		VTTX	VT_TX
VCCINT	VCORE			

Introduction

The ML32*x* platform allows designers to investigate and experiment with the features of RocketIO transceivers. This document describes the features and operation of the boards.

The platforms and their corresponding packages are shown in Table 2.

Table 2: **Platforms and Packages**

Platform	Package
ML324	FF1517
ML325	FF1704

Features

- Virtex-II Pro FPGA
- On-board power supplies for all necessary voltages capable of supplying 3A each
- Power supply jacks for optional use of external power supplies
- JTAG configuration port for use with Parallel Cable III and Parallel Cable IV cables
- System ACE configuration controller
- RS-232 serial port
- Two 125-MHz or 156.25-MHz differential clock oscillators
- Two 2.5V clock oscillator sockets
- Four differential clock pairs with SMA connectors
- Two single-ended clocks with SMA connectors
- One pair of 36-position headers with ground headers for parallel BERT cables
- 16 or 32 pairs of SMA connectors for the RocketIO transceivers
- Power indicator LEDs
- General purpose DIP switches, LEDs, and push buttons
- 128 Mb SDRAM

Figure 1shows a block diagram of the board.

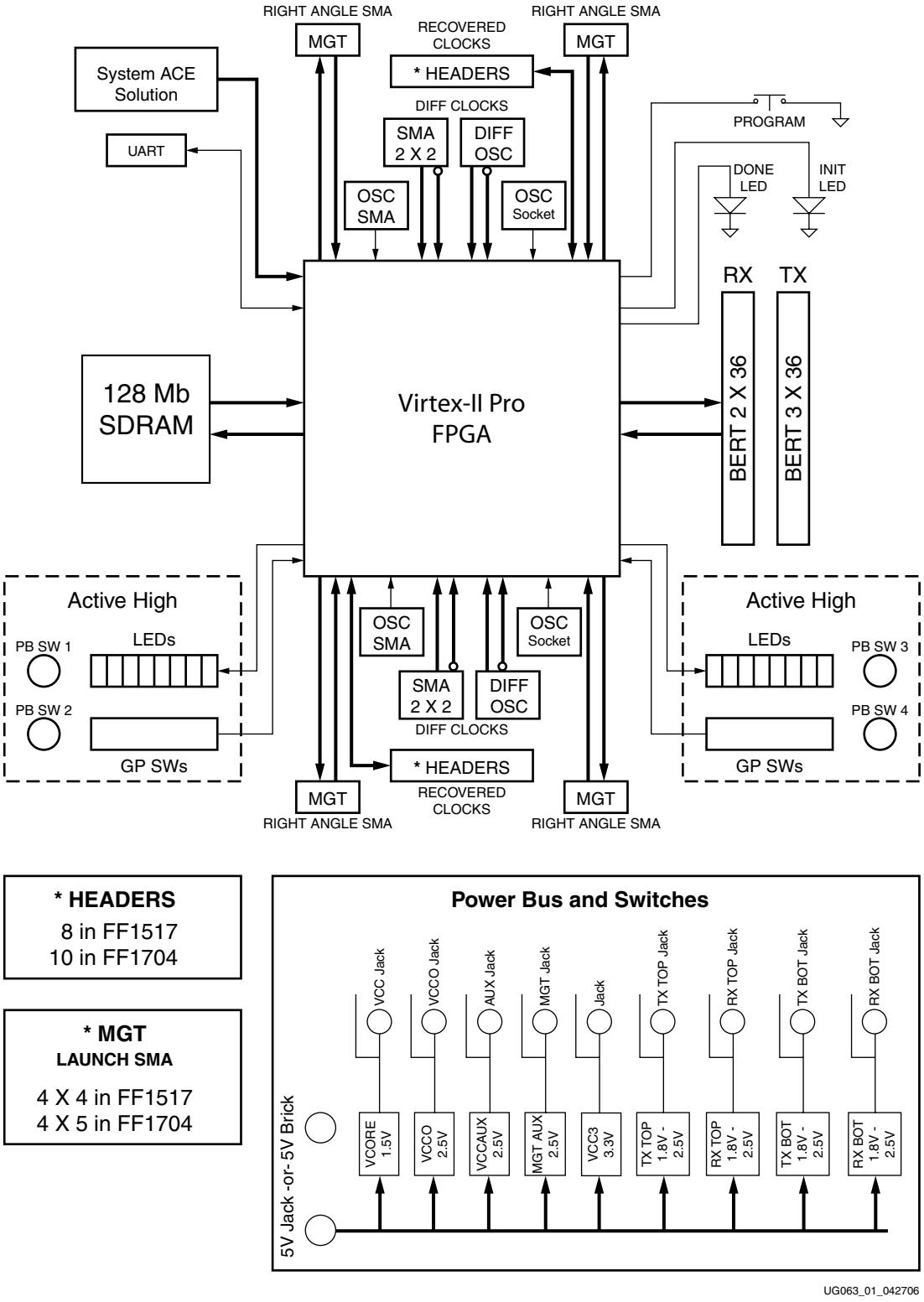

Figure 1: **Virtex-II Pro ML32*x* Platform Block Diagram**

Detailed Description

The ML325 platform show in n Figure 2 represents the ML32x platforms described in this user guide. Each feature is detailed in the numbered sections that follow.

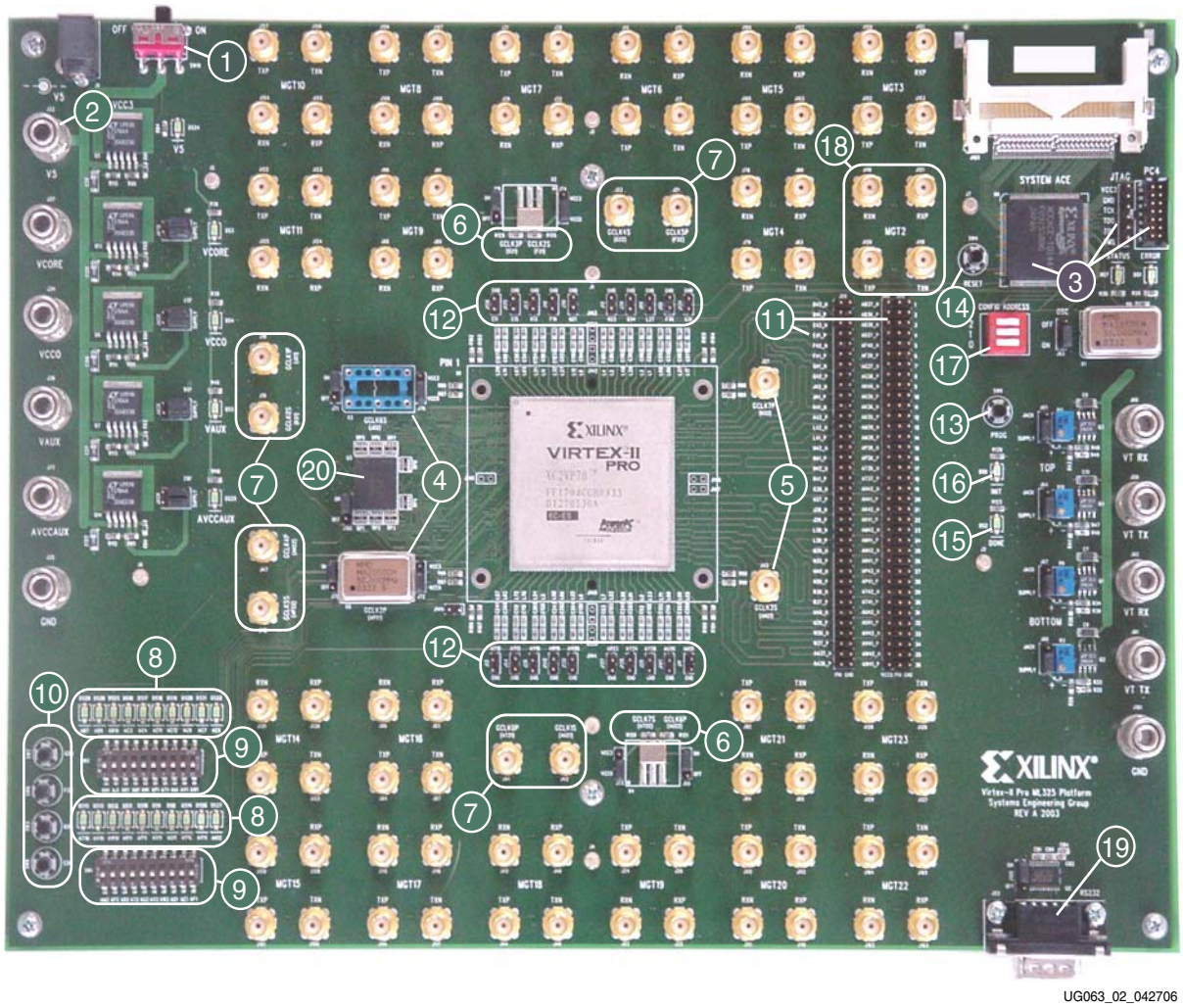

Figure 2: **Detailed Description of Virtex-II Pro ML32*x* Platform Components**

1. Power Switch

The board has an on-board power supply and an on|off power switch. When lit, a green LED indicates power from the power brick connector or the 5V jack.

On Position

In the *on* position, the power switch enables delivery of all power to the board by way of voltage regulators situated close to the left and right edges of the board. These regulators feed off a 5V external power brick or the 5V power supply jack.

The voltage regulators deliver fixed voltages. Maximum current range for each voltage regulator is 3A.

RocketIO termination voltages are situated on the right edge of the board and are marked as VT_RX, VT_TX (top set) and VT_RX, VT_TX (bottom set). These can be used to deliver a fixed voltage by appropriate selection of the resistors designated as R32, R39, R46, and R49 (default is set to 2.5V). These can be made to deliver a variable voltage by depopulating the above mentioned resistors and manipulating the potentiometers (R3, R9, R10, R11). The voltage range is as shown in Table 3.

Table 3: **Voltage Ranges**

Label	Max Voltage
VCORE	1.5V (1.65V for -ES devices)
VCCO	2.5V
VCCAUX	2.5V
AVCCAUX	2.5V
VT_TX (top set)	1.7 - 2.5V
VT_RX (top set)	1.7 - 2.5V
VT_TX (bottom set)	1.7 - 2.5V
VT_RX (bottom set)	1.7 - 2.5V

Off Position

In the *off* position, the power switch disables all modes of powering the FPGA.

Power Enable Jumpers

For each power supply there are headers marked **Supply** on one side and **Jack** on the other side. Appropriate placements of jumpers on these headers enables delivery of all power from either the on-board regulators or power supply jacks marked V5, VCORE, VCCO, VCCAUX, AVCCAUX, VT_TX, VT_RX (top set) and VT_TX, VT_RX (bottom set).

2. Power Supply Jacks

One method of delivering power to the FPGA is by way of the power supply jacks. These jacks are:

- AVCCAUX
  - Supplies power to the RocketIO transceivers on the FPGA
- VCCAUX
  - Supplies voltage to the V_{AUX} header and the V_{AUX} FPGA pins
- VCCO
  - Supplies I/O voltages to the FPGA
- VCORE
  - Supplies voltage to the core of the FPGA
    (Consult the *Virtex-II Pro Platform FPGAs: Complete Data Sheet* (DS083) at http://direct.xilinx.com/bvdocs/publications/ds083.pdf for the maximum VCORE voltage for the device you are using)

The following two jacks supply termination voltages to the RocketIO transceivers on the top and bottom edges of the FPGA:

- VT_TX (top set and bottom set)
- VT_RX (top set and bottom set)

Note: 5V must always be applied to the 5V jack or to the external power brick connector to power the 3.3V regulator for the System ACE chip.

3. FPGA Configuration

The FPGA can only be configured in JTAG mode using one of the following options:

- Parallel Cable III cable
- Parallel Cable IV cable
- System ACE configuration controller(1)

Using the configuration address DIP switches, one of eight bitstreams stored in the CompactFlash memory can be accessed through the on-board System ACE controller.

Note: When using the flying wire leads or the Parallel Cable IV cable, the System ACE controller will be bypassed, thus causing no disruption in the JTAG chain.

1. For further information, consult the System ACE CompactFlash Solution (DS080) http://www.xilinx.com/bvdocs/publications/ds080.pdf.).

4. Oscillator Sockets

The ML32*x* platform has two crystal oscillator sockets, each wired for standard LVTTL-type oscillators. These connect to the FPGA clock pins as shown in Table 4. The oscillator sockets accept both half- and full-sized oscillators and are powered by 3.3V or the VCCO 2.5V power supply.

Table 4: **OSC Connections**

Label	ML324		ML325	
	Clock Name	Pin	Clock Name	Pin
X3	CLK_OCS_TOP	M21	CLK_OCS_TOP	J22
X5	CLK_OCS_BOT	AG20	CLK_OCS_BOT	AP21

5. Single-Ended SMA Clocks

The ML32*x* platform has two SMA clock inputs that allow connection to an external function generator. These connect to the FPGA clock pins as shown in Table 5.

Table 5: **SMA Clock Pin Connections**

Label	ML324		ML325	
	Clock Name	Pin	Clock Name	Pin
J27	CLK_SMA_TOP	L21	CLK_SMA_TOP	K22
J43	CLK_SMA_BOT	AH20	CLK_SMA_BOT	AN21

6. Differential Oscillators

The ML32*x* platform has two differential oscillators, each wired to LVDS inputs on the FPGA. These connect to the FPGA clock pins shown in Table 6. The differential oscillators are powered by 3.3V or the VCCO 2.5V power supply.

Table 6: **Differential Oscillator Pin Connections**

Label	ML324		ML325	
	Clock Name	Pin	Clock Name	Pin
X2	CLK_BREF2_TOP_P CLK_BREF2_TOP_N	K20 J20	CLK_BREF2_TOP_P CLK_BREF2_TOP_N	G21 F21
X4	CLK_BREF_BOT_P CLK_BREF_BOT_N	AT20 AR20	CLK_BREF_BOT_P CLK_BREF_BOT_N	AU22 AT22

7. Differential SMA Clock

There are four pairs of 50Ω SMA connectors that can be used (with 100Ω termination) to connect to an external function generator. These connect to the FPGA pins as shown in Table 7. These SMA connectors can also be used as eight single-ended clock inputs.

Table 7: **Differential Clock Pin Connections**

Label	ML324		ML325	
	Clock Name	Pin	Clock Name	Pin
J21 J23	CLK_BREF_TOP_P CLK_BREF_TOP_N	E20 D20	CLK_BREF_TOP_P CLK_BREF_TOP_N	G22 F22
J41 J42	CLK_BREF2_BOT_P CLK_BREF2_BOT_N	AK20 AL20	CLK_BREF2_BOT_P CLK_BREF2_BOT_N	AT21 AU21
J16 J19	CLK_DIFF_TOP_P CLK_DIFF_TOP_N	M20 N20	CLK_DIFF_TOP_P CLK_DIFF_TOP_N	K21 J21
J47 J48	CLK_DIFF_BOT_P CLK_DIFF_BOT_N	AJ21 AH21	CLK_DIFF_BOT_P CLK_DIFF_BOT_N	AN22 AP22

8. User LEDs (Active High)

There are 20 active-high LEDs, as shown in Table 8 and Table 9, connected to user I/O pins on the FPGA. These LEDs can be used to indicate status or for any other purpose the user desires.

Table 8: **User LEDs - LED Row 1**

LED Row 1	ML324	ML325
	Pin	Pin
DS15	AK30	AT10
DS13	AL30	AV10
DS12	AN30	AW10
DS11	AM30	AR11
DS10	AT30	AP11
DS9	AL29	AV11
DS8	AT29	AU11
DS14	AM29	AY10
DS26	AR29	AY11
DS27	AK29	AN12

Table 9: **User LEDs - LED Row 2**

LED ROW 2	ML324	ML325
	Pin	Pin
DS29	D10	AB7
DS28	H14	AB9
DS23	E15	AB10
DS16	G15	AC3
DS17	F14	AC4
DS18	D14	AC11
DS19	J10	A12
DS20	G11	AC6
DS21	F10	AC7
DS22	E11	AC9

9. User DIP Switches (Active High)

There are 20 active-high DIP switches, as shown in Table 10 and Table 11, connected to user I/O pins on the FPGA. These DIP switches can be used to generate vectors or any other purpose that the user sees fit.

Table 10: **User DIP Switches - SW1**

SW1	ML324	ML325
	Pin	Pin
1	AA10	AM2
2	AB10	AP2
3	AC10	AR2
4	AD10	AT2
5	AE10	AU2
6	AF10	AV2
7	AG10	AW2
8	AH10	AD1
9	AB11	AE1
10	AF11	AF1

Table 11: **User DIP Switches - SW2**

SW2	ML324	ML325
	Pin	Pin
1	M10	AH1
2	N10	AJ1
3	P10	AK1
4	R10	AM1
5	T10	AN1
6	U10	AP1
7	V10	AT1
8	W10	AU1
9	N11	AV1
10	T11	AW1

10. User Push Buttons (Active High)

There are four active-high push buttons, as shown in Table 12, connected to user I/O pins on the FPGA. These push buttons can be used for any purpose that the user sees fit.

Table 12: **User Push Buttons**

Label	ML324	ML325
	Pin	Pin
SW7	D30	G33
SW6	E30	F33
SW3	AL18	D34
SW8	AK18	C34

11. BERT Headers

There is one pair of 72-position headers intended to be used for parallel Bit Error Rate Testing (BERT). The odd numbered pins of the BERT headers J56 and J55 are connected to user I/O pins (see Table 13, which spans multiple pages). The even numbered pins of J56 and J55 are connected to GND. The third row of header pins (J49) to the left of J55 are connected to VCCO. This gives the user the ability to jumper I/O pins on J56 to GND and I/O pins on J55 to either VCCO or GND.

Table 13: **BERT Headers J56 and J55**

Header J56	ML324	ML325	Polarity	Header J55	ML324	ML325	Polarity
	Pin	Pin			Pin	Pin	
1	H34	D42	N	1	AB35	AB37	N
2	H33	D41	P	3	AB34	AB36	P
3	H38	E42	N	5	AB37	AD38	N
4	H37	E41	P	7	AB36	AD37	P
5	J39	F42	N	9	AC39	AF40	N
6	J38	F41	P	11	AC38	AF39	P
7	K33	G41	N	13	AD34	AG37	N
8	K34	G42	P	15	AD33	AG38	P
9	K39	J42	N	17	AD38	AK40	N
10	K38	J41	P	19	AD37	AK39	P
11	L37	K41	N	21	AE37	AK36	N
12	L36	K42	P	23	AE36	AK35	P
13	L39	L42	N	25	AE39	AM39	N
14	L38	L41	P	27	AE38	AM38	P
15	M34	N42	N	29	AF34	AP39	N
16	M33	N41	P	31	AF33	AP38	P

Table 13: **BERT Headers J56 and J55 *(Continued)***

Header J56	ML324 Pin	ML325 Pin	Polarity	Header J55	ML324 Pin	ML325 Pin	Polarity
17	N39	R42	N	33	AF39	AT38	N
18	N38	R41	P	35	AF38	AR37	P
19	P36	G38	N	37	AG34	AH42	N
20	P35	H37	P	39	AG33	AH41	P
21	P39	J38	N	41	AH38	AK42	N
22	P38	J39	P	43	AH37	AK41	P
23	R35	L38	N	45	AJ37	AM42	N
24	R34	L39	P	47	AJ36	AM41	P
25	R39	M36	N	49	AJ35	AN42	N
26	R38	M35	P	51	AJ34	AN41	P
27	T38	N40	N	53	AJ39	AP42	N
28	T37	N39	P	55	AJ38	AP41	P
29	U35	R38	N	57	AK36	AT42	N
30	U34	R37	P	59	AK35	AT41	P
31	V35	U40	N	61	AK39	AU42	N
32	V34	U39	P	63	AK38	AU41	P
33	V37	W38	N	65	AL34	AV42	N
34	V36	W37	P	67	AL33	AV41	P
35	W35	AA37	N	69	AL39	AW42	N
36	W34	AA36	P	71	AL38	AW41	P

12. Recovered Clock Monitor Headers

There are 16 or 20 2-pin headers connected to user I/O pins near the top and bottom of the FPGA. These headers are intended to be used to monitor the recovered clock for each RocketIO transceiver as shown in Table 14. Note, if these headers are not being used to monitor the clocks, they may be used for any other purpose the user sees fit.

Table 14: **Recovered Clock Monitor Pins**

Label	ML324	ML325
	Pin	Pin
J136	C11	C11
J135	D11	C15
J53		K13
J10	C14	F19
J30	C15	M21
J12	C22	H23
J39	C23	D24
J96	C29	L27
J50		F30
J134	C30	G31
J13	AU10	AT12
J54		AT13
J28	AU11	AY15
J140	AU14	AW19
J139	AU15	AV20
J137	AU22	AR23
J138	AU23	AY24
J20	AU29	AY28
J141		AU30
J11	AU30	AN31

13. Program Switch (Active Low)

The active-low program switch, when pressed, grounds the program pin on the FPGA.

14. Reset Switch (Active Low)

The active-low reset switch resets the System ACE controller.

15. DONE LED

The DONE LED indicates the status of the **DONE** pin on the FPGA. This LED lights when **DONE** is high or if power is applied to the board without a part in the socket.

16. INIT LED

The INIT LED lights during initialization.

17. Config Address DIP Switch

This switch (SW5) is used to select one of eight addresses in the CompactFlash memory card, from which a configuration bitstream can be read. The open ("O") position indicates a logic '0' and the closed ("C") position indicates a logic '1' as shown in Table 15.

Table 15: **Bitstream Address Table**

2	1	0	Addr
O	O	O	0
O	O	C	1
O	C	O	2
O	C	C	3
C	O	O	4
C	O	C	5
C	C	O	6
C	C	C	7

18. RocketIO Transceiver Pins

The RocketIO transceiver pins are as shown in Table 16.

Table 16: **RocketIO TX and RX Pin Pairs**

MGT	ML324				ML325			
	TXP	TXN	RXP	RXN	TXP	TXN	RXP	RXN
2	A35	A36	A34	A33	A40	A41	A39	A38
3					A36	A37	A35	A34
4	A31	A32	A30	A29	A32	A33	A31	A30
5	A27	A28	A26	A25	A28	A29	A27	A26
6	A23	A24	A22	A21	A24	A25	A23	A22
7	A18	A19	A17	A16	A20	A21	A19	A18
8	A14	A15	A13	A12	A16	A17	A15	A14
9	A10	A11	A9	A8	A12	A13	A11	A10
10					A8	A9	A7	A6
11	A6	A7	A5	A4	A4	A5	A3	A2
14	AW6	AW7	AW5	AW4	BB4	BB5	BB3	BB2
15					BB8	BB9	BB7	BB6
16	AW10	AW11	AW9	AW8	BB12	BB13	BB11	BB10
17	AW14	AW15	AW13	AW12	BB16	BB17	BB15	BB14
18	AW18	AW19	AW17	AW16	BB20	BB21	BB19	BB18
19	AW23	AW24	AW22	AW21	BB24	BB25	BB23	BB22
20	AW27	AW28	AW26	AW25	BB28	BB29	BB27	BB26
21	AW31	AW32	AW30	AW29	BB32	BB33	BB31	BB30
22					BB36	BB37	BB35	BB34
23	AW35	AW36	AW34	AW33	BB40	BB41	BB39	BB38

Note: Shaded areas denote pins that are not used.

19. RS-232 Port Pins

The RS-232 port pins are as shown in Table 17. The pins are set up in DTE mode as shown in Figure 3.

Table 17: **RS-232 Port Pins**

FPGA UART Port Name	Direction	Net	ML324	ML325
TXD	OUT	T1IN	AK25	AV34
RTS	OUT	T2IN	AP26	AU34
RXD	IN	R1OUT	AR26	AR34
CTS	IN	R2OUT	AM25	AT34

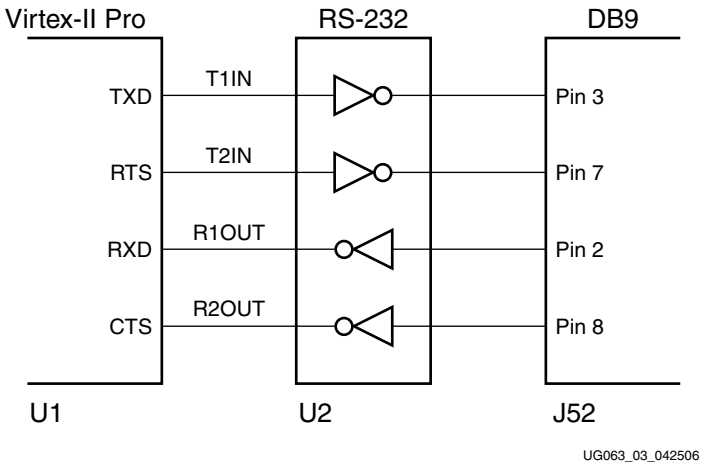

Figure 3: **RS-232 Pins in DTE Mode**

20. SDRAM Connection

The ML32x platform has 128Mb SDRAM on-board memory, Micron part number MT48V4M32LFFC-8. The connections to the Virtex-II Pro FPGA are shown in Table 18 (which spans multiple pages).

Table 18: **Headers for the SDRAM Signals**

		ML324	ML325			ML324	ML325
Pin	**Name**	**PIN**	**PIN**	**Pin**	**Name**	**PIN**	**PIN**
R9	DQ2	AE1	R1	A1	DQ26	K2	F1
R8	DQO	AE2	R2	A2	DQ24	L1	F2
R7	VDD4	VCCO	VCCO	A3	VSS1	GND	GND
R3	VSS4	GND	GND	A7	VDD1	VCCO	VCCO
R2	DQ15	AJ1	V2	A8	DQ23	L3	J2
R1	DQ13	AJ2	W1	A9	DQ21	M3	K1
P9	DQ4	AD2	P2	B1	DQ28	K1	E2
P8	VSSQ11	FILTERED GND	FILTERED GND	B2	VDDQ1	FILTERED VCCO	FILTERED VCCO
P7	VDDQ11	FILTERED VCCO	FILTERED VCCO	B3	VSSQ1	FILTERED GND	FILTERED GND
P3	VSSQ10	FILTERED GND	FILTERED GND	B7	VDDQ2	FILTERED VCCO	FILTERED VCCO
P2	VDDQ10	FILTERED VCCO	FILTERED VCCO	B8	VSSQ2	FILTERED GND	FILTERED GND
P1	DQ11	AK1	W2	B9	DQ19	R2	K2
N9	VDDQ9	FILTERED VCCO	FILTERED VCCO	C1	VSSQ3	FILTERED GND	FILTERED GND
N8	DQ3	AC2	P1	C2	DQ27	J1	E1
N7	DQ1	AF1	T2	C3	DQ25	L2	G1
N3	DQ14	AH2	V1	C7	DQ22	K3	J1
N2	DQ12	AK2	Y3	C8	DQ20	T2	L1
N1	VSSQ9	FILTERED GND	FILTERED GND	C9	VDDQ3	FILTERED VCCO	FILTERED VCCO
M9	VDDQ8	FILTERED VCCO	FILTERED VCCO	D1	VSSQ4	FILTERED GND	FILTERED GND
M8	DQ5	AC1	N2	D2	DQ29	J2	D2
M7	DQ6	AF2	U1	D3	DQ30	N1	G2
M3	DQ9	AG2	U2	D7	DQ17	J3	H2
M2	DQ10	AL1	Y4	D8	DQ18	U2	L2

Table 18: **Headers for the SDRAM Signals *(Continued)***

		ML324	ML325			ML324	ML325
Pin	Name	PIN	PIN	Pin	Name	PIN	PIN
M1	VSSQ8	FILTERED GND	FILTERED GND	D9	VDDQ4	FILTERED VCCO	FILTERED VCCO
L9	VSSQ7	FILTERED GND	FILTERED GND	E1	VDDQ5	FILTERED VCCO	FILTERED VCCO
L8	DQ7	AB2	N1	E2	DQ31	H2	D1
L7	VDD3	VCCO	VCCO	E3	NC1	NC	NC
L3	VSS3	GND	GND	E7	NC2	NC	NC
L2	DQ8	AL2	AA3	E8	DQ16	V2	M2
L1	VDDQ6	FILTERED VCCO	FILTERED VCCO	E9	VSSQ5	FILTERED GND	FILTERED GND
K9	DQM0	AH3	E3	F1	VSS2	GND	GND
K8	WE#	AG3	F3	F2	DQM3	P1	U3
K7	CAS#	AF3	G3	F3	A3	N2	D3
K3	NC5	NC	NC	F7	A2	P2	G4
K2	NC4	NC	NC	F8	DQM2	R1	H4
K1	DQM1	AE3	H3	F9	VDD2	VCCO	VCCO
J9	RAS#	AD3	K3	G1	A4	P3	J4
J8	CS#	HEADER J49	HEADER J166	G2	A5	N3	L4
J7	BA0	AB4	L3	G3	A6	R3	M4
J3	A9	AB3	M3	G7	A10	T3	N4
J2	CKE	AA4	N3	G8	A0	U4	T4
J1	CLK	AG20	AP21	G9	A1	V3	U4
H9	NC/A11	Y3	P3	H1	A7	V4	V4
H8	BA1	W4	R3	H2	A8	W3	W3
H7	NC/A12	NC	T3	H3	NC3	NC	NC

Note:

1. For proper operation of the SDRAM, use the LVCMOSDCI25 voltage standard on the FPGA pins.
2. CS# is tied to the jumper labeled RAM_ENABLE/RAM_DISABLE.
3. Disable the SDRAM when using the DUT pins as standard I/O pins.
4. For information on SDRAM operation, see: http://www.micron.com/products/dram/sdram/

Document status refers to the internal classification of the document. This classification can affect how and to whom the document is distributed.