PHY Daughter Card User Guide

For ML32x Development Platforms

UG065 (v1.0) P/N 0402279 May 5, 2004

XILINX®

The following table shows the revision history for this document..

	Version	Revision
05/05/04	1.0	Initial Xilinx release.

About This Guide

This guide documents the PHY daughter card for use with Xilinx ML32x Development Platforms.

Additional Resources

For additional information, go to http://support.xilinx.com. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging http://support.xilinx.com/support/techsup/tutorials/index.htm
Answer Browser	Database of Xilinx solution records http://support.xilinx.com/xlnx/xil_ans_browser.jsp
Application Notes	Descriptions of device-specific design techniques and approaches http://support.xilinx.com/apps/appsweb.htm
Data Sheets	Device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging http://support.xilinx.com/xlnx/xweb/xil_publications_index.jsp
Problem Solvers	Interactive tools that allow you to troubleshoot your design issues http://support.xilinx.com/support/troubleshoot/psolvers.htm
Tech Tips	Latest news, design tips, and patch information for the Xilinx design environment http://www.support.xilinx.com/xlnx/xil_tt_home.jsp

Conventions

This document uses the following conventions. An example illustrates each convention.

Online Document

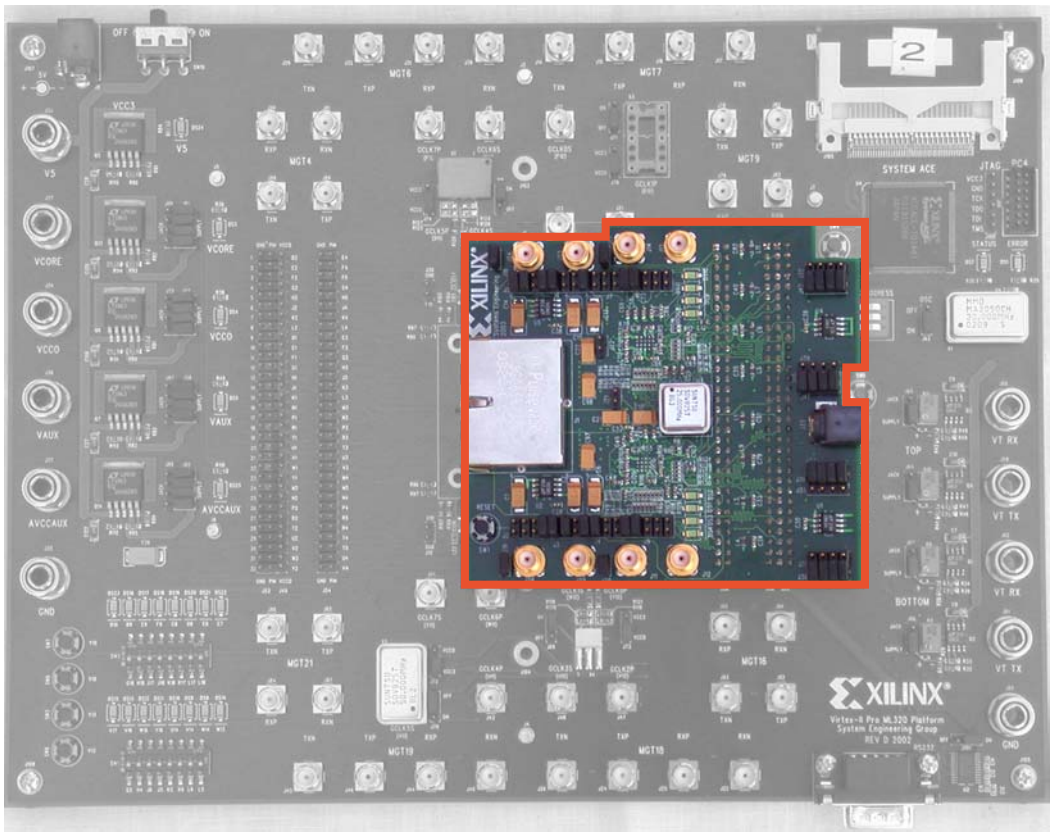
The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Handbook*.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

PHY Daughter Card

Overview

The PHY daughter card provides Ethernet capability to Xilinx ML32x Development Platforms by using two Marvell Alaska Gigabit Ethernet over copper transceivers, 88E1111. These PHY devices can perform all physical layer (PHY) functions, can operate at 10/100/1000 Mb/s, and support many interfaces to the MAC. The PHY daughter card connects to ML32x boards through the J55 and J56 headers as shown in Figure 1.



UG065_01_042704

Figure 1: **PHY Daughter Card Connected to an ML320 Board**

Features

The PHY daughter card features the following:

- Two Marvell Alaska PHY devices (88E1111) with 10/100/1000 Mb/s operation
- Support for the following interfaces:
  - GMII/MII
  - SGMII
  - RGMII
- Two power connection options:
  - ML32x header pins
  - 5V external power jack
- Two-port RJ-45 connector
- 2.5V - 25 MHz crystal oscillator for both PHY devices
- SMA connectors for the SGMII interface

Power Settings

The ML32x PHY daughter card can be powered up either through the V_{CC} pins of the ML32x board when the daughter card is connected to it, or through an external power 5V jack if used on other boards.

To power the daughter card from the V_{CC} pins of the ML32x board through the headers, set the jumpers according to Figure 2.

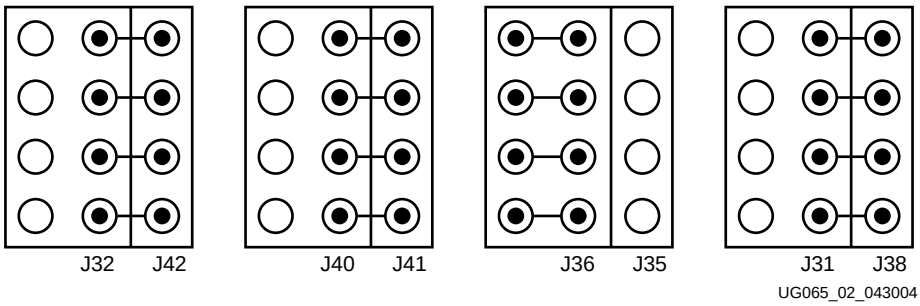


Figure 2: **Jumper Settings to Power Up from an ML32x Board**

To power the daughter card from the 5V jack connector, set the jumpers according to Figure 3.

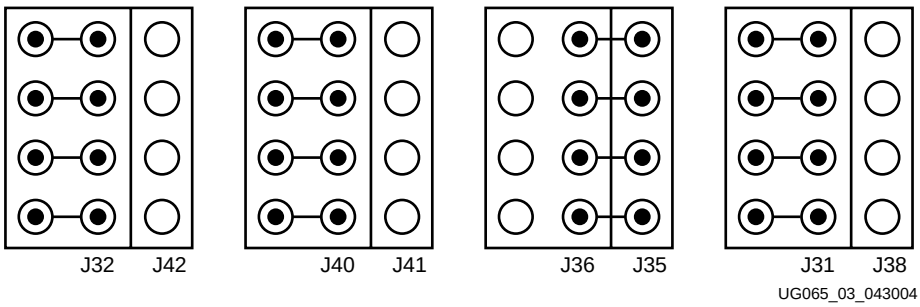


Figure 3: **Jumper Settings to Power Up from 5V Jack Connector**

Signal Connectivity

Table 1 shows the signal connections between the PHY daughter card and the ML320, ML321, and ML323 Platforms.

Table 1: **Connections Between the PHY Daughter Card and the ML32x**

J15	J56			J16	J55		
PHY	ML320	ML321	ML323	PHY	ML320	ML321	ML323
1 - P1_TXD1	E19	E23	K31	1 -	D21	A25	N33
3 - P1_TXEN	F19	G23	L32	3 - P1_RXC_RXCLK	E21	C25	P33
5 - P1_GTXCLK	F18	H23	M32	5 - P1_RXD1	F21	D25	R33
7 - P1_COL	G19	J23	N32	7 - P1_RXCTL_RXDV	G21	E25	T33
9 - P1_TXD3	H19	E24	P32	9 - P1_RCLK1	H21	H25	U33
11 - P1_TXD2	J19	G24	R32	11 - P1_CRS	J21	B26	V33
13 -	K19	H24	T32	13 - P1_RXER	K21	C26	E34
15 - P1_TXD0	L19	J24	U32	15 - P1_RXD7	L21	D26	F30
17 - P1_TXD7	E20	K24	E33	17 - P1_RXD0	D22	E26	L31
19 - P1_TXD6	F20	L24	E31	19 -	E22	F26	H34
21 - P1_TXD5	G20	M24	F31	21 - P1_RXD2	F22	G26	K34
23 - P1_TXD4	H20	N24	H33	23 - P1_RXD3	G22	H26	L34
25 - P1_MDC	J20	J25	J33	25 - P1_RXD4	H22	J26	M34
27 - P1_MDIO	K20	L25	K33	27 - P1_RXD5	J22	K26	N34
29 - P1_TXER	L20	M25	L33	29 - P1_RXD6	K22	L26	P34
31 - P1_INT	M20	N25	M33	31 - P0_CRS	N22	M26	R34
33 - P0_COL	N20	P25	AD33	33 -	P22	R26	Y34
35 - P0_TXD7	P20	R25	AE33	35 - P0_RXD0	R22	T26	AA34
37 - P0_INT	R20	P24	AF33	37 - P0_RXD1	T22	U26	AB34
39 - P0_TXD6	T20	R24	AD31	39 -	U22	V26	AC34
41 - P0_TXD5	U20	T24	AH30	41 - P0_RXD2	V22	W26	AD34
43 - P0_TXD4	V20	U24	AK31	43 -	W22	Y26	AE34
45 - P0_TXD3	M19	V24	AL33	45 - P0_RXCTL_RXDV	Y22	AA26	AG34
47 - P0_TXD2	M18	W24	V32	47 - P0_RXD4	M21	AC26	AD32
49 - P0_TXD1	N19	Y24	W32	49 - P0_RXD5	N21	AD26	AE30
51 - P0_TXD0	P19	AB24	Y32	51 - P0_RXD6	P21	AE26	AK32
53 - P0_MDC	R18	AC24	AA32	53 - P0_RXD7	R21	T25	AL34
55 - P0_MDIO	R19	AD23	AB32	55 - P0_RCLK1	T21	V25	W33
57 - RESET	T19	U23	AC32	57 - P0_RXD3	U21	W25	Y33

Table 1: **Connections Between the PHY Daughter Card and the ML32x *(Continued)***

J15	J56			J16	J55		
PHY	ML320	ML321	ML323	PHY	ML320	ML321	ML323
59 - P0_GTXCLK	U18	V23	AF32	59 - P0_RXER	V21	AC25	AA33
61 - P0_TXEN	U19	W23	AD30	61 - P0_RXC_RXCLK	W21	AD25	AB33
63 - P0_TXER	V19	Y23	AE31	63 -	Y21	AF25	AC33

Configuration Settings

The Marvell Alaska PHY can be configured with several options such as the physical address, the PHY operating mode, auto-negotiation, the physical connection type, and others. The CONFIG[6:0] pins are used to set these options. Please refer to the ML32x PHY daughter card schematic attached to this document, specifically to sheets 7 and 8 for PHY0 and PHY1, respectively, and to the Marvell Alaska PHY data sheet for details.

The CONFIG[6:0] pins must be tied to one of the pins as shown in Table 2. These seven CONFIG pins should not be left floating. The pins shown in Table 2 are LEDs, V_{DDO}, and V_{SS} pins of the PHY where each pin encodes a 3-bit constant value.

Table 2: **Pin to Constant Mapping**

Pin	Bit[2:0]
P0_VDDOH / P1_VDDOH	111
P0_LED_LINK10 / P1_LED_LINK10	110
P0_LED_LINK100 / P1_LED_LINK100	101
P0_LED_LINK1000 / P0_LED_LINK1000	100
P0_LED_DUPLEX / P1_LED_DUPLEX	011
P0_LED_RX / P1_LED_RX	010
P0_LED_TX / P1_LED_TX	001
VSS (GND)	000

Table 3 shows the configuration register map to the CONFIG[6:0] pins of the Marvell Alaska PHY 88E1111.

Table 3: **Pin to Configuration Register Mapping**

Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_BDT	INT_POL	75/50 OHM

These configuration options are described in the Hardware Configuration section of the PHY data sheet. These options, except for the PHY address configuration, can be overwritten by writing to the registers through the MDIO interface. Table 4 lists the options available by setting jumpers on the configuration header pins of the PHY daughter card.

Table 4: **Configuration Options on the ML32x PHY Daughter Card**

Configuration Signal	Option	Signal	Configuration Register
CONFIG0	PHYADR = 00000	VSS	PHYADR[2:0] = 000
CONFIG0	PHYADR = 00001	P0_LED_TX / P1_LED_TX	PHYADR[2:0] = 001
CONFIG1		VSS	ENA_PAUSE = 0; PHYADR[4:3] = 00
CONFIG2	Auto-Neg, 1000 Base-T, FD, Master	P0_LED_LINK100 / P1_LED_LINK100	ANEG[3:1] = 101
CONFIG3		P0_LED_TX / P1_LED_TX	ANEG[0] = 0; ENA_XC = 0; DIS_125 = 1
CONFIG4	SGMII to Cu w/o clock, w/ auto-neg	P0_LED_LINK1000 / P1_LED_LINK1000	HWCFG_MODE[2:0] = 100
CONFIG4	RGMII, w/ modified MII in 10/100 Cu	P0_LED_DUPLEX / P1_LED_DUPLEX	HWCFG_MODE[2:0] = 011
CONFIG4	GMII to Cu	P0_VDDOH / P1_VDDOH	HWCFG_MODE[2:0] = 111
CONFIG4	RTBI to Cu	P0_LED_TX / P1_LED_TX	HWCFG_MODE[2:0] = 001
CONFIG4	TBI to Cu	P0_LED_LINK100 / P1_LED_LINK100	HWCFG_MODE[2:0] = 101
CONFIG5	SGMII/TBI to Cu	P0_LED_LINK1000 / P1_LED_LINK1000	DIS_FC=1; DIS_SLEEP=0; HWCFG_MODE[3]=0
CONFIG5	GMII/RGMII/RTBI to Cu	P0_LED_LINK100 / P1_LED_LINK100	DIS_FC=1; DIS_SLEEP=0; HWCFG_MODE[3]=1
CONFIG6	50 Ohm	P0_LED_RX / P1_LED_RX	SEL_BDT = 0; INT_POL = 1; 75/50 OHM = 0

GMII

To set the PHY to operate in GMII mode, jumper the configuration headers as illustrated in Figure 4.

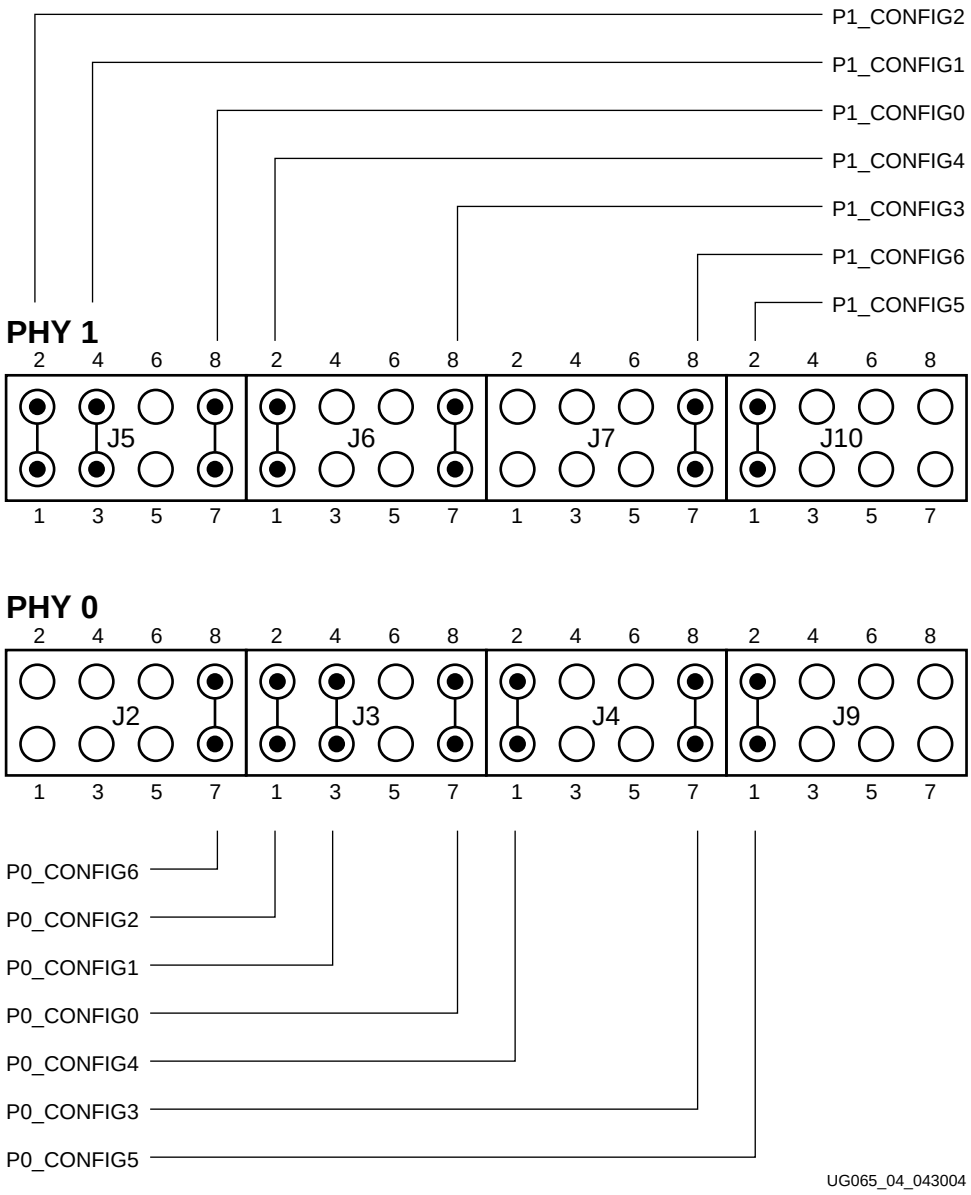


Figure 4: **Configuration Headers in GMII Mode**

Table 5: **Configuration Settings for GMII Mode**

Configuration Signal	Option	Signal	Configuration Register
CONFIG0	PHYADR = 00000	VSS	PHYADR[2:0] = 000
CONFIG1		VSS	ENA_PAUSE = 0; PHYADR[4:3] = 00
CONFIG2	Auto-Neg, 1000 Base-T, FD, Master	P0_LED_LINK100 / P1_LED_LINK100	ANEG[3:1] = 101
CONFIG3		P0_LED_TX / P1_LED_TX	ANEG[0] = 0; ENA_XC = 0; DIS_125 = 1
CONFIG4	GMII to Cu	P0_VDDOH / P1_VDDOH	HWCFG_MODE[2:0] = 111
CONFIG5	GMII/RGMII/RTBI to Cu	P0_LED_LINK100 / P1_LED_LINK100	DIS_FC=1; DIS_SLEEP=0; HWCFG_MODE[3]=1
CONFIG6	50 Ohm	P0_LED_RX / P1_LED_RX	SEL_BDT = 0; INT_POL = 1; 75/50 OHM = 0

RGMII

To set the PHY to operate in RGMII mode, jumper the configuration headers as illustrated in Figure 5.

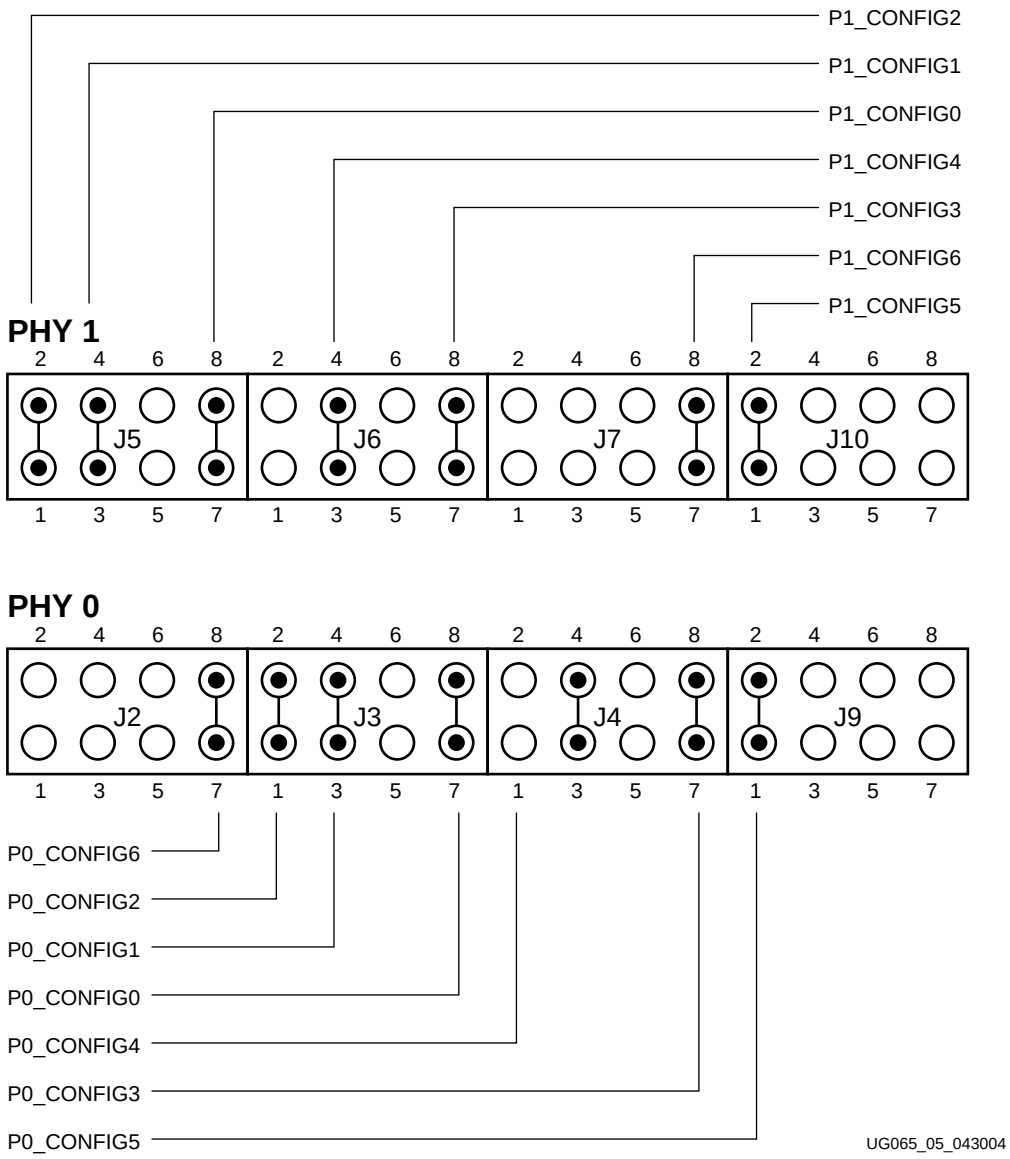


Figure 5: **Configuration Headers for RGMII Mode**

Table 6: **Configuration Settings for RGMII Mode**

Configuration Signal	Option	Signal	Configuration Register
CONFIG0	PHYADR = 00000	VSS	PHYADR[2:0] = 000
CONFIG1		VSS	ENA_PAUSE = 0; PHYADR[4:3] = 00
CONFIG2	Auto-Neg, 1000 Base-T, FD, Master	P0_LED_LINK100 / P1_LED_LINK100	ANEG[3:1] = 101
CONFIG3		P0_LED_TX / P1_LED_TX	ANEG[0] = 0; ENA_XC = 0; DIS_125 = 1
CONFIG4	RGMII, w/ modified MII in 10/100 Cu	P0_LED_DUPLEX / P1_LED_DUPLEX	HWCFG_MODE[2:0] = 011
CONFIG5	GMII/RGMII/RTBI to Cu	P0_LED_LINK100 / P1_LED_LINK100	DIS_FC=1; DIS_SLEEP=0; HWCFG_MODE[3]=1
CONFIG6	50 Ohm	P0_LED_RX / P1_LED_RX	SEL_BDT = 0; INT_POL = 1; 75/50 OHM = 0

SGMII

To set the PHY to operate in SGMII mode, jumper the configuration headers as illustrated in Figure 6.

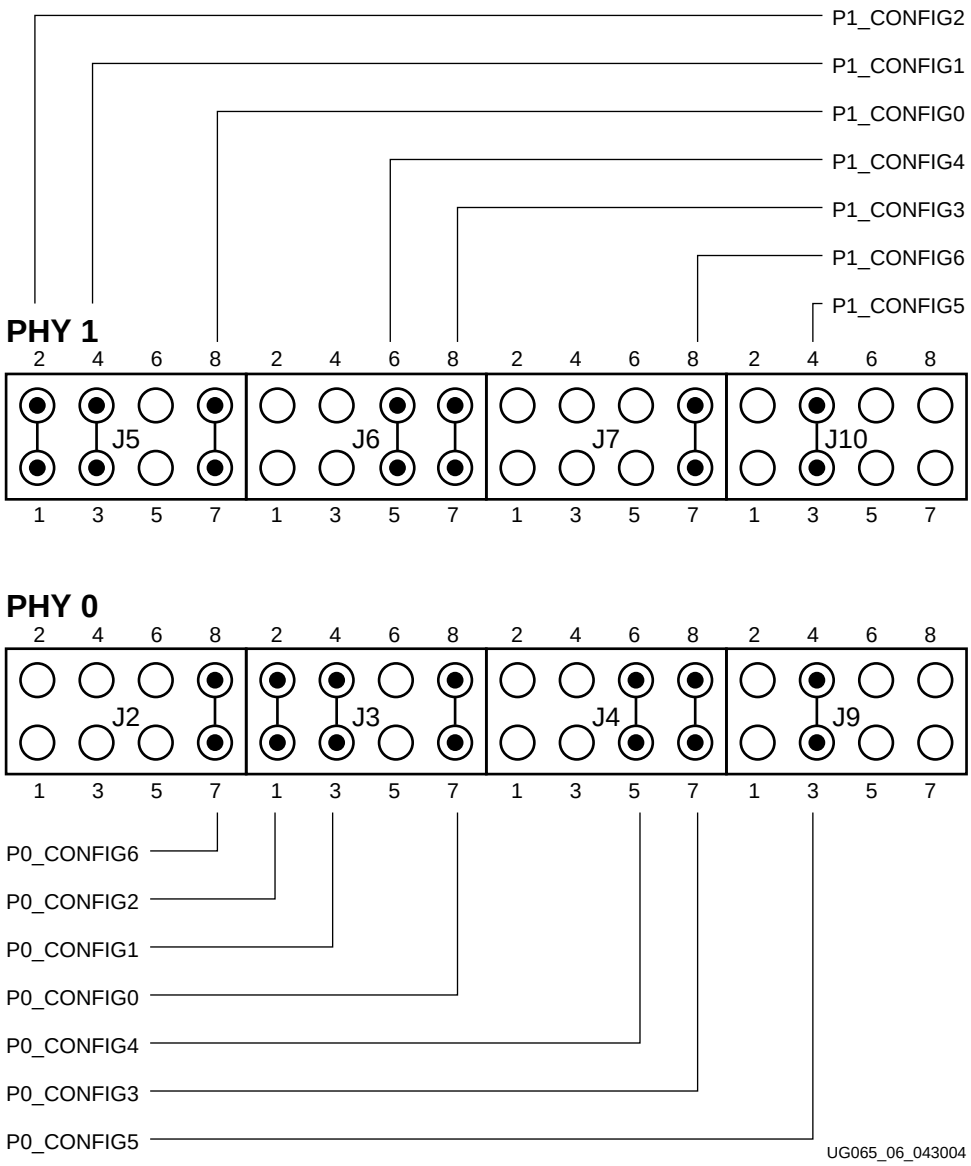


Figure 6: **Configuration Headers for SGMII Mode**

Table 7: **Configuration Settings for SGMII Mode**

Configuration Signal	Option	Signal	Configuration Register
CONFIG0	PHYADR = 00000	VSS	PHYADR[2:0] = 000
CONFIG1		VSS	ENA_PAUSE = 0; PHYADR[4:3] = 00
CONFIG2	Auto-Neg, 1000 Base-T, FD, Master	P0_LED_LINK100 / P1_LED_LINK100	ANEG[3:1] = 101
CONFIG3		P0_LED_TX / P1_LED_TX	ANEG[0] = 0; ENA_XC = 0; DIS_125 = 1
CONFIG4	SGMII to Cu w/o clock, w/ auto-neg	P0_LED_LINK1000 / P1_LED_LINK1000	HWCFG_MODE[2:0] = 100
CONFIG5	SGMII/TBI to Cu	P0_LED_LINK1000 / P1_LED_LINK1000	DIS_FC=1; DIS_SLEEP=0; HWCFG_MODE[3]=0
CONFIG6	50 Ohm	P0_LED_RX / P1_LED_RX	SEL_BDT = 0; INT_POL = 1; 75/50 OHM = 0

For SGMII operation, connect the SMA connectors of the PHY daughter card to the ML32x MGTs as follows:

- For PHY 1:
  - J24 to ML32x TXP
  - J23 to ML32x TXN
  - J13 to ML32x RXP
  - J14 to ML32x RXN
- For PHY 0:
  - J26 to ML32x TXP
  - J25 to ML32x TXN
  - J11 to ML32x RXP
  - J12 to ML32x RXN

MII

To set either PHY device in 10/100 Mb/s MII mode, the configuration headers for both devices must be connected together. The PHY devices must be set with auto-negotiation for any speed and for duplex capability. The speed and duplex are set by the other end to which the PHY daughter card is connected.

To set PHY 0 to work in MII mode, jumper the configuration headers as illustrated in Figure 7.

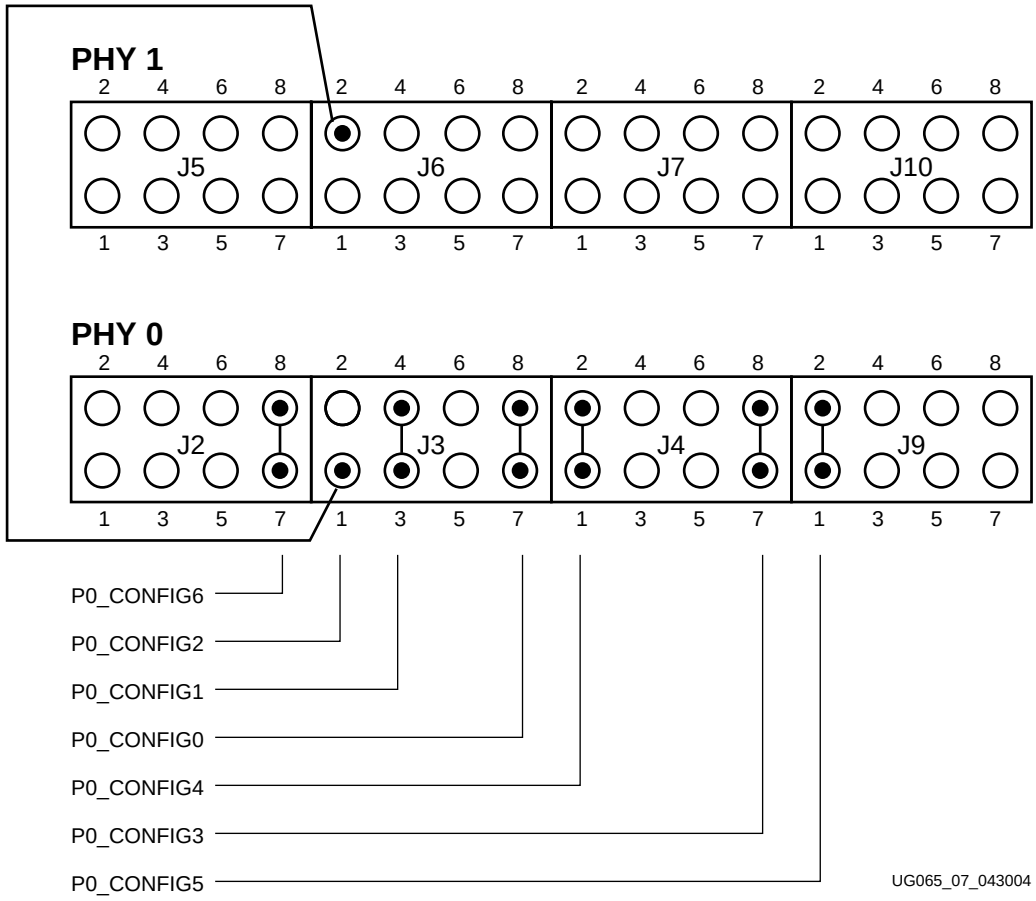


Figure 7: **Configuration Headers for PHY 0 in MII Mode**

Table 8: **Configuration Settings for MII Mode on PHY 0**

Configuration Signal	Options	Signal	Configuration Register
CONFIG0	PHYADR = 00000	VSS	PHYADR[2:0] = 000
CONFIG1		VSS	ENA_PAUSE = 0; PHYADR[4:3] = 00
CONFIG2	Auto-Neg, all capabilities, Master	P0_VDDOH / P1_VDDOH	ANEG[3:1] = 111
CONFIG3		P0_LED_TX / P1_LED_TX	ANEG[0] = 0; ENA_XC = 0; DIS_125 = 1
CONFIG4	GMII to Cu	P0_VDDOH / P1_VDDOH	HWCFG_MODE[2:0] = 111
CONFIG5	GMII/RGMII/RTBI to Cu	P0_LED_LINK100 / P1_LED_LINK100	DIS_FC=1; DIS_SLEEP=0; HWCFG_MODE[3]=1
CONFIG6	50 Ohm	P0_LED_RX / P1_LED_RX	SEL_BDT = 0; INT_POL = 1; 75/50 OHM = 0

To set PHY 1 to work in MII mode, jumper the configuration headers as illustrated in Figure 8.

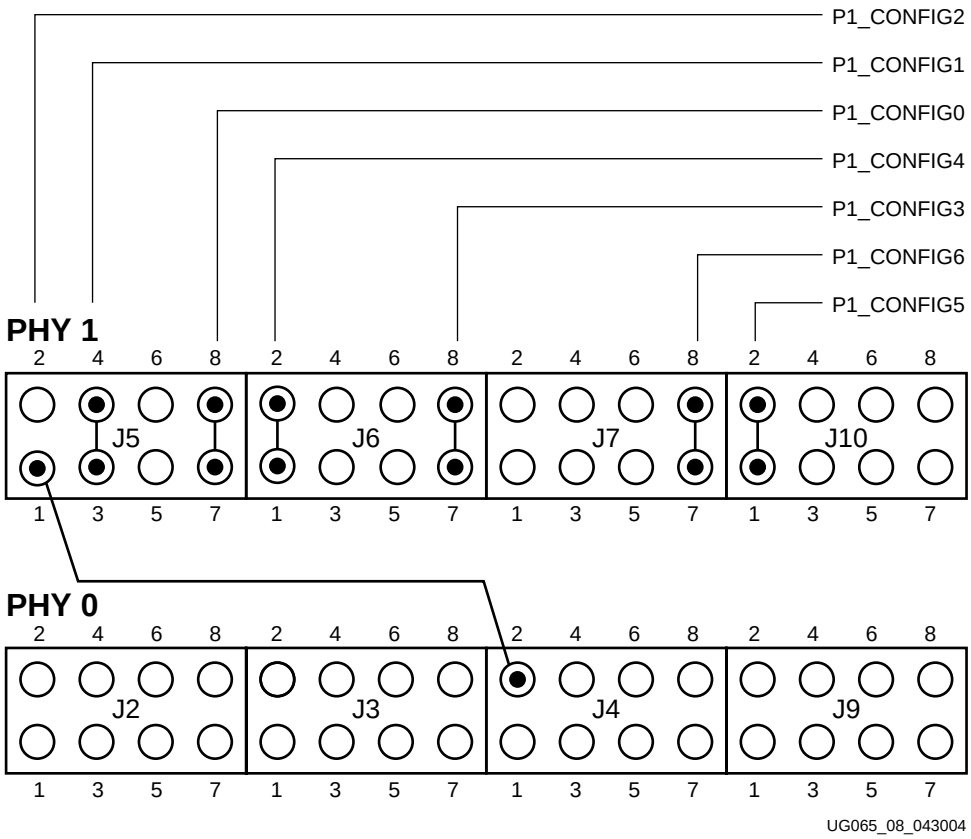


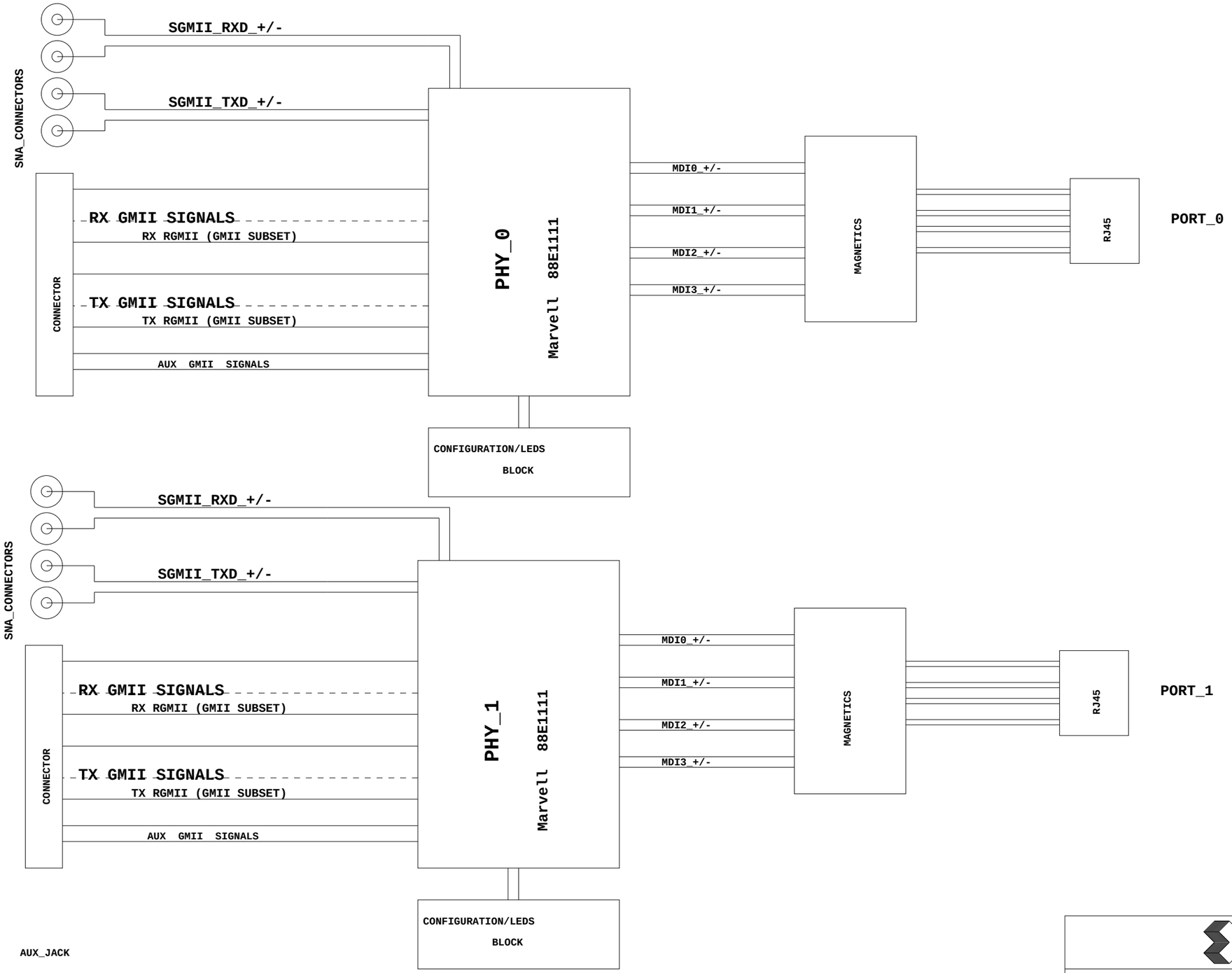
Figure 8: **Configuration Headers for PHY 1 in MII Mode**

Table 9: **Configuration Settings for MII Mode on PHY 1**

Configuration Signal	Options	Signal	Configuration Register
CONFIG0	PHYADR = 00000	VSS	PHYADR[2:0] = 000
CONFIG1		VSS	ENA_PAUSE = 0; PHYADR[4:3] = 00
CONFIG2	Auto-Neg, all capabilities, Master	P0_VDDOH / P1_VDDOH	ANEG[3:1] = 111
CONFIG3		P0_LED_TX / P1_LED_TX	ANEG[0] = 0; ENA_XC = 0; DIS_125 = 1
CONFIG4	GMII to Cu	P0_VDDOH / P1_VDDOH	HWCFG_MODE[2:0] = 111
CONFIG5	GMII/RGMII/RTBI to Cu	P0_LED_LINK100 / P1_LED_LINK100	DIS_FC=1; DIS_SLEEP=0; HWCFG_MODE[3]=1
CONFIG6	50 Ohm	P0_LED_RX / P1_LED_RX	SEL_BDT = 0; INT_POL = 1; 75/50 OHM = 0

References

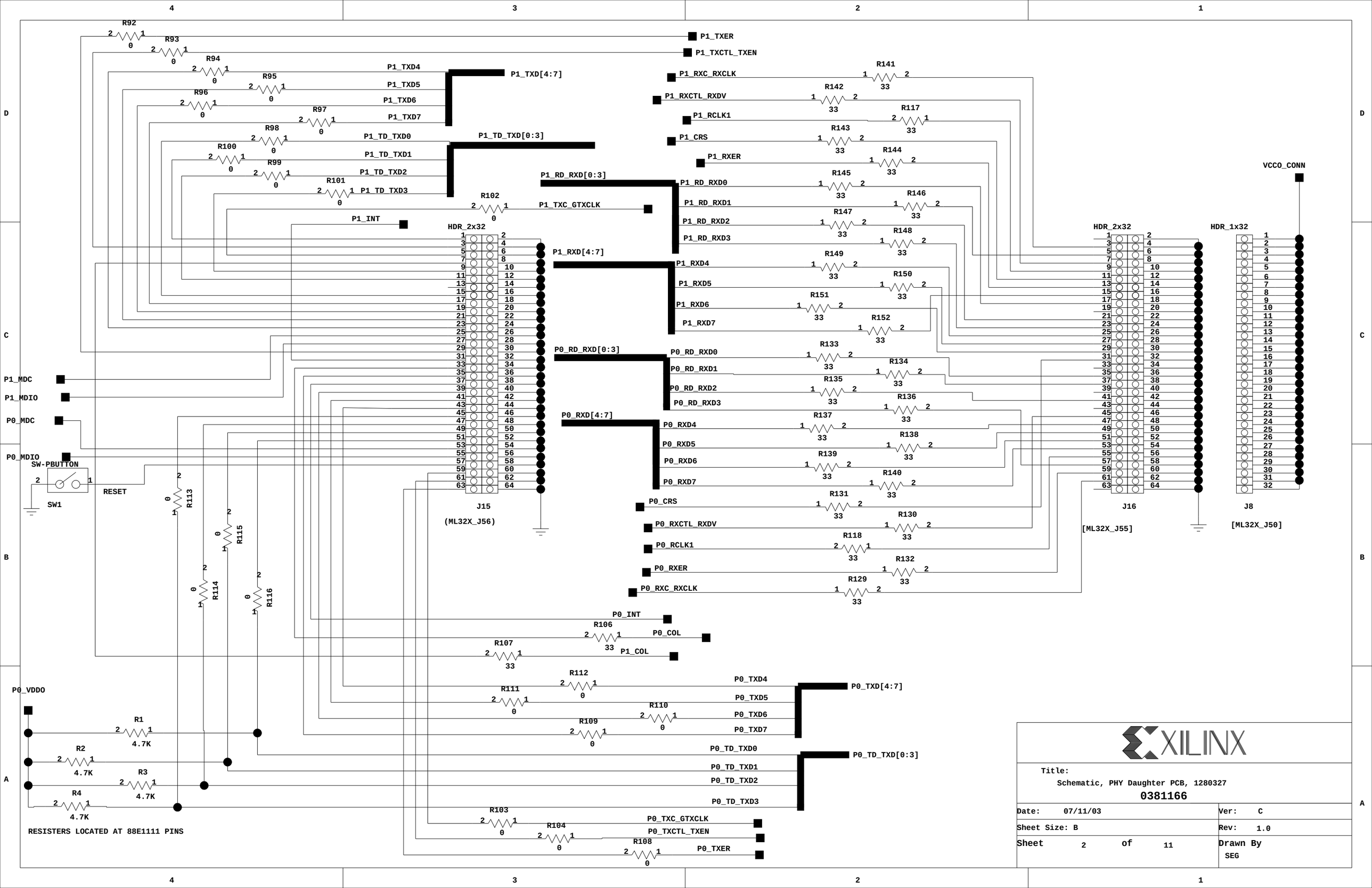
1. Marvell, Marvell Alaska 88E1111 Data Sheet (Available under NDA) http://www.marvell.com
2. Xilinx, Inc., Virtex-II Pro ML320, ML321, ML323 Platform User Guide
3. IEEE, IEEE Std 802.3, 2002 Edition



XILINX

Title:
Schematic, PHY Daughter PCB, 1280327
0381166

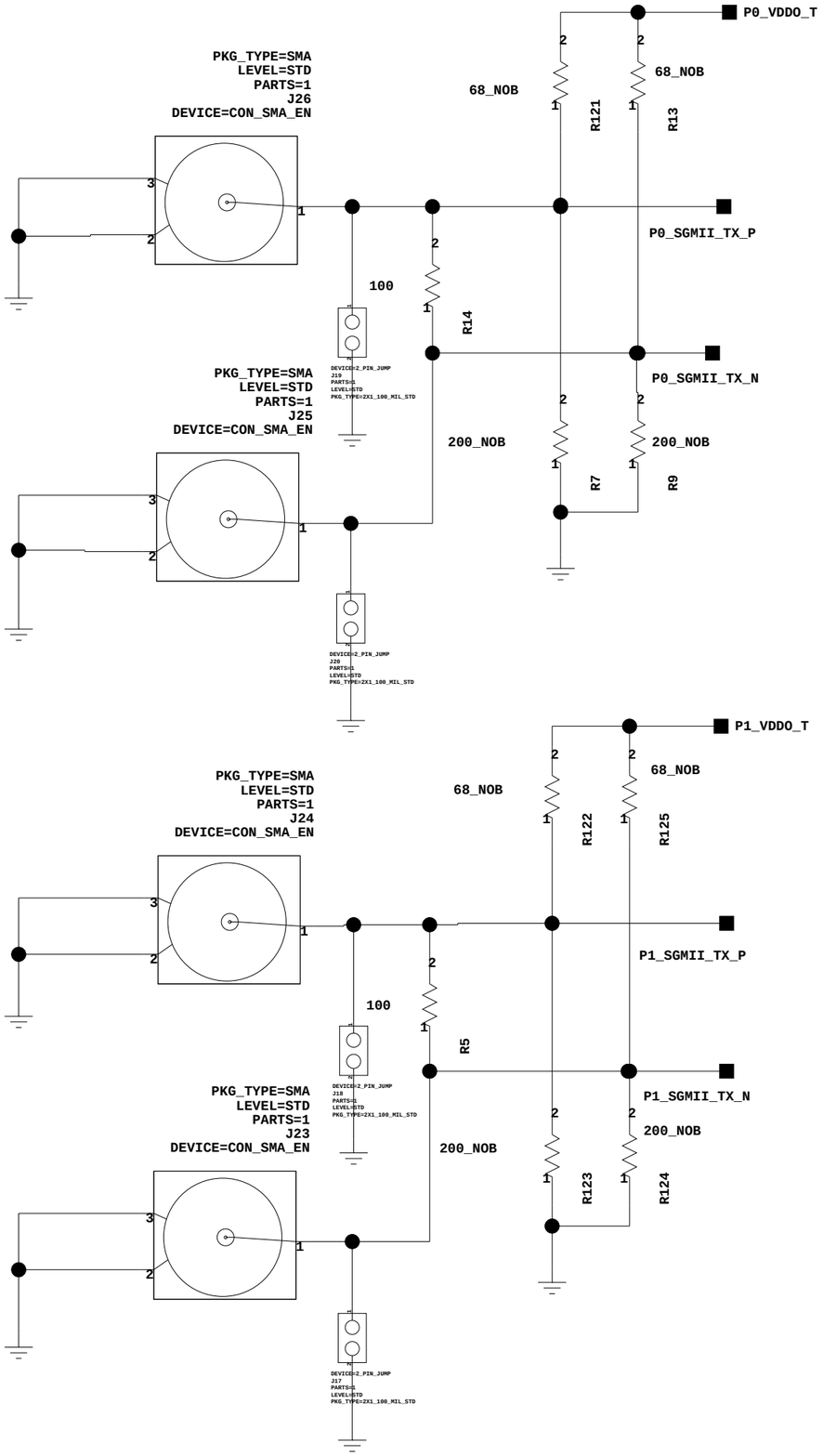
Date: 07/11/03	Ver: C
Sheet Size: B	Rev: 1.0
Sheet 1 of 11	Drawn By SEG

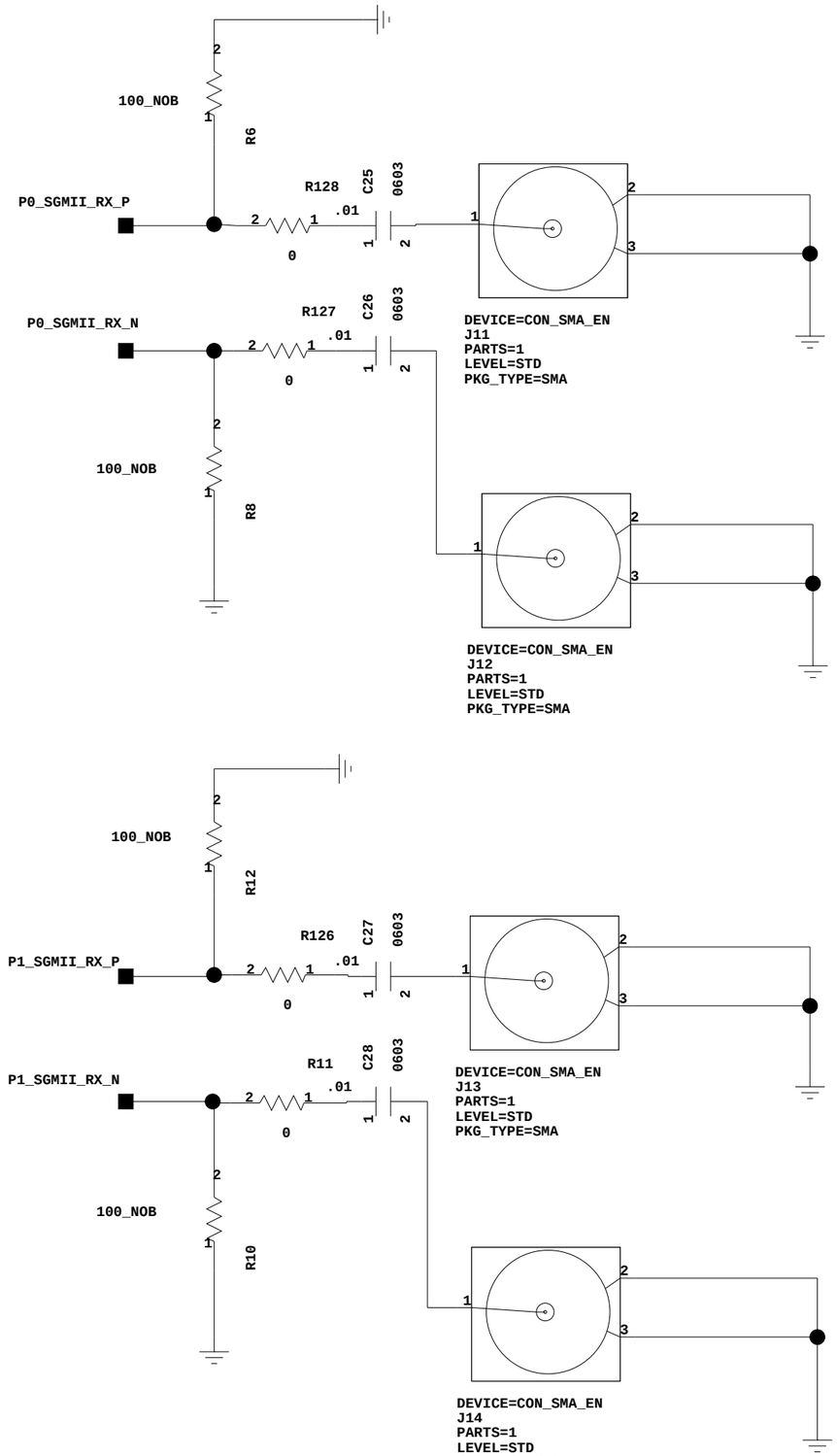


XILINX

Title:
Schematic, PHY Daughter PCB, 1280327
0381166

Date: 07/11/03	Ver: C
Sheet Size: B	Rev: 1.0
Sheet 2 of 11	Drawn By SEG

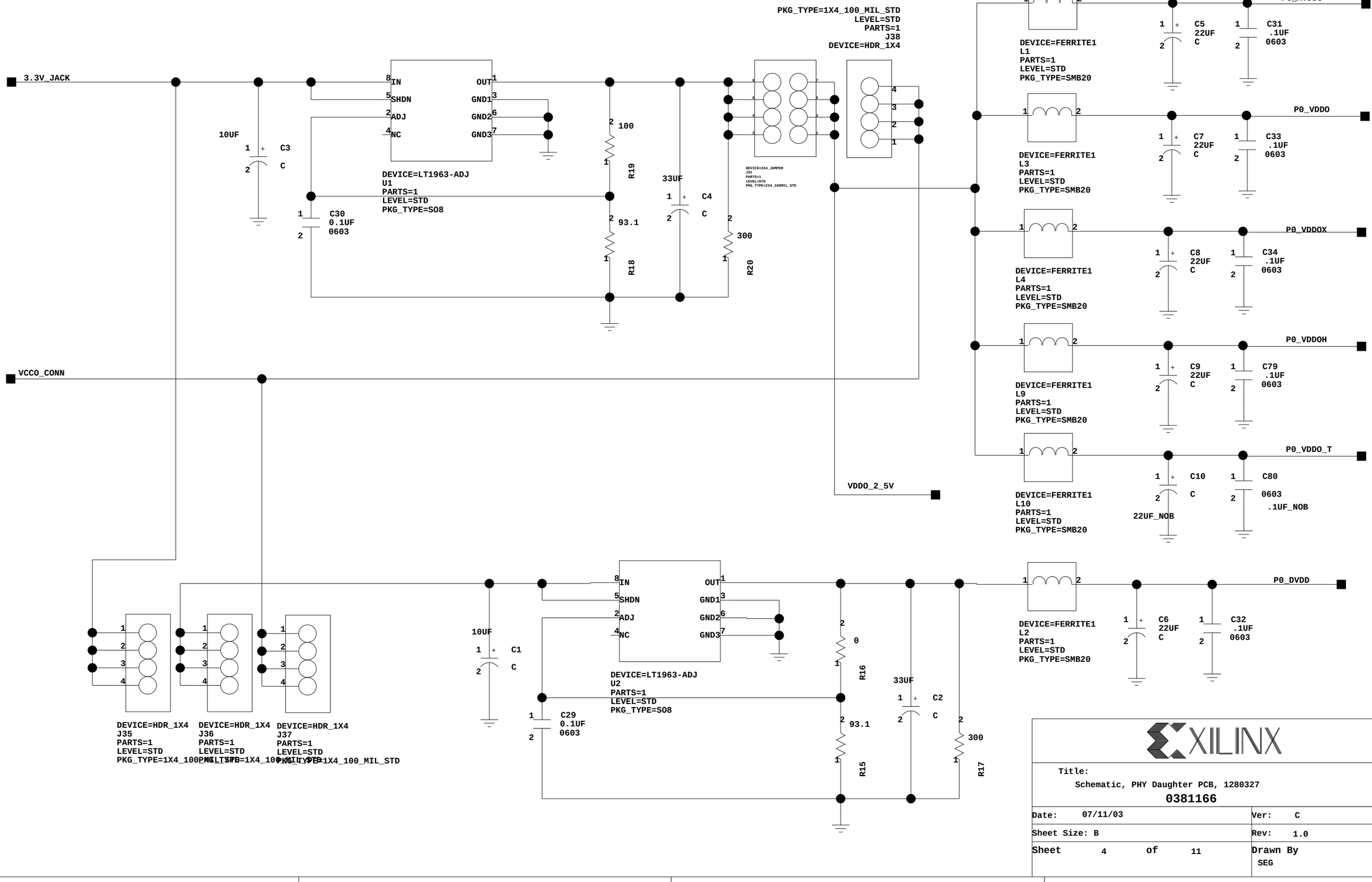




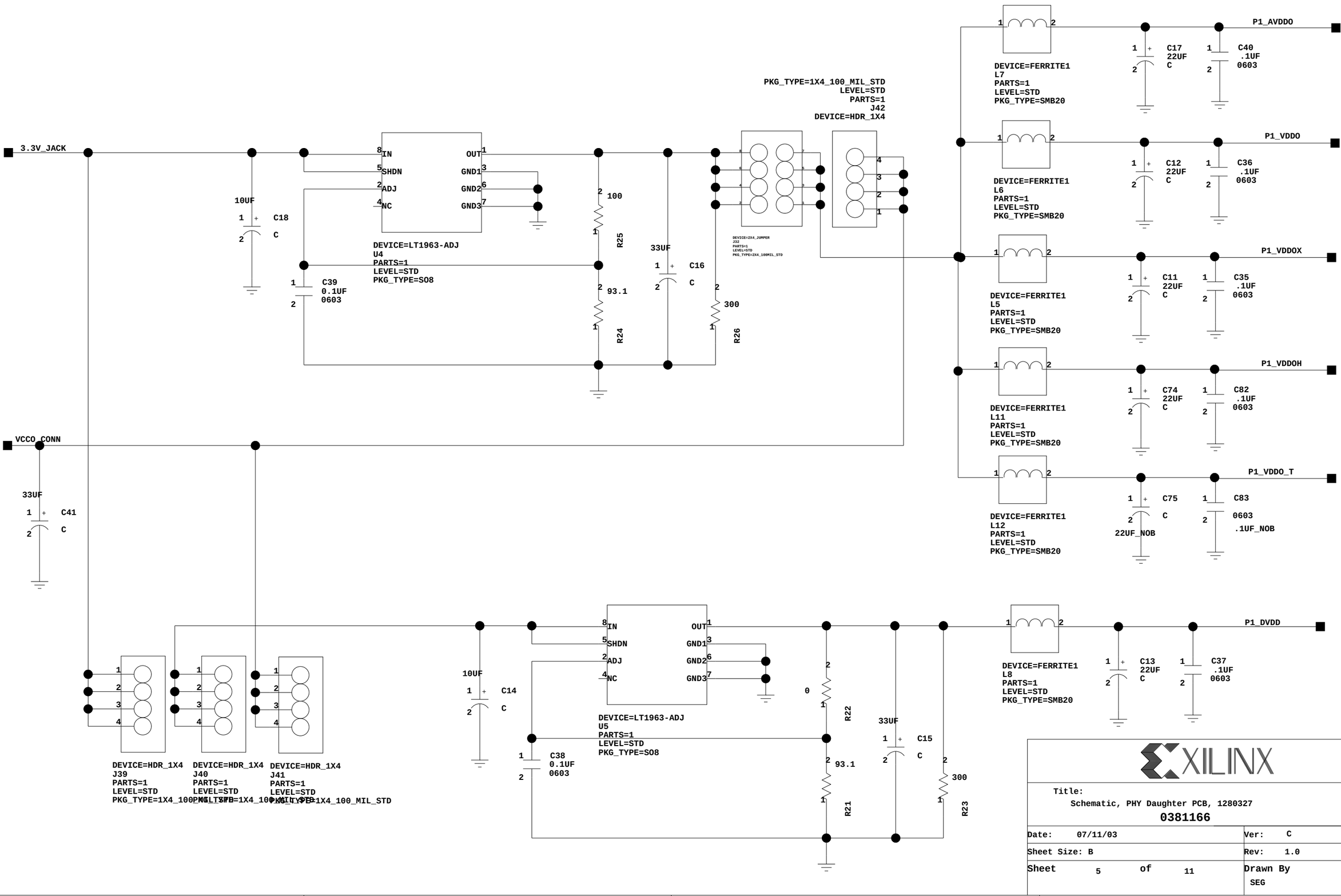
XILINX

Title:
Schematic, PHY Daughter PCB, 1280327
0381166

Date: 07/11/03	Ver: C
Sheet Size: B	Rev: 1.0
Sheet 3 of 11	Drawn By SEG

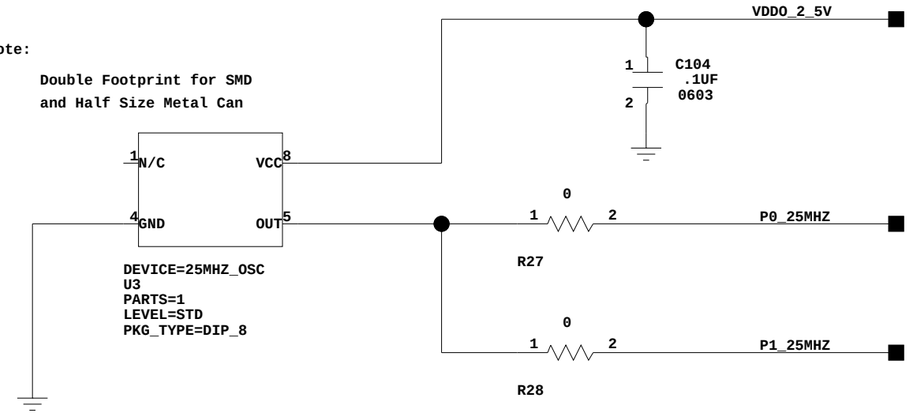


Title: Schematic, PHY Daughter PCB, 1280327	
0381166	
Date: 07/11/03	Ver: C
Sheet Size: B	Rev: 1.0
Sheet 4 of 11	Drawn By SEG


3.3V_JACK
10UF
C18
C
C39
0.1UF
0603
DEVICE=LT1963-ADJ
U4
PARTS=1
LEVEL=STD
PKG_TYPE=SO8
IN
SHDN
ADJ
NC
OUT
GND1
GND2
GND3
100
R25
93.1
R24
33UF
C16
300
R26
PKG_TYPE=1X4_100_MIL_STD
LEVEL=STD
PARTS=1
J42
DEVICE=HDR_1X4
DEVICE=2X4_JUMPER
J32
PARTS=1
LEVEL=STD
PKG_TYPE=2X4_100MIL_STD
P1_AVDDO
DEVICE=FERRITE1
L7
PARTS=1
LEVEL=STD
PKG_TYPE=SMB20
C17
22UF
C
C40
.1UF
0603
P1_VDDO
DEVICE=FERRITE1
L6
PARTS=1
LEVEL=STD
PKG_TYPE=SMB20
C12
22UF
C
C36
.1UF
0603
P1_VDDOX
DEVICE=FERRITE1
L5
PARTS=1
LEVEL=STD
PKG_TYPE=SMB20
C11
22UF
C
C35
.1UF
0603
P1_VDDOH
DEVICE=FERRITE1
L11
PARTS=1
LEVEL=STD
PKG_TYPE=SMB20
C74
22UF
C
C82
.1UF
0603
P1_VDDO_T
DEVICE=FERRITE1
L12
PARTS=1
LEVEL=STD
PKG_TYPE=SMB20
C75
22UF_NOB
C
C83
0603
.1UF_NOB
VCCO_CONN
33UF
C41
C
DEVICE=HDR_1X4
J39
PARTS=1
LEVEL=STD
PKG_TYPE=1X4_100_MIL_STD
DEVICE=HDR_1X4
J40
PARTS=1
LEVEL=STD
DEVICE=HDR_1X4
J41
PARTS=1
LEVEL=STD
10UF
C14
C
C38
0.1UF
0603
DEVICE=LT1963-ADJ
U5
PARTS=1
LEVEL=STD
PKG_TYPE=SO8
0
R22
93.1
R21
33UF
C15
C
300
R23
P1_DVDD
DEVICE=FERRITE1
L8
PARTS=1
LEVEL=STD
PKG_TYPE=SMB20
C13
22UF
C
C37
.1UF
0603
XILINX
Title:
Schematic, PHY Daughter PCB, 1280327
0381166
Date: 07/11/03
Ver: C
Sheet Size: B
Rev: 1.0
Sheet 5 of 11
Drawn By
SEG

Note:

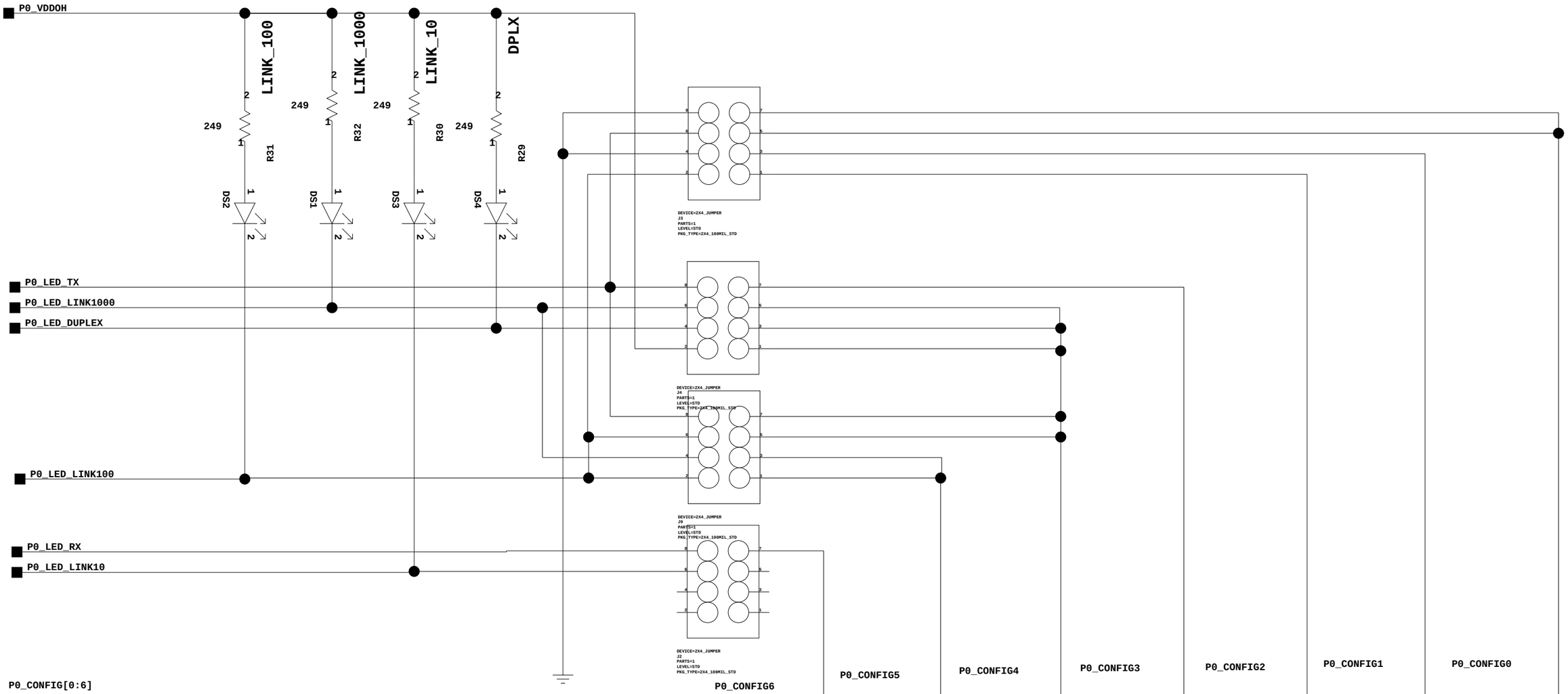
Double Footprint for SMD
and Half Size Metal Can



XILINX

Title:
Schematic, PHY Daughter PCB, 1280327
0381166

Date: 07/11/03	Ver: C
Sheet Size: B	Rev: 1.0
Sheet 6 of 11	Drawn By SEG



PHY_0 CONFIGURATION (RGMII_CU 1000T)

WARNING

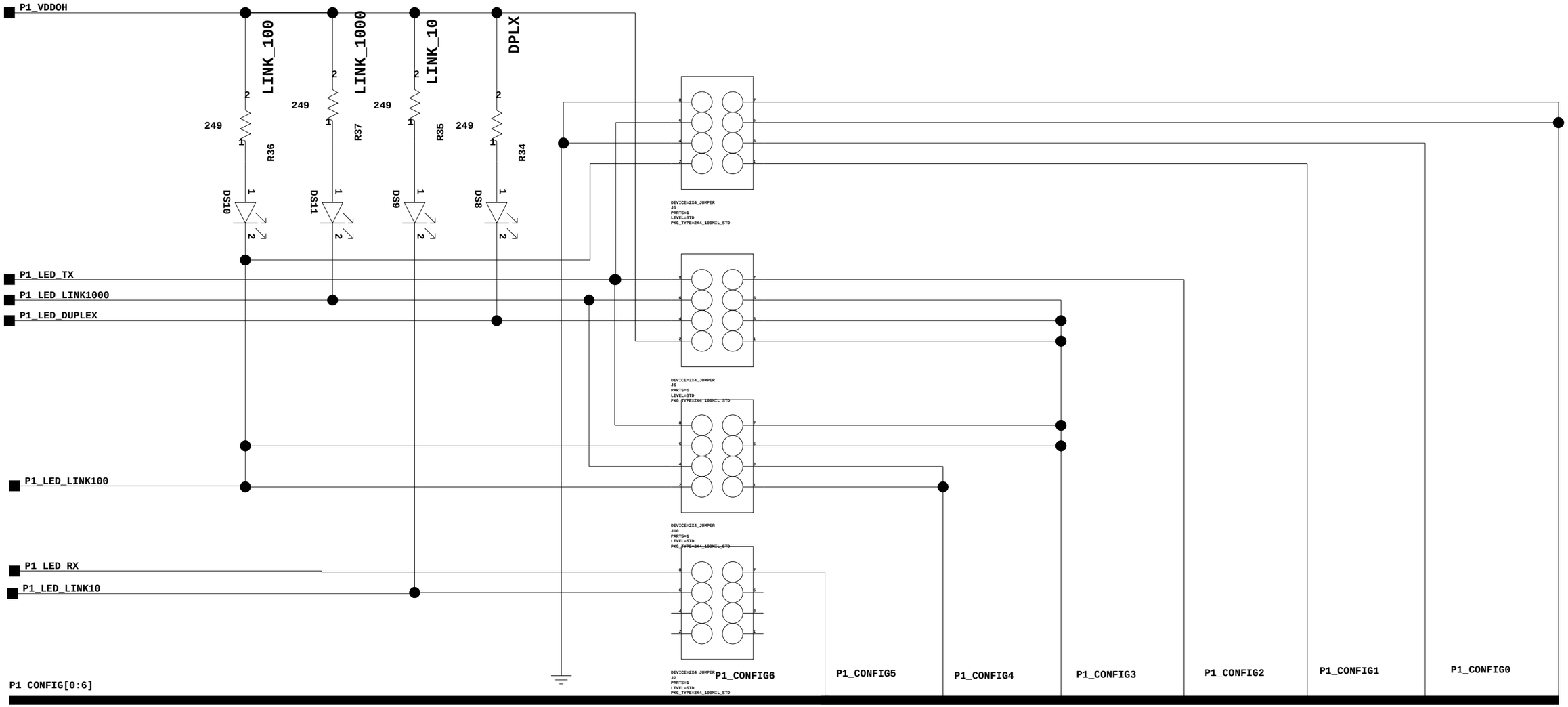
Make sure that only one jumper pair is active on each of these 7 configuration signals

CONFIG SIG	DEFAULT	FUNCTION	SIGNAL
CONFIG0	INSTALLED	PHYADR=0	VSS
CONFIG0		PHYADR=1	LED_TX
CONFIG1	INSTALLED		VSS
CONFIG2	INSTALLED	ANEG 1000M	LED_LINK100
CONFIG3	INSTALLED	ANEG_1000M	LED_TX
CONFIG4		SGMII_CU	LED_LINK1000
CONFIG4	INSTALLED	RGMII_CU	LED_DUPLEX
CONFIG4		GMII_CU	VDD
CONFIG4		RTBI_CU	LED_TX
CONFIG4		TBI_CU	LED_LINK100
CONFIG5		SG/TBI_CU	LED_LINK1000
CONFIG5	INSTALLED	GMII/RGMII	LED_LINK100
CONFIG6	INSTALLED	50 Ohm	LED_RX
SPARE			LED_LINK100

XILINX

Title:
Schematic, PHY Daughter PCB, 1280327
0381166

Date: 07/11/03	Ver: C
Sheet Size: B	Rev: 1.0
Sheet 7 of 11	Drawn By SEG



PHY_1 CONFIGURATION (SGMII_CU 1000T)

WARNING

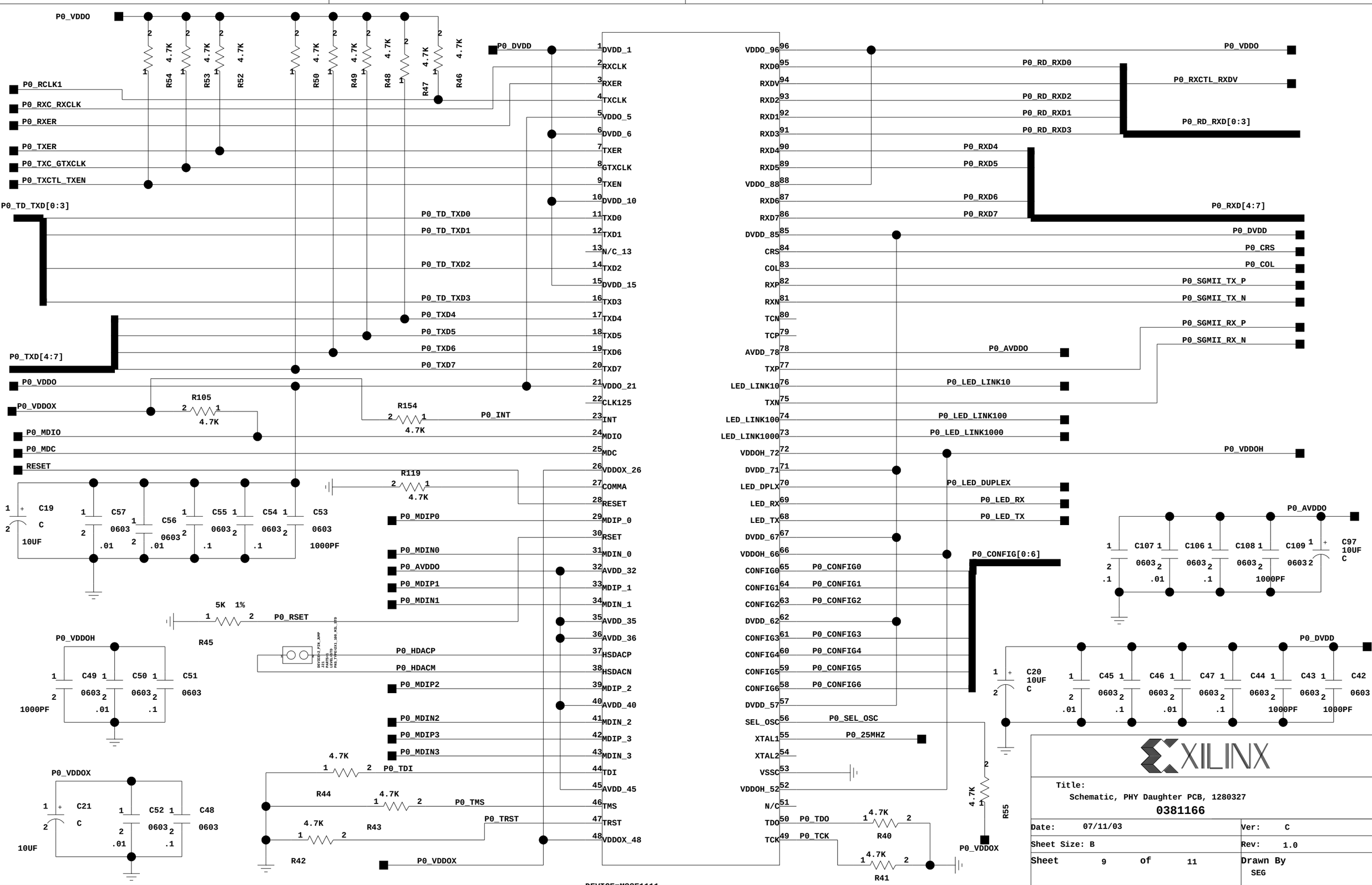
Make sure that only one jumper pair is active on each of these 7 configuration signals

CONFIG SIG	DEFAULT	FUNCTION	SIGNAL
CONFIG0	INSTALLED	PHYADR=0	VSS
CONFIG0		PHYADR=1	LED_TX
CONFIG1	INSTALLED		VSS
CONFIG2	INSTALLED	ANEG 1000M	LED_LINK100
CONFIG3	INSTALLED	ANEG_1000M	LED_TX
CONFIG4	INSTALLED	SGMII_CU	LED_LINK1000
CONFIG4		RGMII_CU	LED_DUPLEX
CONFIG4		GMII_CU	VDD
CONFIG4		RTBI_CU	LED_TX
CONFIG4		TBI_CU	LED_LINK100
CONFIG5	INSTALLED	SG/TBI_CU	LED_LINK1000
CONFIG5		GMII/RGMII	LED_LINK100
CONFIG6	INSTALLED	50 Ohm	LED_RX
SPARE			LED_LINK100

XILINX

Title:
Schematic, PHY Daughter PCB, 1280327
0381166

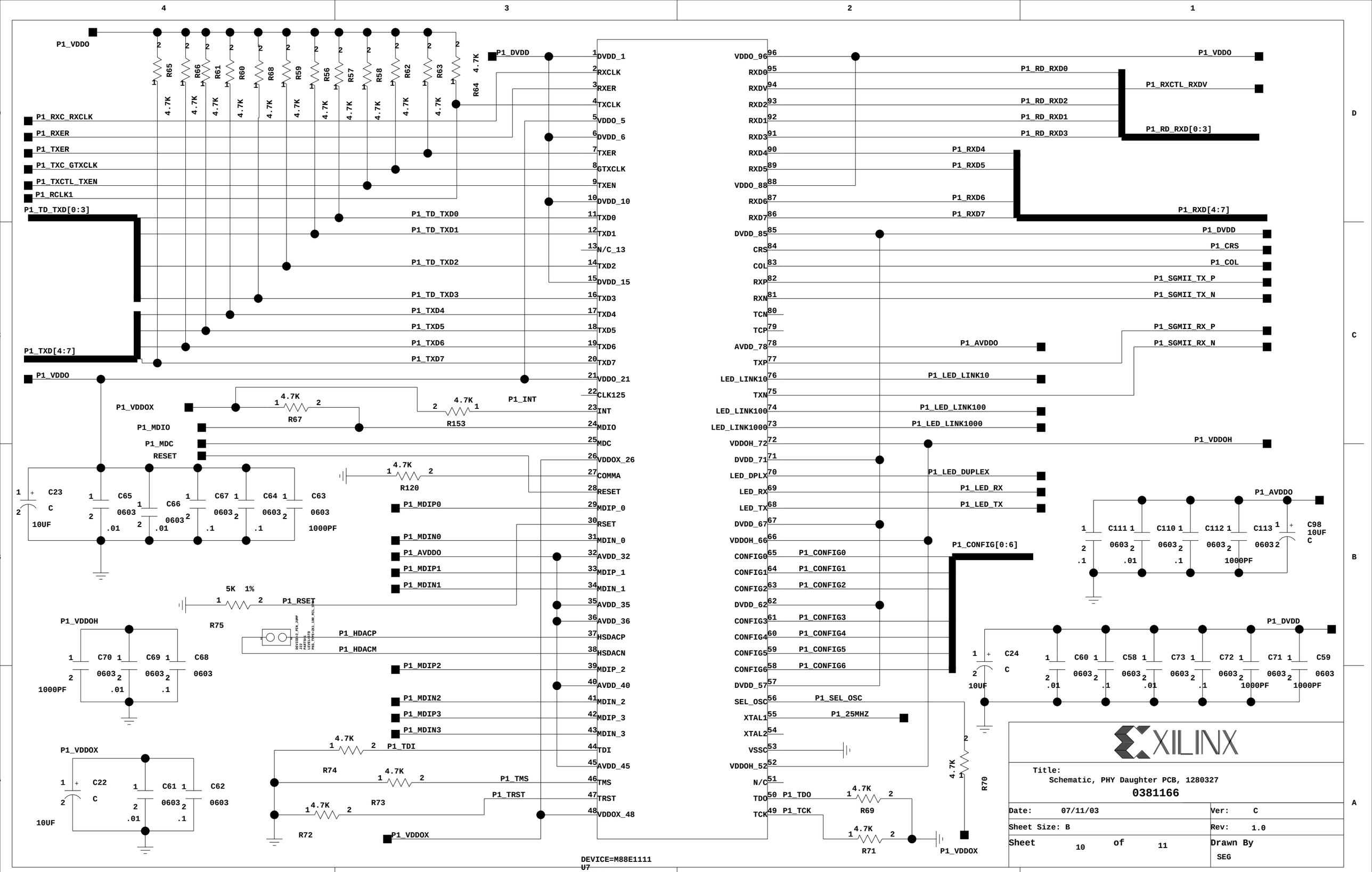
Date: 07/11/03	Ver: C
Sheet Size: B	Rev: 1.0
Sheet 8 of 11	Drawn By SEG

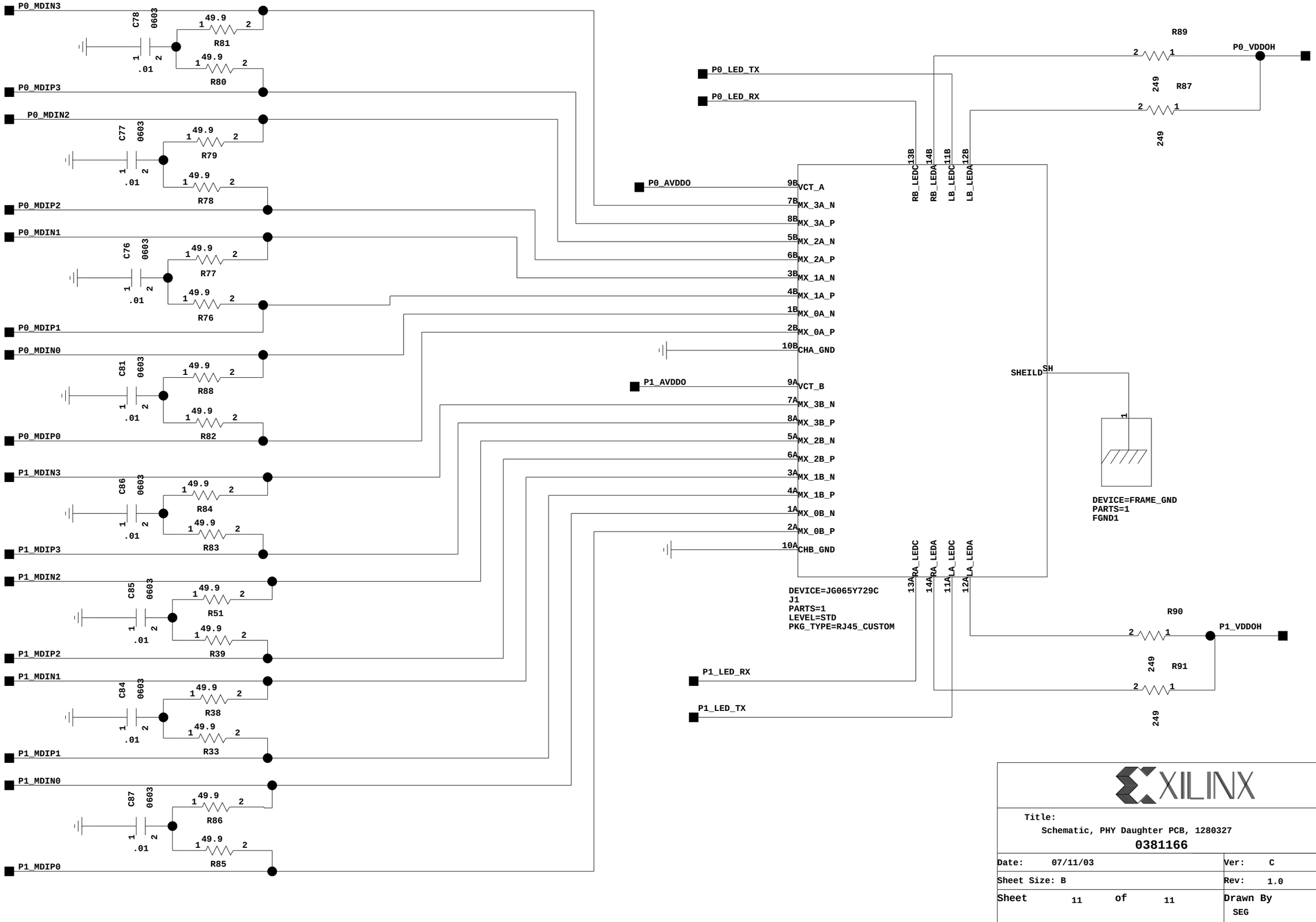


XILINX

Title:
Schematic, PHY Daughter PCB, 1280327
0381166

Date: 07/11/03	Ver: C
Sheet Size: B	Rev: 1.0
Sheet 9 of 11	Drawn By SEG


P1_VDDO
R65 4.7K
R66 4.7K
R61 4.7K
R60 4.7K
R68 4.7K
R59 4.7K
R56 4.7K
R57 4.7K
R58 4.7K
R62 4.7K
R63 4.7K
R64 4.7K
P1_DVDD
P1_RXC_RXCLK
P1_RXER
P1_TXER
P1_TXC_GTXCLK
P1_TXCTL_TXEN
P1_RCLK1
P1_TD_TXD[0:3]
P1_TXD[4:7]
P1_TD_TXD0
P1_TD_TXD1
P1_TD_TXD2
P1_TD_TXD3
P1_TXD4
P1_TXD5
P1_TXD6
P1_TXD7
P1_INT
1 DVDD_1
2 RXCLK
3 RXER
4 TXCLK
5 VDDO_5
6 DVDD_6
7 TXER
8 GTXCLK
9 TXEN
10 DVDD_10
11 TXD0
12 TXD1
13 N/C_13
14 TXD2
15 DVDD_15
16 TXD3
17 TXD4
18 TXD5
19 TXD6
20 TXD7
21 VDDO_21
22 CLK125
23 INT
24 MDIO
25 MDC
26 VDDOX_26
27 COMMA
28 RESET
29 MDIP_0
30 RSET
31 MDIN_0
32 AVDD_32
33 MDIP_1
34 MDIN_1
35 AVDD_35
36 AVDD_36
37 HSDACP
38 HSDACN
39 MDIP_2
40 AVDD_40
41 MDIN_2
42 MDIP_3
43 MDIN_3
44 TDI
45 AVDD_45
46 TMS
47 TRST
48 VDDOX_48
P1_VDDOX
P1_MDIO
P1_MDC
RESET
R67 4.7K
R153 4.7K
C23 C 10UF
C65 0603 .01
C66 0603 .01
C67 0603 .1
C64 0603 .1
C63 0603 1000PF
R120 4.7K
P1_MDIP0
P1_MDIN0
P1_AVDDO
P1_MDIP1
P1_MDIN1
5K 1%
P1_RSET
R75
P1_VDDOH
P1_HDACP
P1_HDACM
C70 0603 1000PF
C69 0603 .01
C68 0603 .1
P1_MDIP2
P1_MDIN2
P1_MDIP3
P1_MDIN3
P1_TDI
R74 4.7K
P1_TMS
R73 4.7K
P1_TRST
R72 4.7K
P1_VDDOX
C22 C 10UF
C61 0603 .01
C62 0603 .1
DEVICE=M88E1111
U7
PARTS=1
LEVEL=STD
VDDO_96 96
RXD0 95
RXDV 94
RXD2 93
RXD1 92
RXD3 91
RXD4 90
RXD5 89
VDDO_88 88
RXD6 87
RXD7 86
DVDD_85 85
CRS 84
COL 83
RXP 82
RXN 81
TCN 80
TCP 79
AVDD_78 78
TXP 77
LED_LINK10 76
TXN 75
LED_LINK100 74
LED_LINK1000 73
VDDOH_72 72
DVDD_71 71
LED_DPLX 70
LED_RX 69
LED_TX 68
DVDD_67 67
VDDOH_66 66
CONFIG0 65
CONFIG1 64
CONFIG2 63
DVDD_62 62
CONFIG3 61
CONFIG4 60
CONFIG5 59
CONFIG6 58
DVDD_57 57
SEL_OSC 56
XTAL1 55
XTAL2 54
VSSC 53
VDDOH_52 52
N/C 51
TDO 50
TCK 49
P1_RD_RXD0
P1_RD_RXD2
P1_RD_RXD1
P1_RD_RXD3
P1_RXD4
P1_RXD5
P1_RXD6
P1_RXD7
P1_AVDDO
P1_LED_LINK10
P1_LED_LINK100
P1_LED_LINK1000
P1_LED_DUPLEX
P1_LED_RX
P1_LED_TX
P1_CONFIG0
P1_CONFIG1
P1_CONFIG2
P1_CONFIG3
P1_CONFIG4
P1_CONFIG5
P1_CONFIG6
P1_SEL_OSC
P1_25MHZ
R69 4.7K
R71 4.7K
R70 4.7K
P1_VDDOX
P1_VDDO
P1_RXCTL_RXDV
P1_RD_RXD[0:3]
P1_RXD[4:7]
P1_DVDD
P1_CRS
P1_COL
P1_SGMII_TX_P
P1_SGMII_TX_N
P1_SGMII_RX_P
P1_SGMII_RX_N
P1_VDDOH
P1_CONFIG[0:6]
P1_AVDDO
C111 0603 .1
C110 0603 .01
C112 0603 .1
C113 0603 1000PF
C98 10UF
P1_DVDD
C24 C 10UF
C60 0603 .01
C58 0603 .1
C73 0603 .01
C72 0603 .1
C71 0603 1000PF
C59 0603 1000PF
XILINX
Title:
Schematic, PHY Daughter PCB, 1280327
0381166
Date: 07/11/03
Ver: C
Sheet Size: B
Rev: 1.0
Sheet 10 of 11
Drawn By
SEG



XILINX

Title:
Schematic, PHY Daughter PCB, 1280327
0381166

Date: 07/11/03	Ver: C
Sheet Size: B	Rev: 1.0
Sheet 11 of 11	Drawn By SEG