Virtex-4 LX/SX Prototype Platform

User Guide

UG078 (v1.2) May 24, 2006

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/30/04	1.0	Initial Xilinx release.
10/20/04	1.0.1	Minor corrections to text and figures.
06/09/05	1.0.2	Modified title from *Virtex-4 Prototype Platform* to *Virtex-4 LX/SX Prototype Platform.* Updated figure titles and Table 8, Table 9, and Table 10.
06/27/05	1.0.3	Corrected clock names in Table 6 (pin W9) and Table 7 (pins H17, AJ17, and AK19).
05/05/06	1.1	Corrected title of Table 7.
05/24/06	1.2	Updated title of Table 5 and Table 7. Added revision number to P/N on title page.

Table of Contents

About This Guide

This user guide describes the features and operation of the Virtex™-4 prototype platform and describes how to configure chains of FPGAs and serial PROMs.

Guide Contents

This manual contains one chapter:

- "Virtex-4 LX/SX Prototype Platform"

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/literature/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *`design_name`*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**

Convention	Meaning or Use	Example
Italic font	Variables in a syntax statement for which you must supply values	**ngdbuild** *design_name*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **bus[7:0]**, they are required.	**ngdbuild** [*option_name*] *design_name*
Braces { }	A list of items from which you must choose one or more	**lowpwr =**{**on**|**off**}
Vertical bar |	Separates items in a list of choices	**lowpwr =**{**on**|**off**}
Vertical ellipsis . . .	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN' . . .
Horizontal ellipsis ...	Repetitive material that has been omitted	**allow block** *block_name loc1 loc2 ... locn;*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Handbook.*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Virtex-4 LX/SX Prototype Platform

Package Contents

- Xilinx Virtex™-4 prototype platform board
- User guide
- Device vacuum tool
- Headers for test points
- CD-ROM
- One low-voltage, 14-pin, dual-inline package (DIP) crystal oscillator

CD-ROM Contents

- User guide in PDF format
- Example designs
  - These designs include the Verilog source code, user constraints files (*.ucf), documentation in PDF, and a readme.txt file
- Bitstream files (*.bit) for each part type supported by the board (Bitstream synthesized using Xilinx tools)
- Full schematics of the board in both PDF format and ViewDraw schematic format
- PC board layout in Pads PCB format
- Gerber files in *.pho and *.pdf for the PC board (There are many free or shareware Gerber file viewers available on the Web for viewing and printing these files)

Introduction

The Virtex-4 prototype platform and demonstration boards allow designers to investigate and experiment with the features of Virtex-4 series FPGAs. This user guide describes the features and operation of the Virtex-4 prototype platform, including how to configure chains of FPGAs and serial PROMs.

Note: Prototype platforms are intended strictly for evaluating the functionality of Virtex-4 features and are not intended for A/C characterization or high-speed I/O evaluation.

Features

- Independent power supply jacks for VCCINT, VCCO, and VCCAUX
- Selectable VCCO-enable pins for each SelectIO™ bank
- Configuration port for use with Parallel Cable III and Parallel Cable IV cables
- 32 clock inputs
  - 4 differential clock pairs
  - 4 LVTTL-type oscillator sockets
  - 20 breakout clock pins
- Power indicator LEDs
- Onboard Platform Flash ISPROM (32 Mb) for configuration
- Onboard power supplies for the Platform Flash ISPROM
- JTAG port for reprogramming the XCF32P series reconfigurable ISPROM and the user FPGA, also known as the *device under test* (DUT)
- Upstream and downstream System ACE™ connectors and configuration interface connectors
- Onboard battery holder
- One low-voltage, 14-pin, DIP crystal oscillators

The kit contains headers that can be soldered to the breakout area, if desired. These headers are useful with certain types of oscilloscope probes for either connecting function generators or wiring pins to the prototype area.

The Virtex-4 prototype platform (the board) contains a DUT FPGA and one In-System Programmable Configuration PROM (ISPROM). The ISPROM can hold up to 33,554,432 bits. The DUT can be configured either from the ISPROM or from the configuration ports (Parallel Cable III/IV cable).

In addition to the ISPROM and the configuration ports, there are upstream connectors and downstream connectors. The upstream connectors can be connected to configure the DUT by using the System ACE configuration solution or by chaining another board. The downstream connectors can be used to connect to another board in a chain for serial configuration. A maximum of two boards can be chained together.

Figure 1 shows a block diagram of the board.

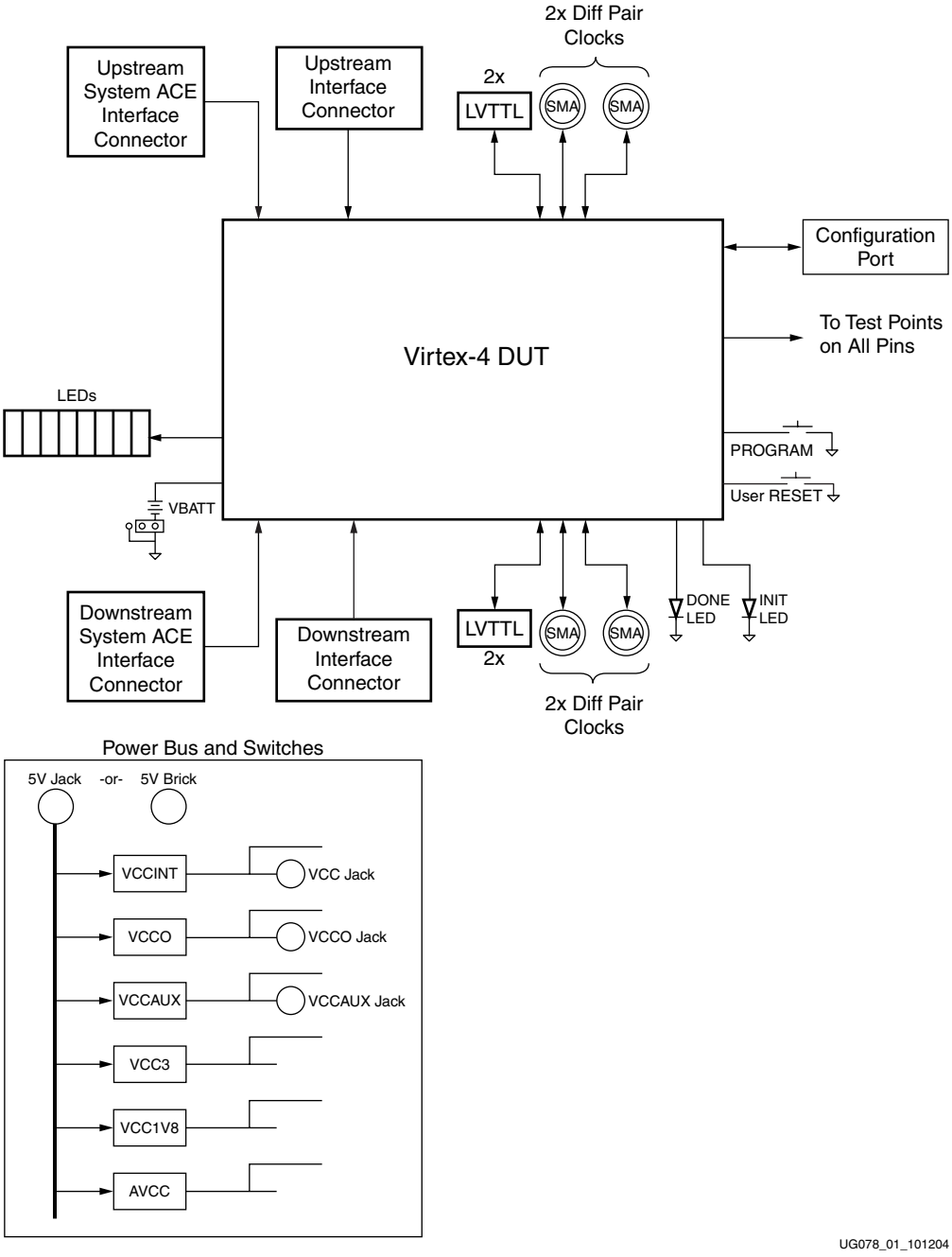

Figure 1: **Virtex-4 LX/SX Prototype Platform Block Diagram**

Detailed Description

The Virtex-4 prototype platform board is shown in Figure 2. Each feature is detailed in the numbered sections that follow.

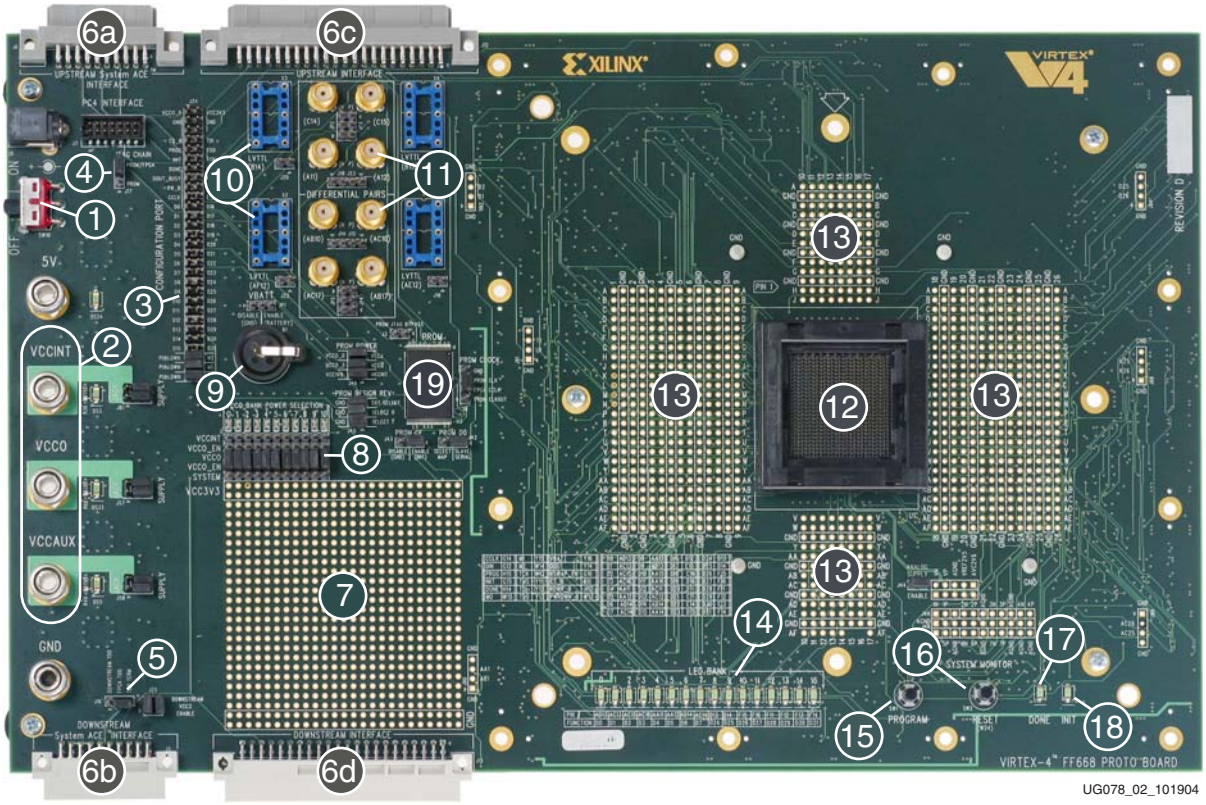

Figure 2: **Detailed Description of Virtex-4 LX/SX Prototype Platform Components**

1. Power Switch

The board has an onboard power supply and an ON | OFF power switch. When lit, a green LED indicates power from the power brick connector or the 5V jack.

On Position

In the ON position, the power switch enables delivery of all power to the board by way of voltage regulators situated on the backside of the board. These regulators feed off a 5V external power brick or the 5V power supply jack.

The voltage regulators deliver fixed voltages. Maximum current range for each supply will vary. Table 1, page 9 shows the maximum voltage and maximum current for each onboard power supply. If the current exceeds maximum ratings, use the power jacks to supply power to the DUT.

Table 1: **Voltage Ranges**

Label	Maximum Voltage	Maximum Current
VCCINT	1.2V	1A
VCCO	3.3V	2A
VCCAUX	2.5V	1.5A
VCC	3.3V	2A
VCC1V8	1.8V	1A
AVCC	2.5V	25 mA

Off Position

In the OFF position, the power switch disables all modes of powering the DUT.

Power Enable Jumpers

For each power supply there are headers marked SUPPLY on one side and JACK on the other side. Appropriate placements of jumpers on these headers enables delivery of all power from either the onboard regulators or the three power supply jacks marked VCCINT, VCCO, and VCCAUX.

2. Power Supply Jacks

One method of delivering power to the DUT is by way of the power supply jacks. (Consult the Xilinx data book, http://www.xilinx.com/partinfo/datasheet.htm, for the maximum voltage rating for each device you are using.) The power supply jacks are:

- VCCINT
  - Supplies voltage to the V_{CCINT} of the DUT
- VCCO
  - Supplies I/O voltages to the DUT
  - Each bank can be powered from one of two sources (V_{CCO}, V_{CCINT}) by appropriate placement of jumpers on the header
- VCCAUX
  - Supplies voltage to the V_{CCAUX} DUT pins

3. Configuration Ports

These headers can be used to connect a Parallel Cable III or Parallel Cable IV cable to the board (see Table 2) and support all Virtex-4 device configuration modes. See Table 3 for connecting the cables to the configuration ports and Figure 3 for setting up the JTAG chain on the board.

Table 2: **Serial Mode**

Configuration Port Header	Parallel Cable III/IV Pins
VCC3	VCC
GND	GND
CCLK	CCLK
DONE	D/P
DIN	DIN
PROG	PROG
INIT	

Table 3: **JTAG Mode**

Configuration Port Header Parallel Cable IV Connector	Parallel Cable III Pins	Parallel Cable IV Pins
VCC3V3	VCC	VCC
GND	GND	GND
TMS	TMS	TMS
TDI	TDI	TDI
TDO	TDO	TDO
TCK	TCK	TCK
INIT		INIT

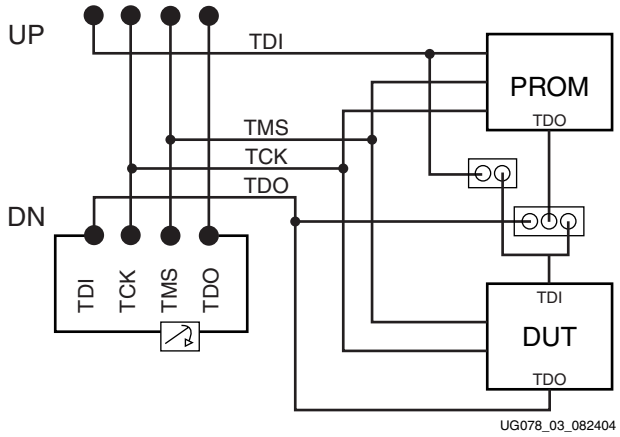

Figure 3: **JTAG Chain Termination**

4. JTAG Chain

Jumper J17 provides the ability to have the Virtex-4 in the JTAG chain or remove it from the JTAG chain.

Note: The Virtex-4 device must *not* be in the socket when detecting the ISPROM in the chain.

5. JTAG Termination Jumper

The DUT TDO pin can be jumpered to the TDO TERM pin or the downstream TDO pin. When another board is connected to the downstream System ACE connector or downstream interface connector, jumper the DUT TDO pin to the downstream TDO pin for serial chaining. The connection allows the DUT TDO pin to be connected to the next device in the chain.

The TCK and TMS pins are parallel feedthrough connections from the upstream System ACE interface connector to the downstream System ACE interface connector and drive the TCK and TMS pins of the onboard PROM and the DUT.

Note: The termination jumper must be in place on the last board in the chain to connect the TDO pin of the final device to the TDO feedback chain.

6a. Upstream System ACE Interface Connector

The upstream System ACE interface connector, as shown in Figure 4, can be used to configure the DUT. Any JTAG configuration stream can source this connector. For example, a System ACE controller with a CompactFlash card can be used to generate very large JTAG streams for configuring multiple Virtex-4 prototype platforms using the downstream System ACE interface connector.

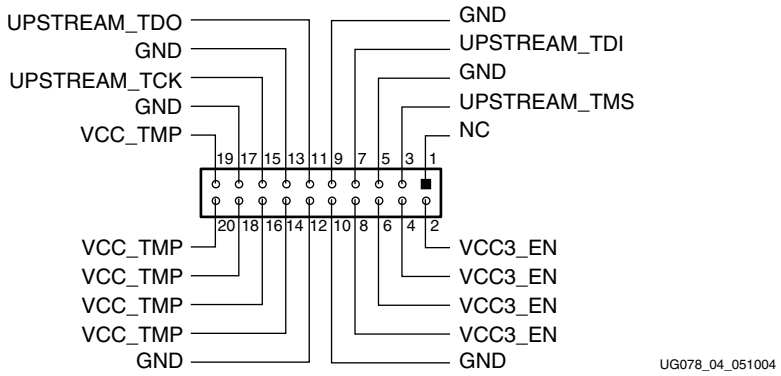

Figure 4: **Upstream System ACE Interface Connector (20-Pin Female)**

6b. Downstream System ACE Interface Connector

The downstream System ACE interface connector, as shown in Figure 5, is used to pass configuration information to a DUT in a downstream prototype platform board from sources such as a Parallel Cable III cable or an upstream System ACE interface connector.

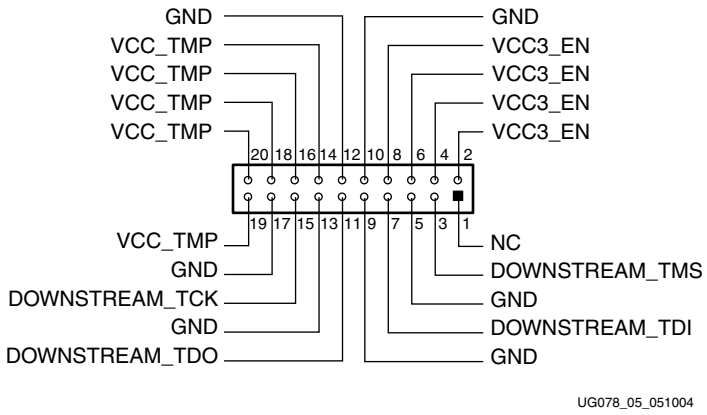

Figure 5: **Downstream System ACE Interface Connector (20-Pin Male)**

6c. Upstream Interface Connector

The upstream interface connector, as shown in Figure 6, is used to configure the DUT in select map or slave-serial mode. This connector can be sourced by a downstream interface connector of another prototype platform board.

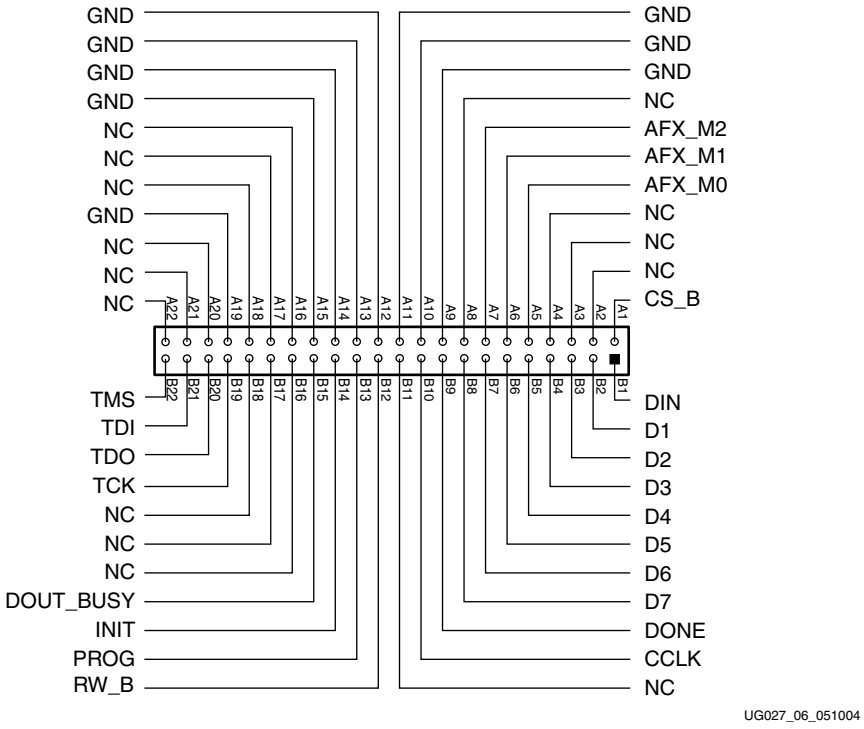

Figure 6: **Upstream Interface Connector (44-Pin Female)**

6d. Downstream Interface Connector

The downstream interface connector, as shown in Figure 7, passes serial configuration information to the DUT in the downstream prototype platform board.

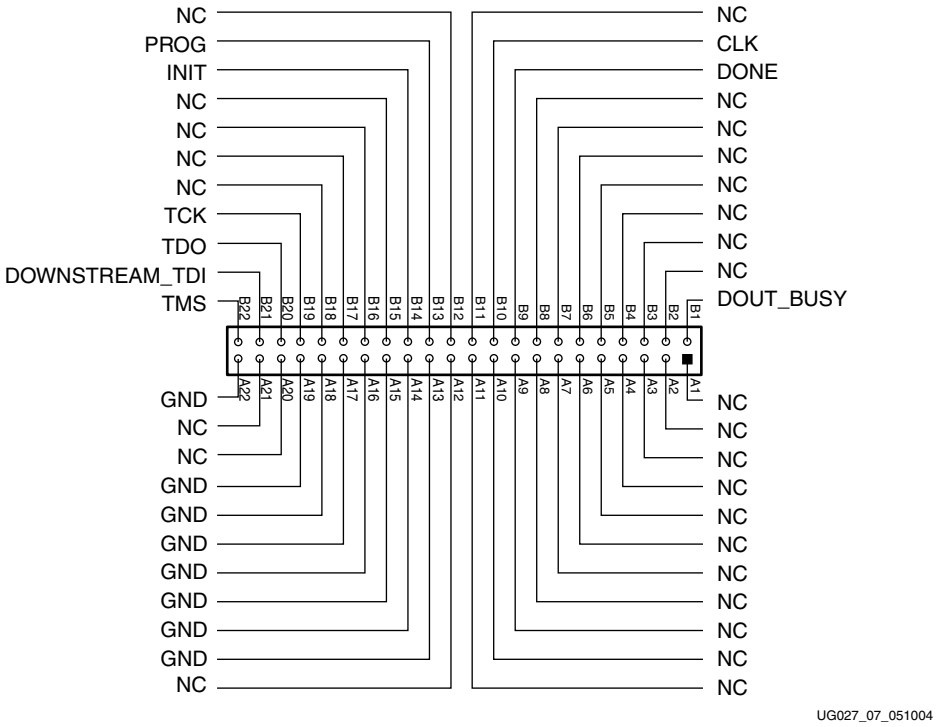

Figure 7: **Downstream Interface Connector (44-Pin Male)**

7. Prototyping Area

The prototyping area accommodates 0.10-inch spaced ICs. The kit contains headers that can be soldered to the breakout area, if desired. Power and ground buses are located at the top and bottom edges, respectively, of the prototyping area.

8. VCCO-Enable Supply Jumpers

Virtex-4 series devices have 9 to 17 SelectIO banks, labeled 0 through 16, each with a VCCO-enable supply jumper. The VCCO-enable supply jumpers can connect each bank to one of the two onboard supplies, VCCINT or the VCCO supply. These jumpers must be installed for the Virtex-4 device to function normally.

9. VBATT

An onboard battery holder is connected to the VBATT pin of the DUT. If an external power supply is used, the associated jumper must be removed and instead use a 12 mm lithium coin battery (3V).

10. Oscillator Sockets

The board has four crystal oscillator sockets, all wired for standard LVTTL-type oscillators. These sockets connect to the DUT clock pads as shown in Table 4 and Table 5. Onboard termination resistors can be changed by the user. The oscillator sockets accept both half- and full-sized oscillators and are powered by the DUT VCCO power supply.

Table 4: **Oscillator Socket Clock Pin Connections for SF363 and FF668**

Label	SF363		FF668	
	Clock Name	Pin Number	Clock Name	Pin Number
OSC Socket Top 1	IO_L1N_GCLK_CC_LC_3	A11	IO_L1N_GCLK_CC_LC_3	B14
OSC Socket Top 2	IO_L1P_GCLK_CC_LC_3	B12	IO_L1P_GCLK_CC_LC_3	B15
OSC Socket Bottom 1	IO_L1P_GCLK_CC_LC_4	W13	IO_L1P_GCLK_CC_LC_4	AF12
OSC Socket Bottom 2	IO_L1N_GCLK_CC_LC_4	W12	IO_L1N_GCLK_CC_LC_4	AE12

Table 5: **Oscillator Socket Clock Pin Connections for FF1148 and FF1513**

Label	FF1148		FF1513	
	Clock Name	Pin Number	Clock Name	Pin Number
OSC Socket Top 1	IO_L1N_GCLK_CC_LC_3	G18	IO_L1N_GCLK_CC_LC_3	N20
OSC Socket Top 2	IO_L1P_GCLK_CC_LC_3	F18	IO_L1P_GCLK_CC_LC_3	P20
OSC Socket Bottom 1	IO_L1P_GCLK_CC_LC_4	AF18	IO_L1P_GCLK_CC_LC_4	AH20
OSC Socket Bottom 2	IO_L1N_GCLK_CC_LC_4	AE18	IO_L1N_GCLK_CC_LC_4	AH19

11. Differential Clock Inputs

In addition to the oscillator sockets, there are eight 50Ω SMA connectors that allow connection to an external function generator. These connect to the DUT clock pads as shown in Table 6 and Table 7. They can also be used as differential clock inputs. The differential clock pairings (DIFFERENTIAL PAIRS) are as shown in the tables.

Table 6: **SMA Clock Pin Connections for SF363 and FF668**

Label	SF363		FF668	
	Clock Name	Pin Number	Clock Name	Pin Number
N	IO_L8N_GC_LC_3	B7	IO_L8N_GC_LC_3	C12
P	IO_L8P_GC_LC_3	A7	IO_L8P_GC_LC_3	C13
N	IO_L2N_GC_VRP_LC_3	B9	IO_L2N_GC_VRP_LC_3	A11
P	IO_L2P_GC_VRN_LC_3	A10	IO_L2P_GC_VRN_LC_3	A12
N	IO_L2N_GC_LC_4	W5	IO_L2N_GC_LC_4	AB10
P	IO_L2P_GC_LC_4	Y5	IO_L2P_GC_LC_4	AC10
N	IO_L8N_GC_CC_LC_4	W8	IO_L8N_GC_CC_LC_4	AD11
P	IO_L8P_GC_CC_LC_4	W9	IO_L8P_GC_CC_LC_4	AD12

Table 7: **SMA Clock Pin Connections for FF1148 and FF1513**

Label	FF1148		FF1513	
	Clock Name	Pin Number	Clock Name	Pin Number
N	IO_L8N_GC_CC_LC_3	G16	IO_L8N_GC_CC_LC_3	K21
P	IO_L8P_GC_CC_LC_3	G17	IO_L8P_GC_CC_LC_3	L21
N	IO_L2N_GC_VRP_LC_3	J17	IO_L2N_GC_VRP_LC_3	K19
P	IO_L2P_GC_VRP_LC_3	H17	IO_L2P_GC_VRP_LC_3	J19
N	IO_L2N_GC_LC_4	AF16	IO_L2N_GC_LC_4	AF18
P	IO_L2P_GC_LC_4	AG16	IO_L2P_GC_LC_4	AF19
N	IO_L8N_GC_CC_LC_4	AH17	IO_L8N_GC_CC_LC_4	AJ19
P	IO_L8P_GC_CC_LC_4	AJ17	IO_L8P_GC_CC_LC_4	AK19

12. DUT Socket

The DUT socket contains the user FPGA, referred to as the *device under test* (DUT). The DUT must be oriented using the P1 indicator on the board.

> ***Caution!*** Failure to insert the device to the proper orientation can damage the device. To avoid pin damage, always use the vacuum tool provided when inserting or removing the Virtex-4 device. When using BGA packages, do not apply pressure to the device while activating the socket. Doing so can damage the socket and/or the device.

13. Pin Breakout

The pin breakout area is used to monitor or apply signals to each of the DUT pins. Headers can be soldered to the breakout area to use with certain types of oscilloscope probes, for either connecting function generators or wiring pins to the pin breakout area. Clocks in the pin breakout area that connect to the DUT clock pads are shown in Table 8 and Table 9, page 20.

Table 8: **Breakout Clock Pin Connections for SF363 and FF668**

Label	SF363		FF668	
	Clock Name	Pin Number	Clock Name	Pin Number
Breakout Area	IO_L4P_GC_LC_3	B10	IO_L4P_GC_LC_3	B13
	IO_L4N_GC_VREF_LC_3	C10	IO_L4N_GC_VREF_LC_3	B12
	IO_L5P_GC_LC_3	B13	IO_L5P_GC_LC_3	A16
	IO_L5N_GC_LC_3	A13	IO_L5N_GC_LC_3	A15
	IO_L6P_GC_LC_3	A8	IO_L6P_GC_LC_3	A10
	IO_L6N_GC_LC_3	B8	IO_L6N_GC_LC_3	B10
	IO_L7P_GC_LC_3	B14	IO_L7P_GC_LC_3	B17
	IO_L7N_GC_LC_3	A14	IO_L7N_GC_LC_3	A17
	IO_L3P_GC_LC_3	C11	IO_L3P_GC_LC_3	C14
	IO_L3N_GC_LC_3	B11	IO_L3N_GC_LC_3	C15
	IO_L4P_GC_LC_4	Y6	IO_L4P_GC_LC_4	AF11
	IO_L4N_GC_VREF_LC_4	W6	IO_L4N_GC_VREF_LC_4	AF10
	IO_L5P_GC_LC_4	W11	IO_L5P_GC_LC_4	AE14
	IO_L5N_GC_LC_4	W10	IO_L5N_GC_LC_4	AE13
	IO_L6P_GC_LC_4	Y7	IO_L6P_GC_LC_4	AE10
	IO_L6N_GC_LC_4	W7	IO_L6N_GC_LC_4	AD10
	IO_L7P_GC_VRN_LC_4	Y10	IO_L7P_GC_VRN_LC_4	AD17
	IO_L7N_GC_VRP_LC_4	Y9	IO_L7N_GC_VRP_LC_4	AD16
	IO_L3P_GC_CC_LC_4	Y12	IO_L3P_GC_CC_LC_4	AB17
	IO_L3N_GC_CC_LC_4	Y11	IO_L3N_GC_CC_LC_4	AC17

Table 9: **Breakout Clock Pin Connections for FF1148 and FF1513**

Label	FF1148		FF1513	
	Clock Name	Pin Number	Clock Name	Pin Number
Breakout Area	IO_L4P_GC_LC_3	E13	IO_L4P_GC_LC_3	J21
	IO_L4N_GC_VREF_LC_3	E17	IO_L4N_GC_VREF_LC_3	J20
	IO_L5P_GC_LC_3	K18	IO_L5P_GC_LC_3	M21
	IO_L5N_GC_LC_3	K17	IO_L5N_GC_LC_3	M20
	IO_L6P_GC_LC_3	E16	IO_L6P_GC_LC_3	L20
	IO_L6N_GC_LC_3	F16	IO_L6N_GC_LC_3	L19
	IO_L7P_GC_LC_3	K19	IO_L7P_GC_LC_3	P22
	IO_L7N_GC_LC_3	J19	IO_L7N_GC_LC_3	P21
	IO_L3P_GC_LC_3	H19	IO_L3P_GC_LC_3	N22
	IO_L3N_GC_LC_3	H18	IO_L3N_GC_LC_3	M22
	IO_L4P_GC_LC_4	AK18	IO_L4P_GC_LC_4	AG20
	IO_L4N_GC_VREF_LC_4	AK17	IO_L4N_GC_VREF_LC_4	AF20
	IO_L5P_GC_LC_4	AG18	IO_L5P_GC_LC_4	AL20
	IO_L5N_GC_LC_4	AG17	IO_L5N_GC_LC_4	AL19
	IO_L6P_GC_LC_4	AE17	IO_L6P_GC_LC_4	AH18
	IO_L6N_GC_LC_4	AE16	IO_L6N_GC_LC_4	AG18
	IO_L7P_GC_VRN_LC_4	AJ19	IO_L7P_GC_VRN_LC_4	AL21
	IO_L7N_GC_VRP_LC_4	AK19	IO_L7N_GC_VRP_LC_4	AK21
	IO_L3P_GC_CC_LC_4	AH19	IO_L3P_GC_CC_LC_4	AJ21
	IO_L3N_GC_CC_LC_4	AH18	IO_L3N_GC_CC_LC_4	AJ20

14. User LEDs (Active-High)

There are 16 active-high user LEDs on the board. Before configuration, the LEDs reflect the status of the configuration mode pins. During configuration, the LEDs are in a high-impedance condition. After configuration, the LEDs are available to the user and reflect the status of pins D0-D7 and D24-D31 (corresponding to LED 0- LED 15). The LED assignments are shown in Table 10.

Table 10: **LED Assignments and Corresponding I/O**

LED	After Configuration	Pin Number For Package Type			
		SF363	FF668	FF1148	FF1513
0	Available as user LEDs	U9	AD13	G13	B16
1		V10	AC13	F13	A16
2		V11	AC15	J21	R22
3		U12	AC16	H22	T23
4		V8	AA11	H13	G15
5		V9	AA12	H14	G16
6		V12	AD14	M20	N24
7		V13	AC14	N20	M25
8		D6	D13	K14	H15
9		E7	D14	J14	J16
10		E14	F15	D21	D26
11		D15	F16	E21	E26
12		F6	F11	L14	L16
13		E6	F12	L15	K16
14		E15	F13	N18	F25
15		F15	F14	N19	F26

15. PROGRAM Switch

The active-low PROGRAM switch, when pressed, grounds the program pin on the DUT.

16. RESET Switch (Active-Low)

The RESET switch connects to a standard I/O pin on the DUT, allowing the user, after configuration, to reset the logic within the DUT. When pressed, this switch grounds the pin.

Table 11 shows the INIT pin locations for the available DUT package types.

Table 11: **User Hardware and Corresponding I/O Pins**

Label	Pin Number For Package Type			
	SF363	FF668	FF1148	FF1513
RESET	R16	W24	AP21	AH23

Note: Refer to the readme.txt file for implementation of this user pin.

17. DONE LED

The DONE LED indicates the status of the DONE pin on the DUT. This LED lights when DONE is high or if power is applied to the board without a part in the socket.

18. INIT LED

The INIT LED lights during initialization.

19. Platform Flash ISPROM

A 32-Mb Platform Flash In-System Programmable Configuration PROM (ISPROM) is provided on the board for configuration (see Table 12). Refer to *Platform Flash ISPROM* (DS123) at http://direct.xilinx.com/bvdocs/publications/ds123.pdf for a detailed description.

Table 12: **Platform Flash ISPROM Configuration**

Label	Description
J46	Provides power to the ISPROM. These jumpers must be installed for proper operation of the ISPROM.
J45	Sets the design revision control for the ISPROM.
J43	Enables or disables the ISPROM by placing the address counter in reset and DATA output lines in high-impedance state.
J42	Sets the ISPROM for serial or select map configuration.
J8	Selects one of two modes of CCLK operation: • ISPROM provides CCLK (PROM CLKOUT) • FPGA provides CCLK (FPGA CCLK)