

ML605 Reference Design User Guide

UG535 (v1.0) September 25, 2009



Xilinx is disclosing this user guide, manual, release note, and/or specification (the "Documentation") to you solely for use in the development of designs to operate with Xilinx hardware devices. You may not reproduce, distribute, republish, download, display, post, or transmit the Documentation in any form or by any means including, but not limited to, electronic, mechanical, photocopying, recording, or otherwise, without the prior written consent of Xilinx. Xilinx expressly disclaims any liability arising out of your use of the Documentation. Xilinx reserves the right, at its sole discretion, to change the Documentation without notice at any time. Xilinx assumes no obligation to correct any errors contained in the Documentation, or to advise you of any corrections or updates. Xilinx expressly disclaims any liability in connection with technical support or assistance that may be provided to you in connection with the Information.

THE DOCUMENTATION IS DISCLOSED TO YOU "AS-IS" WITH NO WARRANTY OF ANY KIND. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE DOCUMENTATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NONINFRINGEMENT OF THIRD-PARTY RIGHTS. IN NO EVENT WILL XILINX BE LIABLE FOR ANY CONSEQUENTIAL, INDIRECT, EXEMPLARY, SPECIAL, OR INCIDENTAL DAMAGES, INCLUDING ANY LOSS OF DATA OR LOST PROFITS, ARISING FROM YOUR USE OF THE DOCUMENTATION.

© 2009 Xilinx, Inc. XILINX, the Xilinx logo, Virtex, Spartan, ISE, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. PCI, PCI Express, PCIe, and PCI-X are trademarks of PCI-SIG. All other trademarks are the property of their respective owners.

Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|------------|---------|-------------------------|
| 09/25/2009 | 1.0 | Initial Xilinx release. |

Table of Contents

Preface: About This Guide

| | |
|------------------------------------|---|
| Additional Documentation | 5 |
| Additional Support Resources | 6 |

Chapter 1: ML605 Evaluation Board

| | |
|--|----|
| Introduction | 7 |
| ML605 Features | 8 |
| Reference Designs | 9 |
| Built-In Self Test (BIST) | 9 |
| Memory Interface Generator (MIG) DDR3 Design | 10 |
| Integrated Block for PCI Express | 12 |
| MultiBoot Design | 13 |
| ChipScope Pro IBERT Design | 14 |
| System Monitor | 15 |
| Stand-Alone Applications | 16 |
| Restoring Flash Contents | 17 |

Appendix A: References

About This Guide

This user guide introduces several designs that demonstrate Virtex®-6 FPGA features using the ML605 evaluation board. The provided designs include processing systems based on the MultiBoot and the Xilinx Memory Interface Generator for the Spartan-6 FPGA.

Additional Documentation

The following documents are also available for download at <http://www.xilinx.com/support/documentation/virtex-6.htm>.

- **Virtex-6 Family Overview**
The features and product selection of the Virtex-6 family are outlined in this overview.
- **Virtex-6 FPGA Data Sheet: DC and Switching Characteristics**
This data sheet contains the DC and Switching Characteristic specifications for the Virtex-6 family.
- **Virtex-6 FPGA Packaging and Pinout Specifications**
This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.
- **Virtex-6 FPGA Configuration Guide**
This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, boundary-scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.
- **Virtex-6 FPGA Clocking Resources User Guide**
This guide describes the clocking resources available in all Virtex-6 devices, including the MMCM and PLLs.
- **Virtex-6 FPGA Memory Resources User Guide**
The functionality of the block RAM and FIFO are described in this user guide.
- **Virtex-6 FPGA SelectIO Resources User Guide**
This guide describes the SelectIO™ resources available in all Virtex-6 devices.
- **Virtex-6 FPGA GTX Transceivers User Guide**
This guide describes the GTX transceivers available in all Virtex-6 FPGAs except the XC6VLX760.

- Virtex-6 FPGA Embedded Tri-Mode Ethernet MAC User Guide
This guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in all Virtex-6 FPGAs except the XC6VLX760.
- Virtex-6 FPGA DSP48E1 Slice User Guide
This guide describes the architecture of the DSP48E1 slice in Virtex-6 FPGAs and provides configuration examples.
- Virtex-6 FPGA System Monitor User Guide
The System Monitor functionality available in all Virtex-6 devices is outlined in this guide.
- Virtex-6 FPGA PCB Design Guide
This guide provides information on PCB design for Virtex-6 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Support Resources

To search the database of silicon and software questions and answers or to create a technical support case in WebCase, see the Xilinx website at:

<http://www.xilinx.com/support>.

ML605 Evaluation Board

Introduction

The Virtex®-6 FPGA ML605 Evaluation Kit [Ref 1] is the Xilinx base platform for developing system designs that demand high-performance, serial connectivity and advanced memory interfacing. This yields design applications for markets such as wired telecommunications, wireless infrastructure, broadcast and many others. Integrated tools help streamline the creation of elegant solutions to complex design requirements.

The ML605 Evaluation Kit is based on the XC6VLX240T-1FFG1156 Virtex-6 FPGA [Ref 2]. This FPGA contains 241,152 logic cells, a rating that reflects the increased logic capacity offered by the 6-input LUT architecture. For additional information, see the *Virtex-6 Family FPGAs Product Table* at

http://www.xilinx.com/publications/prod_mktg/Virtex6_Product_Table.pdf.

A Built-In Self Test (BIST), feature demonstrations, and reference design files are provided with the ML605 Evaluation Kit. The CompactFlash card included with the kit contains a BIST application. The BIST provides a convenient way to test many of the board's features on power-up and upon reconfiguration through the System ACE CF JTAG interface. After running through the tutorial provided in the *Getting Started with the Xilinx Virtex-6 FPGA ML605 Evaluation Kit* [Ref 3], the tutorials and reference designs available on the ML605 Web page can be used to further explore the capabilities of the ML605 and the Virtex-6 FPGA.

For the most up-to-date information on the demonstration content provided with the ML605 Evaluation Kit, see the ML605 Reference Design Web page at

http://www.xilinx.com/products/boards/ml605/reference_designs.htm.

ML605 Features

The ML605 designs demonstrate Virtex-6 FPGA features using the ML605 evaluation board. These features include:

- DDR3 SODIMM
- 16 MB Platform Flash XL
- 32 MB Linear BPI Flash
- System ACE CF
- USB JTAG
- 16 x 2 LCD character display
- Video VGA
- USB host and peripheral
- Ethernet (10/100/1000) with SGMII
- GTX port with SMA x4
- 200 MHz differential clock, 66 MHz socketed oscillator, clock SMA connectors
- MGT clocking SMA x4
- VITA 57.1 FMC HPC connector
- VITA 57.1 FMC LPC connector
- PCIe® Gen1 (8-lane), Gen2 (4-lane)
- UART (via USB cable)
- IIC EEPROM
- LEDs
- DIP switch
- Pushbuttons
- System Monitor
- Power monitoring
- Power supply: 12V AC adapter or 12V 4-pin ATX

For detailed information on the features of the ML605 board, see the *ML605 Hardware User Guide*. [\[Ref 1\]](#)

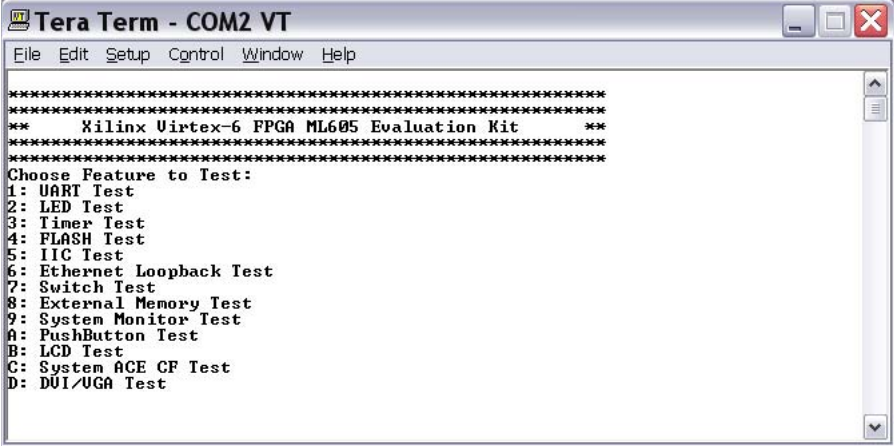
Reference Designs

- [Built-In Self Test \(BIST\)](#)
- [Memory Interface Generator \(MIG\) DDR3 Design](#)
- [Integrated Block for PCI Express](#)
- [MultiBoot Design](#)
- [ChipScope Pro IBERT Design](#)
- [System Monitor](#)

Built-In Self Test (BIST)

The BIST tests many of the features offered by the ML605 Evaluation Kit. When configured to boot from the CompactFlash memory, the BIST menu appears on power-up. After FPGA configuration, the text shown in [Figure 1-1](#) appears in a terminal program window, such as Tera Term. Type the number associated with one of the listed tests to run the test application. For example, typing a “5” results in the IIC Test application being run.

See the *ML605 Built-In Self Test Flash Application* tutorial for more information on the BIST software and its operation. [\[Ref 22\]](#)



```
Tera Term - COM2 VT
File Edit Setup Control Window Help
*****
**      Xilinx Virtex-6 FPGA ML605 Evaluation Kit      **
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: System Monitor Test
A: PushButton Test
B: LCD Test
C: System ACE CF Test
D: DUI/UGA Test
```

Figure 1-1: BIST Initial Screen

The default location of the BIST program is at System ACE CF configuration address 0 on the CompactFlash (CF) card included with the ML605 Evaluation Kit. The *ML605 Restoring Flash Contents* tutorial provides instructions for restoring the image to its factory default content. [\[Ref 29\]](#)

Memory Interface Generator (MIG) DDR3 Design

The Virtex-6 FPGA memory interface solutions core (Figure 1-2) provides high-performance connections to DDR3 and DDR2 SDRAMs, and QDR II+ SRAM. The physical layer (PHY) side of the design is connected to the DDR2 or DDR3 SDRAM device via FPGA I/O blocks (IOBs) and the user interface (UI) side is connected to the user design via FPGA logic.

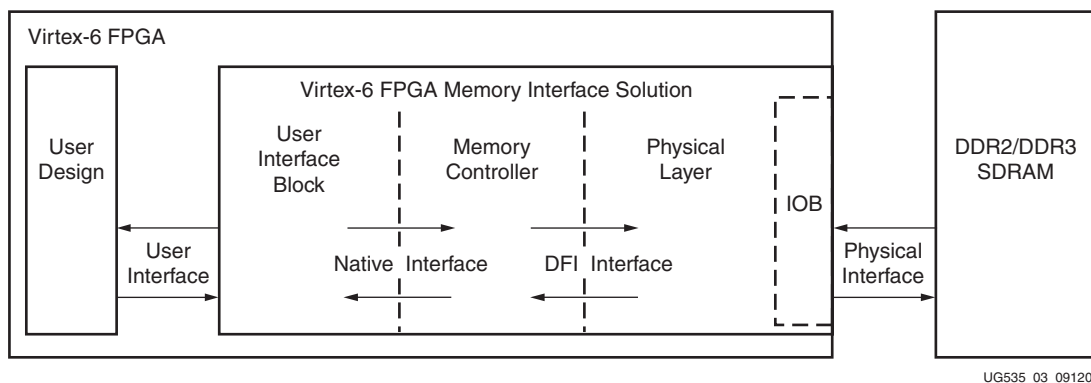


Figure 1-2: Virtex-6 FPGA Memory Interface Solution

The ML605 DDR3 SODIMM design and associated tutorial demonstrates the high effective bandwidth of a MIG-generated 64-bit DDR3 memory application. The example design includes a ChipScope Pro interface to the memory controller's physical layer logic. This interface is used for monitoring the status of read calibration, write calibration, phase detector control and to verify the written data patterns.

See the *ML605 MIG Design Creation* tutorial for more information on the DDR3 memory application. [Ref 23]

The MIG tool (Figure 1-3) can be used to create a simple user interface. See the *Virtex-6 FPGA Memory Resources User Guide* [Ref 9] for more information on MIG.



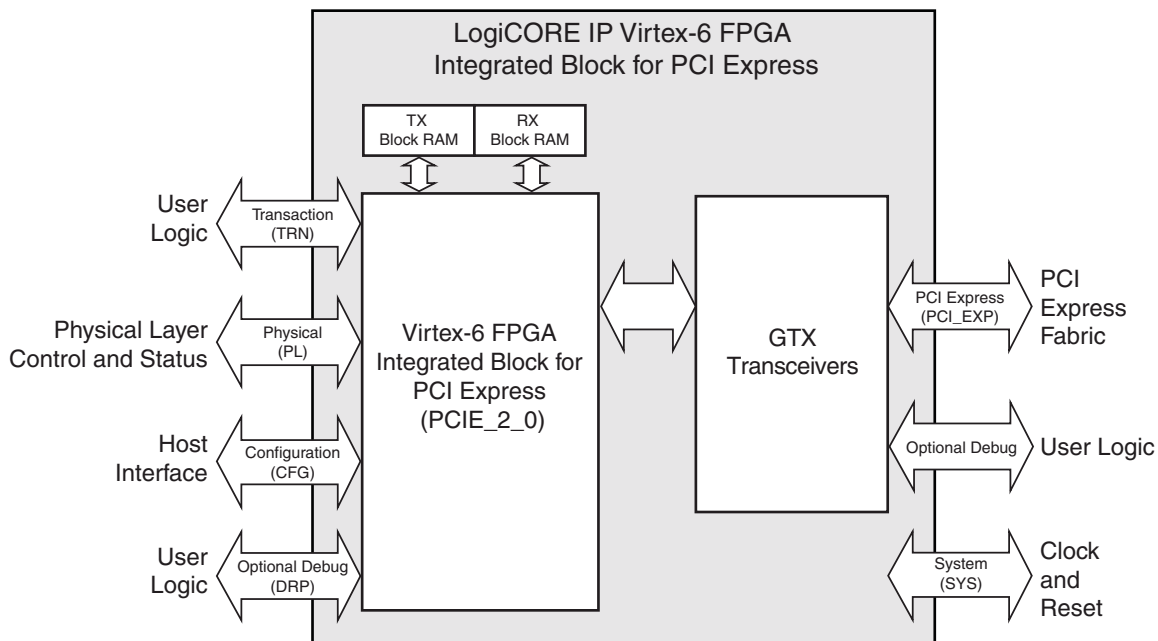
Figure 1-3: MIG Graphical User Interface

Integrated Block for PCI Express

The LogiCORE™ IP Virtex-6 Integrated Block for PCI Express® is a reliable, high-bandwidth, scalable serial interconnect building block for use with the Virtex-6 FPGA family. The core instantiates the Virtex-6 Integrated Block for PCI Express found in the Virtex-6 family, and supports only Verilog®-HDL.

The Integrated Block for PCIe core internally instances the Virtex-6 Integrated Block for PCI Express. The integrated block follows the PCI Express Base Specification layering model, which consists of the Physical, Data Link, and Transaction Layers. The integrated block is compliant with the *PCI Express Base Specification v2.0*.

The LogiCORE™ IP Virtex-6 Integrated Block for PCI Express core is a high-bandwidth, scalable, and reliable serial interconnect building block for use with Virtex-6 FPGA devices. The Integrated Block for PCI Express (PCIe®) solution supports 1-lane, 2-lane, 4-lane, and 8-lane Endpoint operation at up to Gen2 speed, all of which are compliant with the PCI Express Base Specification v2.0. [Ref 19] [Ref 20]



UG535_04_091209

Figure 1-4: Top-level Function Blocks and Interfaces

The ML605 provides an 8-lane PCIe edge connector for Endpoint applications. Tutorials and design files describe how to use the CORE Generator™ tool to create PCIe Gen1 x8 and PCIe Gen2 x4 LogiCORE IP blocks. The generated PCIe designs contain a Programmed Input/Output (PIO) example that utilizes FPGA Block RAM to create a memory space accessible from the PCIe interface. A PCIe utility program, running on a PC host, is then used to query configuration space and to read and write FPGA memory over the PCIe interface.

See the tutorials, *ML605 PCIe x8 Gen1 Design Creation* [Ref 24] and *ML605 PCIe x4 Gen2 Design Creation* [Ref 25], for more information.

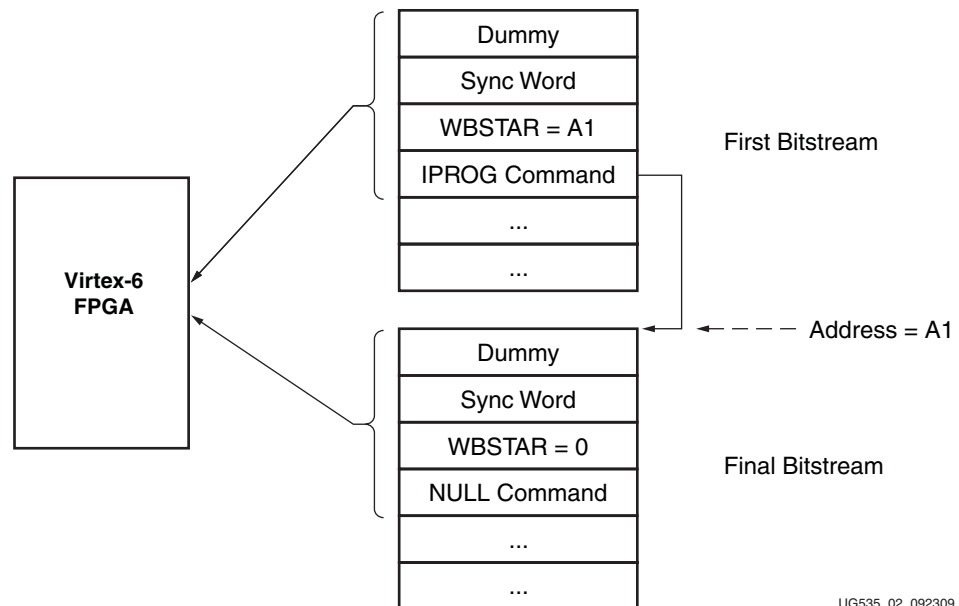
MultiBoot Design

MultiBoot is the process by which the FPGA selectively reprograms and reloads its bitstream from an attached external memory. This feature allows field updating of a stored bitstream with a new bitstream while guarding against system upsets due to an update failure. A general update process is accomplished in a five step procedure:

1. New MultiBoot image is created
2. System setup to receive the new image
3. User application erases section of Flash
4. The new image is delivered into the system's Flash
5. User application resets system

The MultiBoot tutorial demonstrates the ability to switch between two FPGA configurations initiated by a user logic event. The provided reference design utilizes the Internal Configuration Access Port (ICAP), the IPROG command and the FPGA Warm Boot Start Address Register (WBSTAR) to illustrate the Virtex-6 MultiBoot capability.

For additional information on the Virtex-6 MultiBoot feature, see the *Virtex-6 FPGA Configuration User Guide* [Ref 10]. For a demonstration of this operation on the Virtex-6 FPGA, see the *ML605 MultiBoot Design* tutorial [Ref 26].



UG535_02_092309

Figure 1-5: IPROG Embedded in the Bitstream

ChipScope Pro IBERT Design

The CORE Generator tool provides designers using the Virtex-6 GTX transceivers the ability to generate a hardware design containing an Integrated Bit Error Ratio Test (IBERT) core. The IBERT core instantiates a design with Virtex-6 GTX transceivers, data pattern generators, and data pattern checkers. The generated hardware design is based on user input for the device part and package, the location of a system clock pin, the desired GTX reference clock, and the expected line rate. Once configured, the IBERT design running in the FPGA is controlled through the ChipScope Pro Analyzer's IBERT Console to set GTX transceiver attributes and to exercise the high-speed serial GTX transceivers.

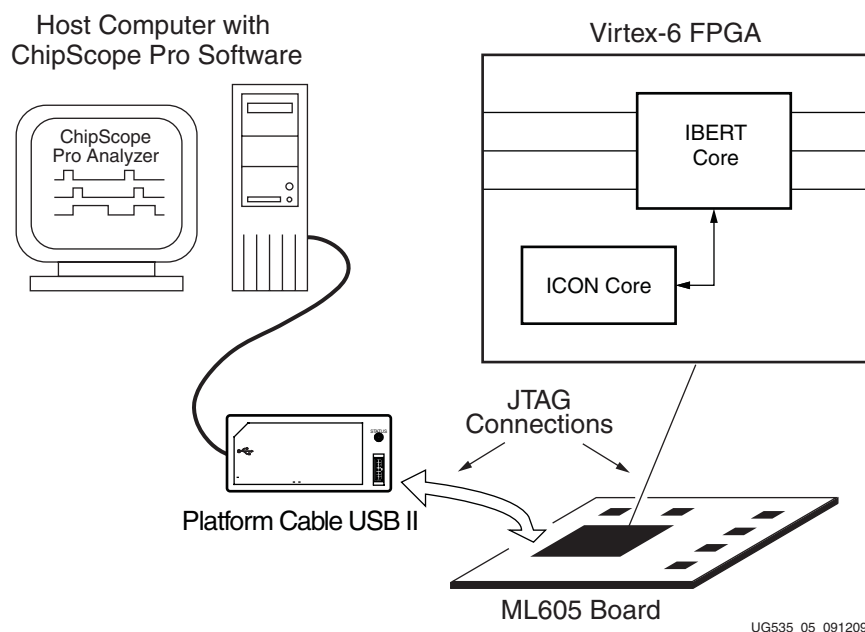


Figure 1-6: IBERT Core Generated Using ChipScope Pro Software

The LogiCORE IBERT designs verify loopback connections over the following interfaces that use the GTX transceivers:

- SFP
- SMA
- Ethernet SGMII
- PCIe
- FMC-HPC
- FMC-LPC

The *ML605 GTX IBERT Design Creation* tutorials and accompanying reference designs illustrate how to use the CORE Generator tool and the ChipScope Pro Analyzer software to exercise the ML605 GTX transceivers. [Ref 27]

For information about the ChipScope Pro Analyzer tool, refer to the *ChipScope Pro Software and Cores User Guide* [Ref 4].

System Monitor

Every member of the Virtex-6 FPGA family contains a single System Monitor, which is located in the center of every die. The System Monitor function is built around a 10-bit, 200-kSPS (kilo-samples per second) Analog-to-Digital Converter (ADC) with digital averaging. When combined with a number of on-chip sensors, the ADC is used to measure FPGA physical operating parameters like on-chip power supply voltages and die temperatures. Access to external voltages is provided through a dedicated analog-input pair (VP/VN) and 16 user-selectable analog inputs, known as auxiliary analog inputs. The external analog inputs allow the ADC to monitor the physical environment of the board or enclosure. System Monitor is fully functional on power up, and measurement data can be accessed via the JTAG port before, during, and after configuration.

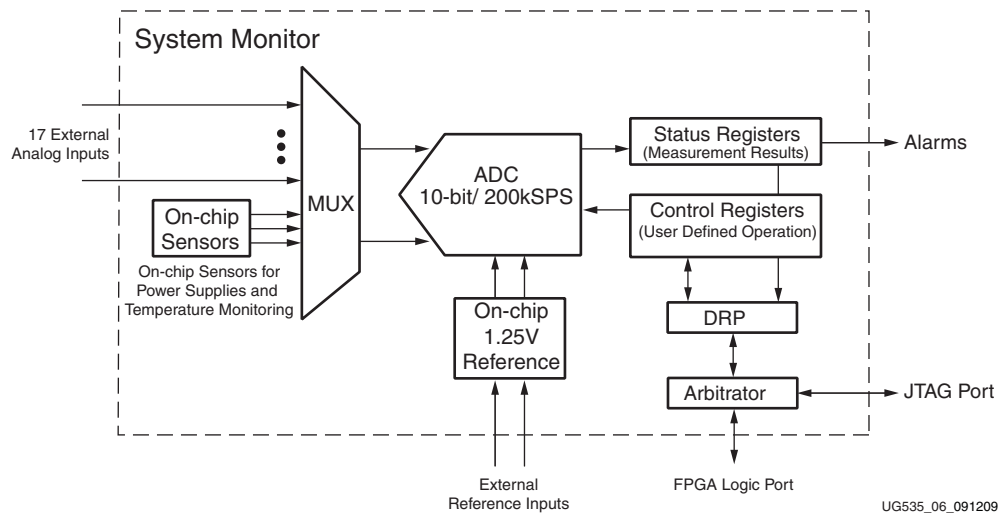


Figure 1-7: System Monitor Block Diagram

The System Monitor will run in a terminal program window, such as Tera Term, displaying the text shown in Figure 1-8. See the *ML605 System Monitor* tutorial for more information. [Ref 28]

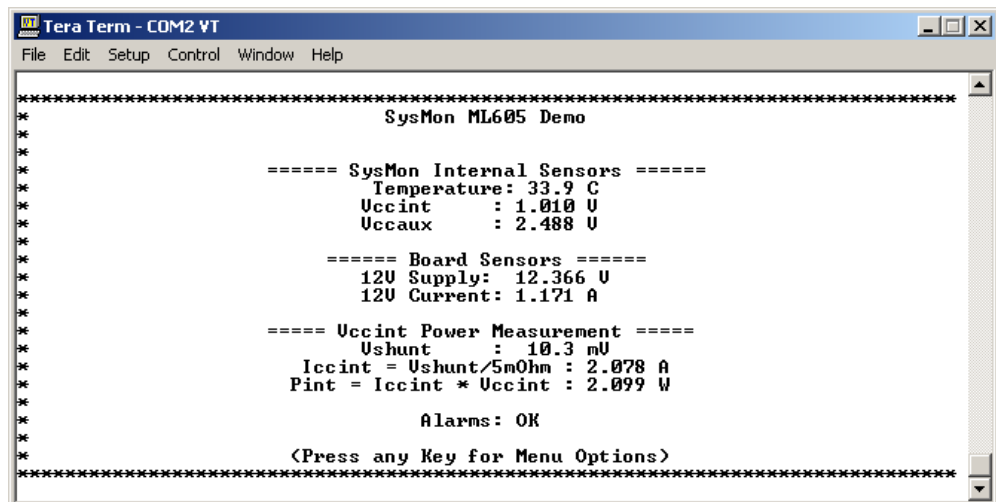


Figure 1-8: System Monitor Test

Stand-Alone Applications

Each feature on the board can be tested for functionality by using the BIST application [Ref 22] or the tutorials and designs offered on the ML605 Web page.

Table 1-1 describes the stand-alone applications for the ML605 board.

Table 1-1: **Stand-Alone Applications**

| Feature | Feature Test Capability |
|--|---|
| Virtex-6 FPGA | BIST |
| DDR3 SODIMM | BIST |
| 128 Mb Platform Flash XL | SelectMAP Configuration Mode |
| Linear BPI Flash | BIST, BPI-UP Configuration Mode |
| System ACE CF Socket, Controller | BIST |
| JTAG Cable Connector (USB-Mini-B) | Configuration |
| Clock Generation | 200 MHz system clock, 66 MHz populated socket, user SMA |
| GTX RX/TX Port | IBERT Web Tutorial |
| PCIe Gen1 (8-lane), Gen2 (4-lane) | PCIE and IBERT Web Tutorials |
| SFP Connector and Cage | IBERT Web Tutorial |
| Ethernet (10/100/1000) with SGMII | IBERT Web Tutorial |
| USB-Mini-B USB-to-UART bridge | BIST |
| USB-A Host, USB-Mini-B peripheral connectors | Factory Test |
| Video-VGA | BIST |
| LED (Ethernet PHY) | BIST |
| LEDs (INIT/DONE) | BIST |
| User LEDs: Green (8), Green (5), Directional | BIST |
| User DIP Switch | BIST |
| User pushbuttons (directional, N.O. momentary) | BIST |
| LCD 16-character x 2-line display | BIST |
| Switches (PROG, ON/OFF, Mode DIP) | BIST |
| FMC-HPC Connector | Factory Test |
| FMC-LPC Connector | Factory Test |
| Power Management | Factory Test |
| 12V Power Input Connectors | BIST |
| System Monitor Interface Connector | BIST, Web Tutorial |

Restoring Flash Contents

The ML605 Evaluation Kit contains several non-volatile memories (Platform Flash XL, Linear BPI Flash, Compact Flash) that can be overwritten by user created designs. The *Restoring Flash Contents* tutorial [\[Ref 29\]](#) provides a means to re-establish the original functionality programmed into the flash memories.

References

This section provides references to documentation supporting Virtex-6 FPGAs, tools, and IP. For additional information, see www.xilinx.com/support/documentation/index.htm.

1. [UG534](#), *ML605 Hardware User Guide*
2. [DS150](#), *Virtex-6 Family Overview*
3. [UG525](#), *Getting Started with the Xilinx Virtex-6 FPGA ML605 Evaluation Kit*
4. [UG029](#), *ChipScope Pro Software and Cores User Guide*
5. [DS152](#), *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*
6. [UG360](#), *Virtex-6 FPGA Configuration User Guide*
7. [UG361](#), *Virtex-6 FPGA SelectIO Resources User Guide*
8. [UG362](#), *Virtex-6 FPGA User Guide: Clocking Resources*
9. [UG363](#), *Virtex-6 FPGA Memory Resources User Guide*
10. [UG364](#), *Virtex-6 FPGA Configurable Logic Block User Guide*
11. [UG365](#), *Virtex-6 FPGA Packaging and Pinout Specifications*
12. [UG366](#), *Virtex-6 FPGA GTX Transceivers User Guide*
13. [UG369](#), *Virtex-6 FPGA DSP48E1 Slice User Guide*
14. [DS186](#), *Virtex-6 FPGA Memory Interface Solutions Data Sheet*
15. [UG370](#), *Virtex-6 FPGA System Monitor User Guide*
16. [DS643](#), *Multi-Port Memory Controller (MPMC) (v5.02a) Data Sheet*
17. [UG086](#), *Memory Interface Solutions User Guide*
18. [UG138](#), *LogiCORE™ IP Tri-Mode Ethernet MAC v4.2 User Guide*
19. [UG517](#), *LogiCORE™ IP Virtex-6 FPGA Integrated Block User Guide v1.3 for PCI Express*
20. [DS715](#), *Virtex-6 FPGA Integrated Block v1.3 for PCI Express Data Sheet*
21. [Platform Studio EDK](#)

ML605 tutorials, demonstration, and design files are located at http://www.xilinx.com/products/boards/ml605/reference_designs.htm:

22. [XTP056](#), *ML605 Built-In Self Test Flash Application (rdf0017.zip)*
23. [XTP047](#), *ML605 MIG Design Creation (rdf0011.zip)*
24. [XTP044](#), *ML605 PCIe x8 Gen1 Design Creation (rdf0008.zip)*
25. [XTP045](#), *ML605 PCIe x4 Gen2 Design Creation (rdf0009.zip)*
26. [XTP043](#), *ML605 MultiBoot Design (rdf0007.zip)*
27. [XTP046](#), *ML605 GTX IBERT Design Creation (rdf0010.zip)*
28. [XTP048](#), *ML605 System Monitor (rdf0012.zip)*
29. [XTP055](#), *ML605 Restoring Flash Contents (rdf0021.zip, rdf0022.zip)*