



Top Marking Change for UltraScale+ Defense-grade “XQ” Products

XCN18016 (v1.0) May 28, 2018

Product Change Notice

Overview

The purpose of this notification is to advise customers of top marking changes for Xilinx® UltraScale+™ Defense-grade “XQ” devices. There are no changes to fit, form, function, or reliability.

Description

Xilinx will be simplifying the topside marking for all Xilinx UltraScale+ Defense-grade “XQ” devices. All topside marking will be removed with the exception of Xilinx logo, 2D barcode, and country of origin. Device and package information will be accessed through the Xilinx 2D barcode application (refer to [AR# 67513](#)). This will allow much improved device-level traceability and security.

The 2D barcode contains a unique serial number that must be scanned using a camera based application to determine the serial number. The device and package information that were previously found on the top marking can only be retrieved using the unique serial number through an internet based application either on a mobile device or through a web browser using a portal (refer to [XTP424](#) or [XCN16014](#) for details). Scanning the existing License Plate Number (LPN) provided on the inner box and bag label will allow access to all device information and codes contained within a specific bag or box using the same portal.

Products Affected

This change affects all package, speed, and temperature grade variations for Xilinx UltraScale+ Defense-grade “XQ” devices. All associated specification control document (SCD) devices are also affected. Xilinx UltraScale+ Defense-grade “XQ” devices not yet in production will only ship with the new simplified top marking.

Key Dates and Ordering Information

Xilinx will begin shipping devices with new top marking starting August 27, 2018. Products with current top marking as shown in [Table 1](#), [2](#) and [3](#), will cross ship until existing inventory is depleted.

Table 1: UltraScale+ Zynq® MPSoC XQ Devices-Packages

Device	Package-Pin	Device	Package-Pin
XQZU3EG	SFQC784	XQZU11EG	FFQC1156
XQZU4EG		XQZU11EG	FFQC1760
XQZU4EG	FBQB900	XQZU19EG	
XQZU6EG	FFQC900	XQZU19EG	
XQZU9EG		XQZU9EG	
XQZU9EG	FFQB1156		
XQZU9CG			

Table 2: UltraScale+ Kintex® XQ Devices-Packages

Device	Package-Pin	Device	Package-Pin
XQKU11P	FFQA1156	XQKU11P	FFQE1517

Table 3: UltraScale+ Virtex® XQ Devices-Packages

Device	Package-Pin	Device	Package-Pin
XQVU7P	FLQA2104	XQVU9P	FSQD2104
XQVU7P	FLQB2104	XQVU13P	FLQA2577
XQVU9P			
XQVU9P	FLQC2104		

Traceability

Affected devices are identified by the following package top marking as shown in Figure 1 below.



Figure 1: Product Marking

Response

No response is required.

Important Notice: Xilinx Customer Notifications (XCNs, XDNs, and Quality Alerts) can be delivered via e-mail alerts sent by the Support website (<https://www.xilinx.com/support>). Register today and personalize your “Documentation and Design Advisory Alerts” area to include Customer Notifications. Xilinx Support provides many benefits, including the ability to receive alerts for new and updated information about specific products, as well as alerts for other publications such as data sheets, errata, application notes, etc. For information on how to sign up, refer to [Xilinx Answer Record 18683](#).

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
05/28/2018	1.0	Initial Release.

Notice of Disclaimer

The information disclosed to you hereunder (the “Materials”) is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx’s limited warranty, please refer to Xilinx’s Terms of Sale which can be viewed at <http://www.xilinx.com/legal.htm#tos>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx’s Terms of Sale which can be viewed at <http://www.xilinx.com/legal.htm#tos>.