

## Overview

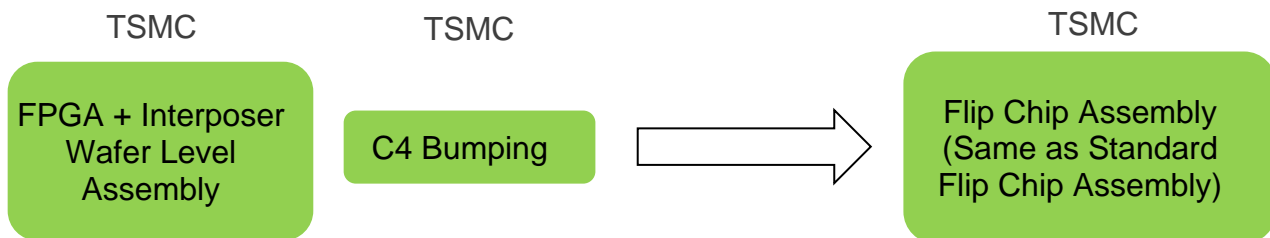
The purpose of this notification is to announce second source supplier qualification of substrate level assembly for SSIT (Stacked Silicon Interconnect Technology) products. There is no change in form, fit, function or reliability.

## Description

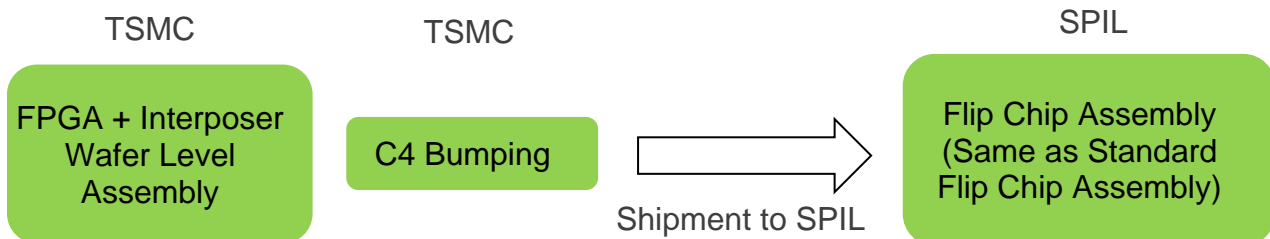
Xilinx qualified SPIL (Siliconware Precision Industries) as a second source supplier for substrate level assembly of stacked die wafers assembled at TSMC. SPIL has been Xilinx's qualified primary flip chip assembly supplier for over 17 years.

In this process flow, TSMC will complete the active die assembly on an interposer and will ship the stacked wafer to SPIL after C4 bumping. SPIL will assemble the stacked die wafer onto substrate similar to a standard flip chip assembly. There is no change in any material sets and the same packaging materials will be used for both process flows. This change is to ensure SSIT product supply continuity.

## Current Process



## Second Source Process



## Products Affected

This change affects all speed, package, and temperature variations of XQ products reflected in [Table 1](#). Any associated specification control document (SCD) versions of the standard part numbers are also affected.

Table 1: UltraScale™ FPGA Products Affected

Device	Package-Pin
XQKU115	RLD1517
	RLF1924

## Key Dates and Ordering Information

Xilinx will start cross-shipping from both assembly sites starting June 1, 2019.

## Qualification Data

Xilinx qualification data for UltraScale (20nm) production parts will be available upon request.

## Traceability

Each assembly lot will be built with a unique lot number. The actual assembly location can be identified by the lot number.

## Response

No response is required.

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## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/18/2019	1.0	Initial release.

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