Reliability Testing Summary
UMC (0.18 um process)
Qualification & Monitor Data Combined

Technology:	**Si Gate CMOS**
Device Type:	**XCVXXXE**
Package Type:	**Various**
Assumed Activation Energy:	**0.7ev, (60% Confidence level)**

	Life Test	HAST	Temp. Cycle
	145C	100Hrs	1,000 Cycs. -65C/+150C
Combined Started Lot:	13	1	8
Failures:	2	0	0
Device on test:	500	76	349
Actual device hours :	318,156	7,600	365,097
Mean :	636	100	1,046
Equivalent device hours @ Tj=125C:	844,540		
Equivalent device hours @ Tj=55C:	65,724,597		
Equivalent device hours @ Tj=25C:	7.95E+08		
Failure Rate(60% C.L.) in FITS @ Tj=55C:	47		
Failure Rate(60% C.L.) in FITS @ Tj=25C:	4		

Failure Analysis:

F/A 99262 - 1 unit failed after 256 hrs of HTOL. The failure mode was leakage current on pin 153 (13.03µA vs. 10 µA). Failure mechanism was a pin hole in the gate oxide. Test was repeated with new wafer lot and with ongoing process monitors but the failure could not be reproduced. This failure is considered a random defect.

F/A-00061 - 1 unit failed after 168 hrs of HTOL. The failure mode was a failure of the HEX line test pattern. Failure mechanism was a metal etch defect due to particle contamination during the photo mask step. This failure is considered a random defect.