May 15, 2002

Product Change Notification PCN2002-07

Virtex™-E Wafer Fabrication Update

(Not applicable to Virtex and Virtex-II product families)

Overview:

This notification is to inform you of some important changes to the Virtex-E product family. The Virtex-E product family will transfer to a 0.18µm (transistor) / 0.15µm (interconnect) 6-layer metal hybrid process on 12-inch wafers at UMC, Taiwan. The only exceptions to this change are the XCV1600E, which will continue to be manufactured on a 0.18µm process on 8-inch wafers, and the XCV2600E and XCV3200E which will continue to be manufactured on the 0.18µm / 0.15µm hybrid process on 8-inch wafers. The following table summarizes the transition plan for each member of the Virtex-E family:

	FROM		TO
	8-inch		12-inch
	0.18µm	0.18µm/ 0.15µm	0.18µm/ 0.15µm
XCV50E	√		√ (qualification complete)
XCV100E	√		√ (qualification complete)
XCV200E	√		√ (qualification complete)
XCV300E	√		√ (qualification complete)
XCV400E	√		√ (qualification complete)
XCV600E	√		√ (qualification complete)
XCV1000E	√	√	√ (qualification complete)
XCV1600E	√		No change
XCV2000E	√	√	√ (qualification complete)
XCV2600E		√	No change
XCV3200E		√	No change

The Virtex-E 0.18µm / 0.15µm hybrid process on 12-inch wafers is pin, function, timing, and programming file compatible with the existing 0.18µm and 0.18µm / 0.15µm hybrid processes on 8-inch wafers. All other key features, such as power supply voltage, and number of metallization layers remain unchanged. The change was initiated to improve Xilinx's ability to support this product effectively, competitively, and to accommodate our customers' high volume demand.

Key Dates:

The qualification of the 0.18µm / 0.15µm hybrid process on 12-inch wafers has been completed. The mask qualifications for the XCV50E, XCV100E, XCV200E, XCV300E, XCV400E, XCV600E, XCV1000E and XCV2000E (manufactured on the 0.18µm / 0.15µm hybrid process on 12-inch wafers) have also been completed. Fully-qualified, production-released material will be available for customers to sample on May 15, 2002.

Starting May 15, 2002, customers can specify 0.18µm / 0.15µm process material on 12-inch wafers by using special ordering number SCD0773. To use SCD0773, append "0773" to the end of the standard ordering part number (e.g., XCV1000E-6FG680C**0773**). Only 0.18µm / 0.15µm process material on 12-inch wafers will be used to fulfill SCD0773 orders. The four-digit SCD number (0773) is top marked on the device (see the example in the Traceability section).

Beginning August 15, 2002, customers may expect to receive XCV50E, XCV100E, XCV200E, XCV300E, XCV400E, XCV600E, XCV1000E, and XCV2000E devices from either the 0.18µm (on 8-inch wafers) or the 0.18µm / 0.15µm processes (on 8-inch or 12-inch wafers) when ordering the standard part number.

Customers who need product manufactured on the 0.18µm process on 8-inch wafers beyond the onset of device cross-shipment (August 15, 2002), may do so on a short-term basis only by using special ordering number SCD0707. To use SCD0707, append "0707" to the end of the standard ordering part number (e.g., XCV1000E-6FG680C**0707**). Only 0.18µm process material on 8-inch wafers will be used to fulfill SCD0707 orders. SCD0707 is available for use starting May 15, 2002, and will be discontinued after December 31, 2002. The four-digit SCD number (0707) is top marked on the device (see the example in the Traceability section).

The following table summarizes the SCD usage for Virtex-E:

SCD #:	SCD DESCRIPTION:	EXAMPLE OF ORDERING PART #:	SCD AVAILABLE ON:	SCD DISCONTINUED ON:
SCD0707	0.18µm process on 8-inch wafers	XCV1000E-6FG680C0707	May 15, 2002	December 31, 2002
SCD0773	0.18µm / 0.15µm process material on 12-inch wafers	XCV1000E-6FG680C0773	May 15, 2002	No planned discontinue date for SCD0773

Qualification Data: The following is the qualification data for the 0.18µm / 0.15µm hybrid process on 12-inch wafers at UMC, Taiwan:

Lot #	Part	Package	Test	Quantity	Hours/Cy	Fails	Status
X0016LT	XCV300E	PQ240	HTOL	76	24	0	continue
			@145°C		48	0	continue
					256	0	continue
					500	0	continue
					1000	0	complete
X0020LT	XCV300E	PQ240	HTOL	76	24	0	continue
			@145°C		48	0	continue
					256	0	continue
					500	0	continue
					1000	0	complete
X0039LT	XCV300E	PQ240	HTOL	78	24	0	continue
			@145°C		48	0	continue
					168	0	continue
					256	0	continue
					500	0	continue
					1000	0	continue
					1500	0	complete
X0040LT	XCV300E	PQ240	HTOL	12	24	0	continue
			@145°C		48	0	continue
					256	0	continue
					500	0	continue
					1000	0	complete
X0017HS	XCV300E	PQ240	HAST	76	100	0	complete
			@130°C/85%RH				
X0015TC	XCV300E	PQ240	Temp Cycle	79	200	0	continue
			@-65°C / +150°C		500	0	continue
			Condition C		1000	0	complete

Traceability:

These devices can be distinguished by a 3-letter code located on the second line of the package topmark in between the package/pin code and the datecode. The combination of the 2nd and 3rd letter of this 3-letter code can be used to identify the wafer fabrication location and process geometry:

2nd Letter:	3rd Letter:	Description:
F	S	0.18µ process on 8-inch wafers
M	S	0.18µ process on 8-inch wafers
F	T	0.18µ / 0.15µ hybrid process on 8-inch wafers
M	T	0.18µ / 0.15µ hybrid process on 12-inch wafers

Amendment to this PCN: To enhance Xilinx's traceability system, a new wafer fabrication code "G" was added in October 2002 to identify all material manufactured at UMC's 12-inch wafer fabrication facility. The 2nd letter of the 3-letter code will be a "G" for any product built at UMC's 12-inch wafer fabrication facility.

Example of a package topmark:

	ACTUAL TOPMARK	DESCRIPTION
Line 1:	XCV1000E™	Xilinx Device Type
Line 2:	FG680AMT0245	FG680 = Package Type A = Circuit Design Revision M, T = 0.18µm/0.15µm process, 12-inch wafers 0245 = Date Code
Line 3:	F1130085A	Assembly Lot Number
Line 4:	6C -0773	6 = Speed C = Grade 0773 = SCD Number

Response and Contact:

Per JEDEC Standard JESD46-B, customers should acknowledge receipt of the PCN within 30 days of delivery of the PCN. Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change. After acknowledgement, lack of additional response within the 90-day period constitutes acceptance of the change.

To obtain samples or production devices, please contact your Xilinx Sales Representative. For additional information or questions on this PCN, please contact the Quality Assurance group via email at pcn@xilinx.com, or directly by fax at (408) 369-1718.