November 8, 2002

PCN2002-11: CoolRunner XCR3256XL CPLD
Change in Wafer Fabrication Facility

Overview: This notification is to inform you of a change in the wafer fab facility for the XCR3256XL™ CoolRunner™ XPLA3™ CPLD. The XCR3256XL will transition from a 0.35µm five-layer metal Flash CMOS process at the Philips MOSIV wafer fab in Nijmegen to a 0.35µm five-layer metal Flash CMOS process at UMC, Taiwan. Another member of the XPLA3 family – XCR3064XL™ – has transitioned from the Philips MOSIV plant to UMC earlier this year, reference PCN2002-04.

This change is being made to improve Xilinx's ability to support this product effectively, competitively, and to accommodate our customers' high volume demands.

One other member of the XPLA3 family – XCR3128XL™ – is also fabricated at the Philips MOSIV plant, but is not scheduled for transition to the UMC facility at this time. A separate process change notification will be communicated at a later date if necessary. The remaining members of the family – XCR3032XL™, XCR3384XL™ and XCR3512XL™ – have always been fabricated at the UMC fab using the same 0.35µm five-layer metal Flash CMOS process technology which will now be used to fabricate the XCR3256XL.

Upon availability of the production units from UMC on February 7, 2003, customers may expect to receive the XCR3256XL device from either UMC or MOSIV until the MOSIV inventory is depleted.

The XCR3256XL devices fabricated at UMC exhibit some performance improvements. The following table lists the datasheet changes that occur as a result of the change in fabrication location:

Data sheet measurement	Current MOSIV spec	UMC spec
Write / erase cycles	1,000	10,000
V_{OH}	Min. of 2.4V when I_{OH} = -8 mA	No change when V_{CC} = 3.0 V to 3.6V Adding the following conditions: If V_{CC} = 2.7V to 3.0V, min = 2.0V If I_{OH} = -500µA, min = 90% V_{CC}
T_{PTCK}[1]	Not present	7.5 ns Tpd = 2.0 ns 10 ns Tpd = 2.5 ns 12 ns Tpd = 3.0 ns
f_{SYSTEM}	7.5 ns Tpd = 140 MHz	7.5 ns Tpd = 155 MHz No change to –10 or –12 speeds
T_F	7.5 ns Tpd = 2.8 ns	7.5 ns Tpd = 2.2 ns No change to –10 or –12 speeds
T_{LOGI3} (Fold-back NAND delay)	7.5 ns Tpd = 6.0 ns 10 ns Tpd = 8.0 ns 12 ns Tpd = 9.5 ns	7.5 ns Tpd = 2.0 ns 10 ns Tpd = 2.5 ns 12 ns Tpd = 3.0 ns

[1]This parameter added to the XPLA3 Family timing model for T_{PCO} measurement. T_{PCO} for the XCR3256XL does not change as a result of this fabrication location change. See the family data sheet (DS012) for timing model information.

The XCR3256XL devices fabricated at UMC require an updated BSDL file. This updated BSDL file can be found at http://www.xilinx.com/support/sw_bsdl.htm#CPLD and will also function with the XCR3256XL devices fabricated at MOSIV.

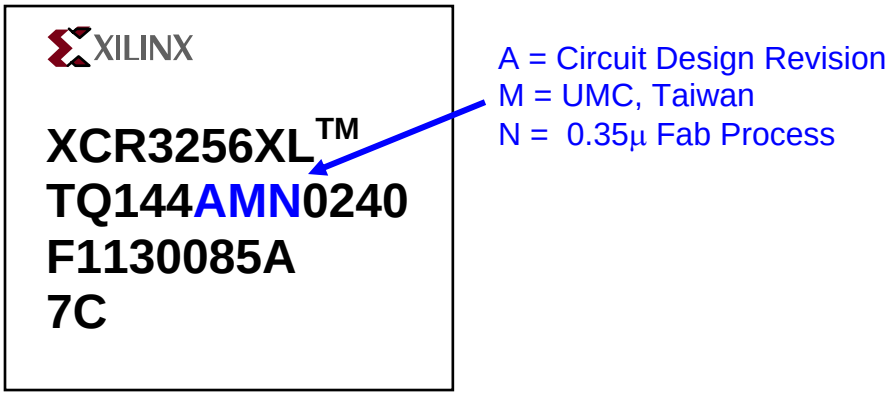
Qualification Data: The following is the qualification data for the 0.35µm process at UMC:

Lot #	Part	Package	Test	Quantity	Hours/Cy	Fails	Status
X8522LT	XCR3032XL	VQ44	HTOL	80	24	0	continue
			@145°C		48	0	continue
					256	0	continue
					500	0	continue
					1000	0	complete
X0026LT	XCR3032XL	VQ44	HTOL	80	256	0	complete
			@145°C				
X8535HS	XCR3032XL	VQ44	HAST	76	100	0	complete
			@130°C/85%RH				
X8535TC	XCR3032XL	VQ44	Temp Cycle	76	200	0	continue
			@-65°C / +150°C		500	0	continue
			Condition C		1000	0	complete

Key Dates: Qualification samples of the XCR3256XL fabricated at UMC are available today. Use special ordering number SCD0771 to obtain these qualification samples. These qualification samples will be equivalent to the production devices of the XCR3256XL fabricated at UMC that will be shipping starting February 7, 2003. Product specifically manufactured on the MOSIV process at Philips can be ordered until February 7, 2003, with a final delivery date of no later than May 9, 2003. Please contact your Xilinx Sales Representative to obtain qualification samples or production devices.

Traceability: These devices can be distinguished by a 3-letter code located on the second line of the package topmark in between the package/pin code and the datecode. The 3-letter code will be "AMN" for product manufactured at UMC, and "APN" for product manufactured at MOSIV. See example below.

Example of a package topmark:



Response and Contact: Please contact your Xilinx Sales Representative to obtain qualification samples or production devices. For additional information or questions, please contact Xilinx Technical Support.

Per JEDEC Standard JESD46-B, customers should acknowledge receipt of the PCN within 30 days of delivery of the PCN. Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change. After acknowledgement, lack of additional response within the 90-day period constitutes acceptance of the change.