Xilinx Stepping Methodology

XCN05025 (v1.1) December 9, 2005 Customer Notification - FYI

Overview

The purpose of this notification is to announce that Xilinx will be using the Stepping Methodology to enhance our production offerings to our customers. The Virtex™-4 LX and SX families will be the first families to leverage the Stepping Methodology.

Description

The Stepping Methodology (http://www.xilinx.com/products/quality/silicon-stepping.htm) provides time-to-market advantages to our customers by offering production solutions as soon as they are available.

Stepping is an identification system used to denote improvement or additional device capabilities in the Xilinx production offerings and can be explicitly ordered by the customer.

Since higher step devices are a functional superset of lower step devices, designs for lower step devices can be used in higher step silicon without customer intervention. As new steps are released, they automatically replace older stepped devices without any disruption to customers. If a design requires the capabilities of a particular step, customers can order that step.

Virtex-4 LX and SX families are the first Xilinx device families to adopt the Stepping Methodology. Xilinx currently offers LX and SX production Step 1 (initial production) devices. Step 2 devices have been extensively tested and are a functional superset of production Step 1 devices. Additionally, Step 2 devices are form, fit, function and bitstream compatible to Step 1 devices. The Step 2 devices, in conjunction with the ISE 7.1i Service Pack 4 (SP4) design tools, improve upon Step 1 devices by addressing the NBTI issue and eliminating restrictions of the following conditions:

- FPGA is powered but not configured for more than 10 minutes at a time (addressed by Step 2 silicon)
- DCM is held in reset for more than 10 seconds at a time (addressed by Step 2 silicon)
- DCM clock is stopped for more than 100 milliseconds at a time (addressed by Step 2 silicon and ISE 7.1i SP4 design tools, refer to Xilinx Answer 21435)

For more information on the Xilinx Stepping Methodology, refer to Xilinx Answer 20947.

Products Affected

All future Xilinx families can leverage the Stepping Methodology. Virtex-4 LX and SX families (including C and I grades, standard, and Pb-free parts) are the first Xilinx device families to adopt the Stepping Methodology. Xilinx will cross ship Step 2 or Step 1 against an order for standard C or I grade part.

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A Step is denoted on the last marking on the fourth line as indicated in the following figure:

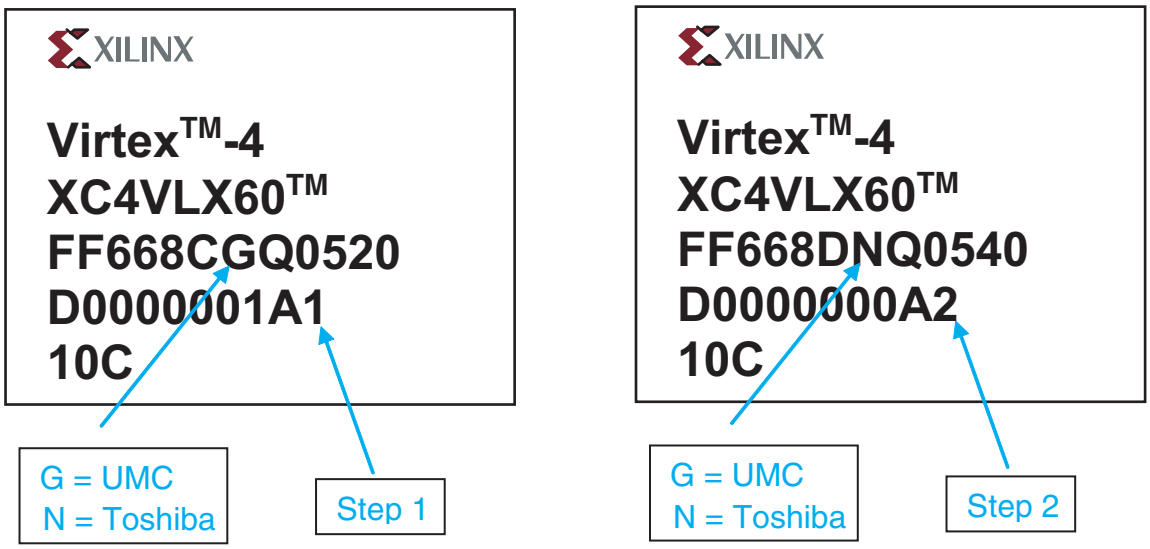

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Figure 1: **Package Top Mark**

Virtex-4 Step 1 devices may not all have the "1" indicated in the device top mark.

Key Dates

Starting in November 2005, production Step 2 devices for LX and SX families will be rolled out in stages.

Starting on November 21, 2005, Xilinx can ship Virtex-4 LX and SX Step 2 devices against standard ordering part numbers since Step 2 devices are a functional superset of Step 1 devices.

Response

No response from the customer is required. Please contact Xilinx Technical Support if you have any questions.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/7/05	1.0	Initial release.
12/9/05	1.1	Corrected DCM clock stop time from "seconds" to "milliseconds" in the Description section, and added a sentence after Figure 1.