Data Sheet Pin-to-Pin Specification Change for the Virtex-5 Family

XCN07021 (v1.0) December 24, 2007

For Your Information

Overview

The purpose of this notification is to communicate a data sheet pin-to-pin specification change for the Virtex™-5 family.

Description

Pin-to-Pin Data Sheet change: For the Virtex-5 family, some pin-to-pin parameters have been changed to improve the accuracy of the generated timing report. A setup/hold and clock to out timing change has been implemented in ISE™ 9.2.04i in conjunction with Speed File v1.58 and the *Virtex-5 FPGA Data Sheet: DC and Switching Characteristics* Data Sheet (DS202 v3.7):

- Designs using PLLs to capture data should be re-timed using speed file v1.58 in conjunction with ISE 9.2.04i.
- XC5VSX95T-2 designs using DCM in System-Synchronous mode should be re-timed using speed file v1.58 in conjunction with ISE 9.2.04i.

Note: **If your design does not meet the above criteria, no action is required.**

DS202 v3.7 Tables	Change	Affected Devices	Details
Table 66	Global Clock Setup and Hold with DCM in System-Synchronous Mode	SX95T-2 setup	Only the SX95T-2 is changing by ~200 ps, consult DS202 v3.7 for specific values
Tables 68 and 61	Global Clock Setup and Hold (and Clock to Out) With PLL in System-Synchronous Mode	All devices and speed grades	Average change is +200 ps to setup, consult DS202 v3.7 for specific values
Tables 69 and 62	Global Clock Setup and Hold (and Clock to Out) With PLL in Source-Synchronous Mode	All devices and speed grades	There will be a minor optimization of the setup and hold times (less than 100 ps), consult DS202 v3.7 for specific values
Tables 70 and 63	Global Clock Setup and Hold (and Clock to Out) With DCM and PLL in System-Synchronous Mode	All devices and speed grades	Average change is +200 ps to setup, consult DS202 v3.7 for specific values
Tables 71 and 64	Global Clock Setup and Hold (and Clock to Out) With DCM and PLL in Source-Synchronous Mode	All devices and speed grades	Average change is +200 ps to setup, consult DS202 v3.7 for specific values

Key Dates and Ordering Information

This change is effective immediately starting from the release of ISE 9.2.04i in conjunction with Speed File v1.58 and the *Virtex-5 FPGA Data Sheet: DC and Switching Characteristics* Data Sheet (DS202 v3.7).

Products Affected

All Virtex-5 products, as noted in the table above, will be affected by this change. This change applies to the Commercial (C) and Industrial (I) temperature grades and all speed grades.

Traceability

Not applicable.

Response

No response is required by this notice. For additional information or questions, please contact Xilinx Technical Support.

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/24/07	1.0	Initial release.