Virtex-6 FPGA: Data Sheet, User Guides, and JTAG ID Updates

XCN11009 (v1.0) January 24, 2011 **Product Change Notice - For Your Information**

Overview

Thank you for designing with the Xilinx Virtex®-6 family of devices. The purpose of this notification is to inform Xilinx customers of changes to data sheets and user guides for the devices listed in Table 1. Changes were made to the product documentation to align with production silicon.

Table 1: **Production Devices Affected by This Customer Change Notice** (1,2)

Devices	XC6VLX75T	JTAG ID (Revision Code) 4 or later
	XC6VLX130T	JTAG ID (Revision Code) 4 or later
	XC6VLX195T	JTAG ID (Revision Code) 4 or later
	XC6VLX240T	JTAG ID (Revision Code) 4 or later
	XC6VLX365T	JTAG ID (Revision Code) 0 or later
	XC6VLX550T	JTAG ID (Revision Code) 0 or later
	XC6VLX760	JTAG ID (Revision Code) 2 or later
	XC6VSX315T	JTAG ID (Revision Code) 4 or later
	XC6VSX475T	JTAG ID (Revision Code) 4 or later
	XC6VCX75T	JTAG ID (Revision Code) 4 or later
	XC6VCX130T	JTAG ID (Revision Code) 2 or later
	XC6VCX195T	JTAG ID (Revision Code) 4 or later
	XC6VCX240T	JTAG ID (Revision Code) 2 or later
Packages	All	
Speed Grades	1, -2, -3 (3), and -1L (3)	
Temperature Grades	C and I	

Notes:

1. The JTAG ID revision will change for Virtex-6 LXT, SXT, and CXT FPGAs as part of ongoing production enhancements. All of the revisions listed are production released and meet all data sheet specifications.
2. The products affected include all standard part numbers and specification control document (SCD) versions of the standard part numbers.
3. -3 and -1L speed grades are not applicable to CXT devices.

Configuration

Configuration Switching Characteristics (-1L Devices Only)

Some of the configuration switching parameters for the -1L speed grade have changed. Table 2 contains the parameters that are affected, including the original parameters and their updated values.

The associated updates will be in the *Configuration Switching Characteristics* table in DS152, *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics:* http://www.xilinx.com/support/documentation/data_sheets/ds152.pdf.

Table 2: **Changes to the -1L Configuration Switching Parameters**

Symbol	Description	Original Spec(1) -1L Only	Updated Spec(2) -1L Only	Unit
TPOR	Power-on reset	55	60	ms, Max
FMCCK	CCLK frequency, serial modes	100	70	MHz, Max
FMCCKTOL	Master CCLK tolerance from nominal	55	60	%, Max
TMCCKL/TMCCKH	Master CCLK low/high duty cycle	45/55	40/60	%, Min/Max
TSMCSCCK	CSI_B setup for SelectMAP/ICAP	4.5	5.5	ns, Min
TSMWCCK	RDWR_B setup for SelectMAP/ICAP	13.5	16	ns, Min
FRBCCK	Readback CCLK frequency for SelectMAP/ICAP	100	60	MHz, Max
FTCK/FTCKB	TCK frequency for configuration/boundary-scan	66	33	MHz, Max

Notes:

1. Version v2.10 and earlier of DS152.
2. Version v2.11 and later of DS152.

The parameters were updated to match production data. Refer to Answer Record 38339 for additional information: http://www.xilinx.com/support/answers/38339.htm.

PROGRAM_B Pin

There were updates to the *Power-On Sequence Precautions* sections of UG360, *Virtex-6 FPGA Configuration User Guide:* http://www.xilinx.com/support/documentation/user_guides/ug360.pdf.

On prior families, the PROGRAM_B or the INIT_B pins can be held Low at power-up to delay configuration. With the Virtex-6 devices, the PROGRAM_B pin is edge sensitive as opposed to level sensitive. So, holding this pin Low at power-up will not continue to delay configuration. Refer to Answer Record 38134 for more information: http://www.xilinx.com/support/answers/38134.htm.

Mixed-Mode Clock Manager (MMCM)

Restriction of Frequency Range for Bandwidth = HIGH or OPTIMIZED (FPFDMIN)

There is a requirement for Virtex-6 FPGA designs using MMCMs with a CLKINPFD (input clock frequency at the Phase Frequency Detector, or F_{CLKIN} / D) less than or equal to 135 MHz, where the BANDWIDTH attribute must always be set to LOW. In ISE® Design Suite 12.3 and previous design tools, when BANDWIDTH = OPTIMIZED, the software defaults to HIGH and must be manually changed to LOW in these cases. The ISE Design Suite tools and affected IP are fixed in version 12.4 so when BANDWIDTH = OPTIMIZED, ISE software chooses the appropriate BANDWIDTH setting based in the input clock PERIOD constraint and D value. Refer to Answer Record 38132 for additional information: http://www.xilinx.com/support/answers/38132.htm.

The changes will appear in the *MMCM Specification* table of the following data sheets. The parameters that changed are F_{PFDMIN} and F_{INMAX}. See:

DS152, *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics:* http://www.xilinx.com/support/documentation/data_sheets/ds152.pdf.

DS153, *Virtex-6 CXT Family Data Sheet:* http://www.xilinx.com/support/documentation/data_sheets/ds153.pdf.

Restriction of Clock Divider Values (F_{INMAX})

In Virtex-6 FPGA designs with an MMCM input clock (F_{CLKIN}) greater than 315 MHz, DIVCLK_DIVIDE (input divider) values of 3 and 4 must not be used. Refer to Answer Record 38133 for more information and to access the recommended work-around; http://www.xilinx.com/support/answers/38133.htm.

The changes will appear in the *MMCM_ADV Primitive* section of the product user guide. See: UG362, *Virtex-6 FPGA Clocking Resources User Guide:* http://www.xilinx.com/support/documentation/user_guides/ug362.pdf.

GTX Transceivers

GTX Reset

There are updates to the *Functional Description, GTX TX Reset in Response to Completion of Configuration,* and *GTX TX Reset in Response to GTXTXRESET Pulse* sections of UG366, *Virtex-6 FPGA GTX Transceivers User Guide:* http://www.xilinx.com/support/documentation/user_guides/ug366.pdf based on the following GTX Transceiver Initialization for Proper TXOUTCLK Functionality information.

GTX Transceiver Initialization for Proper TXOUTCLK Functionality

Virtex-6 FPGA GTX Transceivers can experience errant behavior after FPGA device configuration, or after applying user TXPLL reset (if TX uses TXPLL) or RXPLL reset (if TX uses RXPLL). The results of this behavior are that the internal reset state machine does not complete, and TXRESETDONE does not assert—or that TXOUTCLK might be the incorrect frequency or flat lined. This commonly occurs when using TXOUTCLK to generate USRCLK and USRCLK2 with TXOUTCLK_CTRL = TXOUTCLKPCS, TXOUTCLKPMA_DIV1, or TXOUTCLKPMA_DIV2 and TXPLL_DIVSEL_OUT = 2 or 4. Refer to Answer Record 35681 for more information and to access the recommended work-around: http://www.xilinx.com/support/answers/35681.htm.

GTX Transceiver Delay Aligner

The GTX Transceiver Delay Aligner was one of the components that helped the USRCLK (TXUSRCLK or RXUSRCLK) remain phase aligned to the internal PMA clock when the TX Elastic Buffer or RX Elastic Buffer is bypassed. The GTX Transceiver Delay Aligner generated the TXOUTCLK on the transmitter and the RXRECCLK on the receiver.

When the Transmitter Delay Aligner is used, the TXOUTCLK under certain corner conditions outputs a short clock pulse that can cause transmit data errors. Similarly, when the Receiver Delay Aligner is used, the RXRECCLK under certain corner conditions outputs a short clock pulse that can cause receiver data errors. If these clocks are used by other logic in the FPGA, incorrect user logic behavior can result.

Refer to Answer Record 39430 for the corner conditions that trigger this behavior and the associated work-arounds: http://www.xilinx.com/support/answers/39430.htm. For systems that are field deployed, designers are encouraged to compare the conditions against the boundary conditions to determine the need for a field upgrade. All future systems must adhere to the work-arounds specified in Answer Record 39430.

Key Dates and Ordering Information

These changes are effective upon this PCN release.

Response

No response is required. For additional information or questions, please contact Xilinx Technical Support http://www.xilinx.com/support/techsup/tappinfo.htm.

Important Notice: Xilinx Customer Notifications (XCNs, XDNs, and Quality Alerts) can be delivered via e-mail alerts sent by the Support website (http://www.xilinx.com/support). Register today and personalize your "Documentation and Design Advisory Alerts" area to include Customer Notifications. Xilinx Support provides many benefits, including the ability to receive alerts for new and updated information about specific products as well as alerts for other publications such as data sheets, errata, application notes, etc. For information on how to sign up, refer to Answer Record 18683: http://www.xilinx.com/support/answers/18683.htm.

Additional Documentation

Virtex-6 FPGA Documentation:

http://www.xilinx.com/support/documentation/virtex-6.htm

Xilinx Answer Record Database:

http://www.xilinx.com/support/answers/

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
01/24/11	1.0	Initial release.

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