Virtex-4 and Virtex-5 FPGA UMC Wafer Fabrication Line Consolidation

XCN11030 (v1.0) December 5, 2011 **Product Change Notice**

Overview

The purpose of this notification is to inform Xilinx customers of the consolidation of Virtex®-4 and Virtex®-5 FPGA products at UMC Fab 12 in Tainan, Taiwan. Xilinx has qualified and maintained both Virtex-4 and Virtex-5 FPGA products at UMC Fab 12 in Tainan, Taiwan and Toshiba in Oita, Japan. This consolidation results in certain devices previously sole sourced in Toshiba to transfer to UMC.

Description

Since the introduction of Virtex-4 and Virtex-5 FPGA products, Xilinx has qualified both product families and has been shipping the majority of devices in each product family from both the UMC and Toshiba Fabs. As part of this consolidation effort, wafer fabrication for all Virtex-4 and Virtex-5 FPGA products at Toshiba in Oita, Japan will transfer to UMC Fab 12 in Tainan, Taiwan, on the schedule indicated below.

Xilinx has extensive performance and qualification data for Virtex-4 and Virtex-5 FPGA products at UMC and Toshiba supporting exceptional quality and reliability.

This consolidation results in adding the devices mentioned below to the UMC mask library to permit Xilinx to manufacture the transferred devices to the same quality and reliability specifications that apply to the entirety of the Virtex-4 and Virtex-5 FPGA product families. There is no change in form, fit, function, and reliability.

Products Affected

Affected part numbers are included in the Table 1 and Table 2:

Table 1: **Standard "XC" FPGA Product Changes**

Xilinx Product	Packages
XC4VLX15	SF(G)363, FF(G)668
XC4VLX25	SF(G)363, FF(G)668
XC4VLX40	FF(G)668, FF(G)1148
XC4VLX80	FF(G)1148
XC5VLX20T	FF(G)323
XC5VSX35T	FF(G)665
XC5VSX50T	FF(G)665, FF(G)1136
XC5VSX95T	FF(G)1136, DIE
XC5VSX240T	FF(G)1738

Table 2: **High-Rel "XQ" FPGA Product Changes**

Xilinx Product	Packages
XQ4VLX25	SF363, FF668, DIE
XQ4VLX40	FF668
XQ4VLX160	FF1148
XQ5VSX50T	EF665, DIE
XQ5VSX95T	EF1136
XQ5VSX240T	FF1738

Key Dates and Ordering Information

Qualification availability and cross ship dates for the affected devices are indicated in Table 3 below.

Table 3: **Product Cross-Ship Schedule**

Xilinx Product	Packages	Process Qualification	Mask Qualification	Cross-ship Date
XC4VLX15	SF(G)363, FF(G)668	Completed	January 2012	April 2012
XC4VLX25	SF(G)363, FF(G)668	Completed	January 2012	April 2012
XC4VLX40	FF(G)668, FF(G)1148	Completed	January 2012	April 2012
XC4VLX80	FF(G)1148	Completed	January 2012	April 2012
XC5VLX20T	FF(G)323	Completed	January 2012	April 2012
XC5VSX35T	FF(G)665	Completed	Completed	April 2012
XC5VSX50T	FF(G)665, FF(G)1136	Completed	Completed	April 2012
XC5VSX95T	FF(G)1136, DIE	Completed	Completed	April 2012
XC5VSX240T	FF(G)1738	Completed	Completed	April 2012
XQ4VLX25	SF363, FF668, DIE	Completed	January 2012	April 2012
XQ4VLX40	FF668	Completed	January 2012	April 2012
XQ4VLX160	FF1148	Completed	Completed	April 2012
XQ5VSX50T	EF665, DIE	Completed	Completed	April 2012
XQ5VSX95T	EF1136	Completed	Completed	April 2012
XQ5VSX240T	FF1738	Completed	Completed	April 2012

Qualification Data

Qualification data is available in our reliability monitor report UG116. Virtex-4 LX, Virtex-5 LX, and Virtex-5 SXT FPGA data is available today. Additional mask qualification for the Virtex-4 LX and Virtex-5 LX FPGA devices will be available in January, 2012.

Response

No response is required. For additional information or questions, please contact Xilinx Technical Support.

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Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/05/11	1.0	Initial release.

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