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Flash Wafer Fabrication Change and Gold (Au) to Copper (Cu) Transition for Spartan-3AN FPGA Devices

XTP343 (v1.7) October 3, 2016

FAQ: Implications of XCN14003

Summary

To ensure business continuity, Xilinx is announcing a change in wafer fabrication facility location and process technology (non-optical) shrink from 0.13um to 0.11um for the in-system flash memory used in the Spartan®-3AN FPGA devices. In addition, Xilinx is transitioning the wire bond packages from gold (Au) to copper (Cu) wires meeting industry trends.

Xilinx is transitioning the in-system flash memory for the Spartan-3AN FPGA devices from wafer fabrication facility X-FAB (0.13um process) to UMC (0.11um process). Xilinx is performing the qualification and characterization on the Spartan-3AN FPGA devices which include the in-system flash with 0.11um process. Form, fit, and function will not be affected with this change, except for the XC3S50AN-TQ(G)144and ancillary flash algorithm changes. The in-system flash in the XC3S50AN-TQ(G)144 device is changing from a 1 Mb density to a 2 Mb density. The optional extended device information (EDI) field increases from zero bytes to one byte and the maximum time for certain page erase operations is increasing for the in-system flash memory in the XC3S700AN-FG(G)484. Some programming implementations can be affected by the change to the number of EDI bytes and increases to the XC3S700AN-FG(G)484 page erase times. These ancillary programming algorithm changes are specified in the Xilinx Answer 59572.

To align with the current industry trends and Xilinx product line strategy, we will transition the Spartan-3AN FPGA family from gold (Au) to copper (Cu) wire. This change will not affect fit, form, function or MSL rating of the wire bond packages. Xilinx has successfully implemented Spartan®-3/-3E/-3A with copper wire since August 2011, please refer to XCN11002. For the Cu-wire assembly, only halogen free, EU-ROHS compliant package and green mold compound will be used. The package does not contain published REACH SvHC materials.

FAQs

Q: What's happening?

Xilinx is transitioning the in-system flash memory for the Spartan-3AN FPGA devices from wafer fabrication facility X-FAB (0.13um process) to UMC (0.11um process). To align with current industry trends and Xilinx product line strategy, we will transition the Spartan-3AN FPGA family from gold (Au) to copper (Cu) wire.

Q: Why is Xilinx making these changes?

This change is due to the in-system flash supplier transitioning the business to another supplier.
Note, the new supplier has been using UMC as their Fab Supplier. Xilinx has to ensure business continuity and enable high volume supply chain capabilities for Xilinx Spartan-3AN FPGA devices. The Gold to Copper change makes the devices EU-ROHS compliant, aligns with current industry trends, aligns with other Xilinx product families and is expected to extend product lifecycle which benefits both customers and Xilinx.

Q: What is the benefit to customers?

This change will maintain the supply chain (See previous question/answer). Transitioning the in-system flash memory for the Spartan-3AN FPGA devices from wafer fabrication facility X-FAB (0.13um process) to UMC

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(0.11um process) will enable Xilinx customers to benefit from unified process control, quality, and reliability, continuous improvements and product life cycle stability for Xilinx Spartan-3AN FPGA devices.

Q: Which products are affected?

This change affects all speed and temperature variations of the commercial (C) and industrial (I) grade Spartan-3AN FPGA devices and packages shown in Table 1. Automotive (XA) devices, Hi-Rel (XQ) devices, and parts affected by XCN13016 are not affected by this Product Change Notice.
The changes also apply to all Specification Control Devices (SCD) of these affected product families.

Table 1: **Spartan-3AN FPGA Family Products Affected**

Device	Package	Cut-Over Date	Date Code Identifier
XC3S50AN(2)	TQ(G)144	3-May-15(4)	1517
XC3S200AN	FT(G)256	23-Feb-15(4)	1509
XC3S400AN	FT(G)256	23-Feb-15(4)	1509
	FG(G)400	23-Feb-15(4)	1509
XC3S700AN	FG(G)484	02-Oct-16(4)	1641
XC3S1400AN(2)	FG(G)676	12-Jul-15(4)	1529

Notes:

1. Please refer to the Xilinx Answer 59572 for programming algorithm changes.
2. Certain parts under XC3S50AN and XC3S1400AN devices have been discontinued; please refer to XCN13016.
3. For inquiries about a specific part number, please refer to the XCN14003. Contact your customer operations representative or CQE representative for any additional questions.
4. All dates are subject to change based on customer demand and or usage.

Q: When will this change take effect?

Xilinx will start shipping Spartan-3AN FPGA devices with in-system flash memory from UMC (0.11um process) and copper wires; please refer to Table 1 for the cutover dates.

Q: Is gold to copper transition fully qualified?

Yes. Xilinx has also successfully implemented Spartan-3/-3E/-3A with copper wire since August 2011 (refer to XCN11002). Most customers should not be affected by this announcement. Form, fit, and function will not be affected with this change.

Q: What do customers have to do in response to this announcement?

Nothing - Xilinx has already qualified the Spartan-3AN FPGA devices with the new fab change and gold to copper change.
The only exceptions are for the ancillary programming algorithm changes that will be required for the XC3S50AN-TQ(G)144 devices. All XC3S50AN-TQ(G)144 programming solutions must be updated for compatibility with devices affected by this change, including device programmers, in-system programming files used during test, and Xilinx ISE iMPACT software. Details are specified in the Xilinx Answer 59572. For all other Spartan-3AN devices, the in-system flash from UMC (0.11um process) is backward compatible with the in-system flash from X-FAB (0.13um process).

Q: Are design changes required?

In most cases, design changes are not required for the Spartan-3AN devices. However, all Spartan-3AN FPGA designs must be reviewed for use of the SPI_ACCESS primitive that provides access from the FPGA logic to the

in-system flash. If the design uses the SPI_ACCESS primitive, then check the following details for potential affects on the FPGA design.

If an XC3S50AN-TQ(G)144 FPGA design uses the SPI_ACCESS primitive, then check whether the design reads and depends on a specific ISF memory size value in the Status Register or from the Device ID read. Designs that depend on a specific ISF memory size value must be updated for compatibility with the 1 Mb and 2 Mb ISF memory size value. See Table 3.

Table 2: **Information Read Command Extended Device Information Field**

In-System Flash Revision	Fourth Byte: EDI String Length (hex)	Fifth Byte Value (hex)
X-FAB	0x00	Not applicable
UMC	0x01	0x00

Table 3: **XC3S50AN-TQ(G)144 Memory Size Value Differences from the In-System Flash**

XC3S50AN-TQ(G)144	Manufacturer and Device ID Read Byte 2	Density Code in Status Register[5:2]
With 1 Mb in-system flash	22 (hex)	0011 (binary)
With 2 Mb in-system flash	23 (hex)	0101 (binary)

If an XC3S700AN-FG(G)484 FPGA designs uses the SPI_ACCESS primitive and if the design invokes any of the commands listed in Table 4, then the application can require an update to the allowed time for completion of the command.

Table 4: **In-System Flash Changes for the XC3S700AN-FG(G)484**

Symbol	In-System Flash Command Description	Old Max Time	New Max Time
T_{PE}	81h Page Erase, or 0x3D + 0x2A + 0x7F + 0xCF Sector Protection Register Erase	35 ms, Max	50 ms, Max
T_{PEP}	83h Buffer (1) to Page Program with Built-in Erase, or 86h Buffer (2) to Page Program with Built-in Erase	35 ms, Max	55 ms, Max

Otherwise, if any other affected Spartan-3AN FPGA design uses the SPI_ACCESS primitive, then check whether the design expects a value of zero for the number of optional, extended device information bytes, when performing an Information Read command.

Q: How will Xilinx support the XC3S50AN-TQ(G)144 in-system flash?

Xilinx tools and programming solutions will support only the first 1 Mb of the in-system flash in all XC3S50AN devices, regardless of whether the XC3S50AN device contains a 1 Mb flash or 2 Mb flash. Details of the difference between the 1 Mb and 2 Mb in-system flash will be documented in UG333**.**

Q: Will ordering part numbers change?

Devices will remain in the same packages, with the same functionality and performance. There should be NO change to the customer ordering part numbers.

Q: How long have these devices been in production?

The Spartan-3AN FPGA devices have been in production since 2006 and are being successfully used across multiple applications and market segments.

Q: Will any Spartan-3AN FPGA devices be discontinued?

Certain parts of the XC3S50AN and XC3S1400AN device families have been discontinued; please refer to XCN13016 for details. The parts affected by XCN13016 are not affected by this change.

Q: Is this the first time in-system flash memory products are being manufactured at UMC (0.11um process)?

No. Several large customers are already manufacturing their in-system flash memory products at UMC. Due to existing NDA, we are unable to specify the names.

Q: Has Xilinx qualified Copper (Cu) wire in other FPGA products in the past?

Xilinx has successfully implemented Spartan-3/-3E/-3A with copper wire since August 2011, and we are shipping in high volume production with high reliability. Please refer to XCN11002. For the Cu-wire assembly, only halogen free, EU-ROHS compliant package and green mold compound will be used, which are industry standard.

Q: How is Xilinx assuring this transition and product families at UMC?

Xilinx is conducting extensive qualification and characterization efforts to ensure that there will be no change in Form, Fit, Function, Technical Specifications, performance or quality for these devices.

Xilinx has conducted successful audits of the UMC 0.11um process. Xilinx expects the UMC 0.11um process to be fully qualified to produce the Spartan-3AN FPGA devices in full compliance with our strict quality, reliability and datasheet specifications.

Q: Can customers choose to receive Spartan-3AN FPGA devices from specific Fab locations?

No. After the Spartan-3AN FPGA devices affected by the XCN14003 are qualified and released to production, Xilinx reserves the right to cross-ship production Spartan-3AN FPGA devices with in-system flash memory from UMC (0.11um process) and copper wires or from X-FAB (0.13um process) and gold wires; as needed for optimal supply.

Xilinx is conducting extensive qualification and characterization efforts to ensure that there will be no change in Form, Fit, Function, Technical Specifications or quality for these devices.

Q: Are any other product lines affected?

No, only the Spartan-3AN FPGA devices in Table 1 are affected by this change. This change does not affect any other Xilinx product line or process technology.

Q: Is this change due to any issues at the current supplier X-FAB (0.13um process)?

No, the in-system flash memory was sold to new supplier; therefore, the current supplier's X-FAB (0.13um process) is being EOL.

This change ensures business continuity and enables high volume supply chain capabilities for Xilinx Spartan-3AN FPGA devices. This change also simplifies product logistics which benefits both customers and Xilinx.

Q: What is the status of this change?

Xilinx has completed verification and qualification of the Spartan-3AN FPGA devices in Table 1 affected by this change. Qualification data is available on request.

Q: When will the Spartan-3AN FPGA devices characterization and qualification data be made available?

The characterization and qualification is now available, contact your regional CQE for information.

Q: Is there any change in the test program for the affected devices as a result of this change?

No, the affected devices will use the same production test programs. The only exception is about the ancillary programming algorithm changes that will be required for the XC3S50AN-TQ(G)144 devices and are specified in the Xilinx Answer 59572.

Q. How can the changed product be identified?

There is no top marking or cutoff date code that differentiates amongst the following Spartan-3AN mixes:

- Spartan-3AN with current supplier & Gold wire
- Spartan-3AN with current supplier & Copper wire
- Spartan-3AN with new supplier & Copper wire

Q: How do I find out more?

Customer Operations: Contact your local customer operations representative
Technical & Quality: Contact your CQE representative
Procurement related questions: Contact your local customer operations representative

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
05/05/2014	1.0	Initial release.
05/26/2014	1.1	(Pg.1) Add XC3S700AN-FG(G)484 information to the “Summary” section. (Pg.3) Add new paragraph and table 3 for XC3S700AN-FG(G)484 In-System Flash Changes.
10/06/2014	1.2	Updated reference to Xilinx Answer 59572 for ancillary programming changes for all affected devices. The changes are covered on the Summary section, Table 1 notes and the entire section of the design changes required on page 2 and 3.
10/27/2014	1.3	Converted this FAQ from Xilinx Internal document designation to Xilinx Public document designation. (Pg. 2) Updated to add Operations’ target cutover dates and date codes on Table 1. (Pg.2 & Pg. 5) Deleted the sentence that stated September 1, 2014 cross ship date. The cross ship date is no longer applicable on the product affects. (Pg. 3) Reorganized the tables order for Table 2, Table 3 and Table 4.
02/24/2015	1.4	(Pg.2) Updated Table 1 to adjust the target cut over dates and date codes.
06/30/2015	1.5	(Pg.2) Updated Table 1 to adjust the target cut over dates and date codes.
01/08/2016	1.6	(Pg.2) Updated Table 1 to adjust the target cut over dates and date codes (XC3S700AN).
10/03/2016	1.7	(Pg.2) Updated Table 1 to adjust the target cut over dates and date codes (XC3S700AN).

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