Virtex-4 XC4VFX20, XC4VFX40, XC4VFX60, XC4VFX100, and XC4VFX140 Production Errata

EN070 (v1.8) May 14, 2008 **Errata Notification**

Introduction

Thank you for designing with the Xilinx Virtex™-4 family of devices. Although Xilinx has made every effort to ensure the highest possible quality, the devices in Table 1 are subject to the limitations described in the following errata.

Devices

These errata apply to the XC4VFX20, XC4VFX40, XC4VFX60, XC4VFX100, and XC4VFX140 devices, as shown in Table 1.

Table 1: **Devices Affected by These Errata**

Devices	Step 0[1]	Step 1
	JTAG ID (Revision Code)[2]	JTAG ID (Revision Code)[2]
XC4VFX20C	2	6
XC4VFX20I	NA	6
XC4VFX40C	NA	0
XC4VFX40I	NA	0
XC4VFX60C	2	8
XC4VFX60I	NA	8
XC4VFX100C	0	6
XC4VFX100I	NA	6
XC4VFX140C	NA	4
XC4VFX140I	NA	4
Packages	All	
Speed Grades	-10, -11, -12[3]	

Notes:

1. I-grade not available in Step 0.
2. The revision code is located in bits [31:28] of the JTAG ID Code register. See UG071: V*irtex-4 Configuration Guide* for more information.
3. -12 is only available in C-grade devices. The XC4VFX140C is available in the -10 and -11 speed grades; the XC4VFX140I is available only in the -10 speed grade.

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

FIFO16

The FIFO16 does not correctly generate the ALMOST EMPTY, EMPTY, ALMOST FULL, and FULL flags after the following sequence occurs:

1. Read or Write has reached the threshold value of ALMOST EMPTY OFFSET or ALMOST FULL OFFSET.
2. A single Read or Write operation is performed, followed by a simultaneous Read or Write operation, when active Read and Write clock edges are very close together.

Unexpected or corrupt data can occur as a result of the flag failures, even if the ALMOST EMPTY or ALMOST FULL flags are not being used.

This issue does not happen in FIFO16 applications where Read and Write never occur simultaneously. Workarounds (downloadable macros) are available for users who are performing simultaneous Read/Writes. Not all workarounds achieve data sheet performance. See UG070, *Virtex-4 User Guide*, FIFO16 Error Condition and Work-Arounds section, for details.

Processor Block

For processor block errata and operational guidelines, please refer to Xilinx answer record 20658.

RocketIO Multi-Gigabit Serial Transceivers

This section provides a detailed description of the Virtex-4 RocketIO™ transceiver issues known at the release time of this document.

8B/10B Encoding

Data received with the devices covered by this errata (Table 1) must be 8B/10B encoded when using the analog CDR mode.

Digital Receiver: Buffer Bypass Mode

Buffer Bypass Mode cannot be used in conjunction with the Digital Receiver. Due to this restriction, the Buffered Mode must be used with the Digital Receiver. The Digital Receiver attributes must be set as shown in Table 2 for Buffered Mode operation.

Table 2: **Digital Receiver Attributes**

Attribute	Buffered Mode Value
RX_BUFFER_USE	TRUE
RXCLK0_FORCE_PMACLK	TRUE
DIGRX_SYNC_MODE	FALSE

See the "Digital Receiver" section of UG076: *Virtex-4 RocketIO Multi-Gigabit Transceiver User Guide* for more details regarding these attributes.

CDM ESD Protection (applies to Step 0 devices only)

The CDM ESD for the RocketIO pins (TXN, TXP, RXN, RXP, AVCCAUXRX, GNDA, AVCCAUXTX, VTRX, VTTX, AVCCAUXMGT, MGTCLKP, and MGTCLKN) deviates from the product definition of 250V. The XC4VFX20 and XC4VFX60 devices meet a level of 150V. The XC4VFX100 device meets a level of 100V.

Xilinx recognizes the present level of RocketIO pin ESD is lower than Xilinx internal standards. Xilinx continues to evaluate ESD requirements for high-speed serial interconnects and is committed to providing best-in-class ESD.

Receiver and Transmitter PLL Voltage Controlled Oscillator (VCO) Operating Frequency

The minimum VCO operating frequency is 2480 MHz. The maximum VCO operating frequency is limited by the value of the output divider. Table 3 defines the valid VCO operating frequency ranges for each output divider value. VCO operating frequencies outside of these ranges are not supported.

Table 3: **Supported VCO Operating Frequency Ranges**

Output Divider [RX, TX]OUTDIV2SEL	VCO Frequency		Units
	Minimum	Maximum	
1	2480	5000	MHz
2	2480	4300	MHz
4	2480		MHz
8	2488(1)		MHz
16	Not Supported		—
32			

Notes:

1. When the output divider is equal to 8, the minimum VCO frequency is limited by the minimum data rate of 622 Mb/s.

The VCO operating frequency ranges have a direct impact on line rate. Receiver operation in analog CDR mode at line rates between 2.15 Gb/s–2.48 Gb/s and 4.3 Gb/s–4.96 Gb/s is not supported. Transmitter operation at line rates between 1.075 Gb/s–1.24 Gb/s, 2.15 Gb/s–2.48 Gb/s, and 4.3 Gb/s–4.96 Gb/s is not supported.

Figure 1 illustrates the supported data rates for the Transmitter (Tx), the Receiver in Digital CDR Mode (Rx DCDR), and the Receiver in Analog CDR Mode (Rx ACDR). See Figure 1.

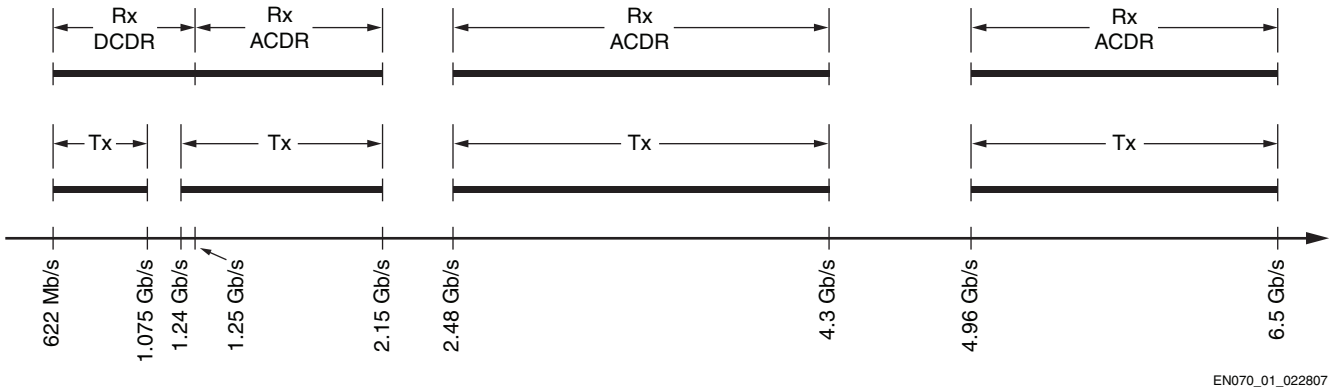

Figure 1: **Transmitter and Receiver Line Rates**

Transmitter PLL Feedback Divider Limitations

Lower PLL feedback divider values yield lower wide-band jitter generation than higher PLL feedback divider values. Table 4 lists the feedback divider / output divider combinations that are supported. DS302: *Virtex-4 Data Sheet: DC and Switching Characteristics* contains jitter generation specifications.

Table 4: **Supported Transmitter PLL Divider Combinations**

Line Rate (Mb/s)		Output Divider TXOUTDIV2SEL	Feedback Divider TXPLLNDIVSEL	VCO Frequency (MHz)	
Minimum	Maximum			Minimum	Maximum
4960	6500	1	8, 10	2480	3250
2480	4300	2	8, 10	2480	4300
3100	4300	2	16, 20	3100	4300
1240	2150	4	8, 10, 16, 20	2480	4300
622	1075	8	8, 10, 16, 20	2488	4300

Notes:

1. For lower wide-band jitter generation, choose a reference clock frequency that uses a lower feedback divider.
2. Line Rate = VCO Frequency*2/TXOUTDIV2SEL.
3. Reference Clock = VCO Frequency/TXPLLNDIVSEL

Receiver PLL Divider Limitations

Table 5 defines supported receiver PLL divider combinations.

Table 5: **Supported Receiver PLL Divider Combinations**

Receiver Mode	Line Rate (Mb/s)		Output Divider RXOUTDIV2SEL	Feedback Divider RXPLLNDIVSEL	VCO Frequency (MHz)	
	Minimum	Maximum			Minimum	Maximum
Analog CDR	4960	6500	1	8, 10	2480	3250
	2480	4300	2	8, 10	2480	4300
	3100	4300	2	16, 20	3100	4300
	1250	2150	4	8, 10, 16, 20	2500	4300
Digital CDR	622	1250	1	8, 10, 16, 20, 32, 40	2488	5000

Notes:

1. Line Rate (Analog CDR) = VCO Frequency*2/RXOUTDIV2SEL
2. Line Rate (Digital CDR) = VCO Frequency*2/8
3. Reference Clock = VCO Frequency/RXPLLNDIVSEL

Reference Clock

The MGTCLK input pins in the -10 devices covered by this errata (Table 1) have a maximum frequency of 400 MHz and a minimum peak-to-peak differential input voltage of 250 mV. No such restrictions exist for -11 and -12 devices.

The GREFCLK input port has a maximum frequency of 160 MHz (for all speed grades).

RXPCSHCLKOUT and TXPCSHCLKOUT Ports

The RXPCSHCLKOUT and TXPCSHCLKOUT MGT output clock ports are not supported in the devices covered by this errata (Table 1).

RXSIGDET – Receive Out-of-Band (Receive OOB) Signaling

The RXCDRLOS attribute does not function with the resolution and accuracy stated in UG076: *Virtex-4 RocketIO Multi-Gigabit Transceiver User Guide*. Refer to Xilinx application note XAPP732: *Inactive Transceiver Behavior Work-Arounds for Virtex-4 FX RocketIO MGTs* for further details.

SYNCLK1OUT and SYNCLK2OUT Ports

The GT11CLK output ports SYNCLK1OUT and SYNCLK2OUT to BUFG, PMCD, and DCM are supported in the devices covered by this errata (Table 1) as shown in Table 6:

Table 6: **SYNCLK1OUT and SYNCLK2OUT to BUFG, PMCD, and DCM**

Connection To	Maximum Frequency (MHz)	
	C-Grade	I-Grade
BUFG	375	312
DCM, PMCD	290	Not supported.

Static Operating Behavior

Static operating behavior is only a concern for transceivers that are expected to transmit or receive in the future. Transceivers that are never used require no action. To view detailed information on this topic, see XAPP732: *Inactive Transceiver Behavior Work-Arounds for Virtex-4 FX RocketIO MGTs.*

Applies to Step 0 Devices:
Under certain and specific conditions, transceivers might cease to correctly transmit or receive data when all three of the following conditions are met:

1. Power has been applied to the FPGA.
2. The FPGA is not configured. Or the FPGA is configured, but the transceiver is not instantiated.
3. Conditions (1) and (2) persist for more than 170 cumulative hours at 100°C T_J, 400 cumulative hours at 85°C T_J, or more than 2,000 cumulative hours at 60°C T_J.

   If conditions (1) and (2) occur simultaneously but intermittently with dynamic operation (the FPGA is configured, the transceiver is instantiated, and data transitions occur on the receiver), the time spent in a static state (unconfigured or uninstantiated) can be extended to 6,000 cumulative hours at 85°C T_J —15 times longer than the static hours listed in condition (3). In this case, the static usage must not exceed 5% of the duty cycle between dynamic and static operation, nor can it exceed 10 minutes in a single duration. If the MGT is in a static state for longer than 10 minutes in a single duration, the total allowed intermittent time is reduced proportionally to the 400 cumulative static hours at 85°C T_J.

Applies to Step 1 Devices:
Under certain and specific conditions, transceivers might cease to correctly transmit or receive data when all three of the following conditions are met:

1. Power has been applied to the FPGA.
2. The FPGA is not configured. Or the FPGA is configured, but the transceiver is not instantiated.
3. Conditions (1) and (2) persist for more than 1,100 cumulative hours at 100°C T_J, 2,500 cumulative hours at 85°C T_J, or more than 12,000 cumulative hours at 60°C T_J.

Applies only to Step 0 C-grade and Step 1 I-grade Devices:
Calibration Block v1.4.1 must be enabled when no data transitions occur on the receiver. See XAPP732: *Inactive Transceiver Behavior Work-Arounds for Virtex-4 FX RocketIO MGTs* for more information. No calibration block is required for Step 1 C-grade devices.

TXENOOB Port – Transmit Out-of-Band (Transmit OOB) Signaling (applies to Step 0 devices only)

The peak-to-peak amplitude of the differential output pins (TXP/TXN) can be higher than 65 mV when TXENOOB is asserted. Xilinx answer record 23481 discusses possible workarounds.

Operational Guidelines

Design Software Requirements

The devices covered by these errata, unless otherwise specified, require the speed specifications and Xilinx development software installations shown in Table 7.

Table 7: **Minimum Speed Specification and Xilinx ISE Software Version**

Speed Grade	Speed Specification	Xilinx ISE Version
-10	v1.58	8.1i Service Pack 2 (SP2)
-11	v1.62	8.2i Service Pack 3 (SP3)
-12	v1.65	9.2i Service Pack 1 (SP1)

Notes:

1. Speed Specification v1.65 or later must be used for XC4VFX40 and XC4VFX140 devices (all speed grades) and for XC4VFX100 (-12 speed grade only). In this case, these family members (and speed grades) are released to production before a speed specification has been released with the correct label (Advance, Preliminary, or Production). These labeling discrepancies will be corrected in a subsequent speed specification release.

- Contact the Xilinx technical support for ISE support. Updates are available on the following web page:

  http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

  The Stepping should be set to "0" or "1" in the constraint file (UCF file):

  CONFIG STEPPING = "0";

  or

  CONFIG STEPPING = "1";

  By using these values, the ISE software inserts a small macro to remove the DCM_INPUT_CLOCK_STOP requirement.
- A summary list of ISE software known issues pertaining to the Virtex-4 features is available at:

  http://support.xilinx.com/xlnx/xil_ans_display.jsp?iLanguageID=1&iCountryID=1&getPagePath=19713

Notes and Recommendations

Virtex-II and Virtex-II Pro FPGA Designers

The CCLK specification in Virtex-4 devices is LVCMOS 12 mA Fast slew rate. Xilinx recommends designing to this new standard.

Traceability

The XC4VFX60C is marked as shown in Figure 2. The other devices listed in Table 1 are marked similarly.

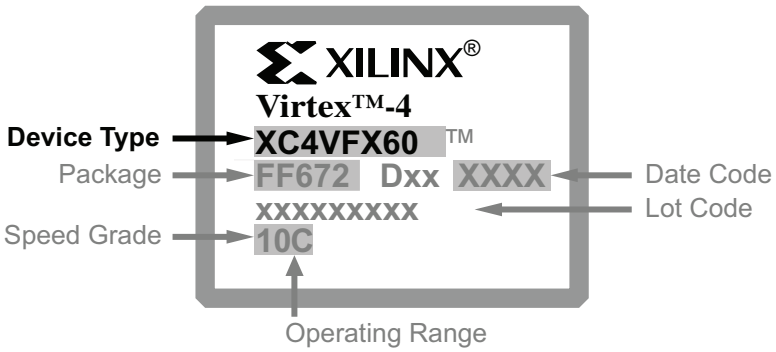

Figure 2: **Example XC4VFX60C Package Marking**

Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications.

For additional questions regarding these errata, please contact your Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Obtaining the Most Recent Errata Version

If this document is printed or saved locally in electronic form, check for the most recent release, available to registered users on the Xilinx website at: http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Errata.

To receive an e-mail alert when this document changes, sign up at: http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=18815.

These errata apply to the following Virtex-4 documents:

Virtex-4 Overview (http://www.xilinx.com/bvdocs/publications/ds112.pdf)

Virtex-4 Data Sheet (http://www.xilinx.com/bvdocs/publications/ds302.pdf)

Virtex-4 User Guide (http://www.xilinx.com/bvdocs/userguides/ug070.pdf)

XtremeDSP™ Design Guide (http://www.xilinx.com/bvdocs/userguides/ug073.pdf)

Virtex-4 Configuration Guide (http://www.xilinx.com/bvdocs/userguides/ug071.pdf)

Virtex-4 Packaging Guide (http://www.xilinx.com/bvdocs/userguides/ug075.pdf)

Virtex-4 RocketIO Multi-Gigabit Transceiver Guide (http://www.xilinx.com/bvdocs/userguides/ug076.pdf)

PowerPC™ 405 Processor Block Reference Guide (http://www.xilinx.com/bvdocs/userguides/ug018.pdf)

Revision History

Date	Version	Description
06/21/06	1.0	Initial Xilinx release.
10/06/06	1.1	Added -11 speed specification to Table 1. Updated Analog Receiver Range, Digital Receiver: Buffer Bypass Mode, and Reference Clock, sections. Removed Frequency Performance section. Updated the Speed Specification in the Design Software Requirements section.
12/20/06	1.2	Updated Processor Block, 8B/10B Encoding, CDR Operating Limitations, Digital Receiver: Buffer Bypass Mode, Reference Clock, Receiver and Transmitter PLL Voltage Controlled Oscillator (VCO) Operating Frequency, and the Design Software Requirements sections. Removed Analog Receiver Range; information added to the data sheet. Also removed the HBM ESD Protection and Static Operating Behavior sections.
04/27/07	1.3	Added Step 1 information to Table 1. Removed Attribute Settings section; information documented in UG076. Replaced Total Jitter Generation and CDR Operating Limitations sections with Receiver and Transmitter PLL Voltage Controlled Oscillator (VCO) Operating Frequency, Transmitter PLL Feedback Divider Limitations, and Receiver PLL Divider Limitations sections. Updated Reference Clock (added GREFCLK limitation).
06/11/07	1.4	Updated with Step 1 I-grade and -12 C-grade information: Table 1, CDM ESD Protection (applies to Step 0 devices only), Reference Clock, SYNCLK1OUT and SYNCLK2OUT Ports, Static Operating Behavior, TXENOOB Port – Transmit Out-of-Band (Transmit OOB) Signaling (applies to Step 0 devices only), and Design Software Requirements sections.
07/30/07	1.5	Updated Static Operating Behavior section.

Date	Version	Description
09/10/07	1.6	Added XC4VFX40 and XC4VFX100I devices. Updated the Design Software Requirements section.
10/01/07	1.7	Added XC4VFX140 devices.
05/14/08	1.8	Updated JTAG information in Table 1.

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