Spartan-6 FPGA LX150T CES Errata

EN124 (v1.3) June 28, 2010 **Errata Notification**

Introduction

Thank you for participating in the Spartan®-6 Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in Table 1. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the Spartan-6 devices shown in Table 1.

Table 1: **Devices Affected by These Errata**

Devices	JTAG ID (Revision Code)
XC6SLX150T-2FGG484CES	0
XC6SLX150T-3FGG484CES	0
XC6SLX150T-2FGG676CES	0
XC6SLX150T-3FGG676CES	0

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

Block RAM

Dual Port Block RAM Address Overlap in READ_FIRST and Simple Dual Port Mode

When using the block RAM in True Dual Port (TDP) READ_FIRST mode or Simple Dual Port (SDP) mode, with different clocks on ports A and B, the user must ensure certain addresses do not occur simultaneously on both ports when both ports are enabled and one port is being written to. Failure to observe this restriction can result in read and/or memory array corruption.

The description is found in the Conflict Avoidance section in v1.2 of UG383, *the Spartan-6 FPGA Block RAM Resources User Guide*.

This description was originally added to the *Spartan-6 FPGA Block RAM Resources User Guide*, v1.1, published 10/28/09. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. ISE® 12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in silicon.

Work-around

See Answer Record 34533.

9K Simple Dual Port Block RAM Width Restriction

The Spartan-6 FPGA RAMB8BWER in Simple Dual Port (SDP) mode (RAM_MODE=SDP) only supports the 36-bit data width on both ports. Failure to set both ports to 36 bits (DATA_WIDTH_A=36, DATA_WIDTH_B=36) can result in data corruption.

The description is found in the Possible Configurations section in v1.2 of UG383, *the Spartan-6 FPGA Block RAM Resources User Guide*.

This description was originally added to the *Spartan-6 FPGA Block RAM Resources User Guide*, v1.2, published 02/23/10. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. ISE 12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in silicon.

Work-around

See Answer Record 34541.

GTP Transceivers

JTAG Configuration

If using the iMPACT, ChipScope™, or System ACE™ tools, see Answer Record 33575.

JTAG configuration outside of the iMPACT or ChipScope tools is not supported when a GTP transceiver is used in the devices listed in Table 1.

Work-around

Instantiate the STARTUP_SPARTAN6 primitive. Connect a free-running clock from an FPGA pin to the CLK input port of the STARTUP_SPARTAN6 primitive. The clock must have a frequency between 50 MHz to 100 MHz. Select the bitstream generator option StartUpClk:UserClk. This work-around must only be used when configuring the FPGA via JTAG. See the Configuration Start-Up section.

Configuration Start-Up

The bitstream generator option StartUpClk:UserClk is not supported when a GTP transceiver is used in the devices listed in Table 1, except for the work-around noted in the JTAG Configuration section.

Work-around

Select the default bitstream generator option StartUpClk:CCLK.

CHAN_BOND_KEEP_ALIGN Attribute

The CHAN_BOND_KEEP_ALIGN attribute is not supported by the devices listed in Table 1. The CHAN_BOND_KEEP_ALIGN attribute must always be set to FALSE.

Transmitter Pre-Emphasis

GTP transmitter pre-emphasis (TXPREEMPHASIS[2:0] port) must be set to `3'b000` when transmitter amplitude (TXDIFFCTRL[3:0] port) is set to `4'b0111` or greater in the devices listed in Table 1.

Endpoint Block for PCI Express

Small TLPs and Packet Not Accepted DLLPs

For the devices listed in Table 1, if the endpoint block for PCIe® receives multiple Packet Not Accepted DLLPs (NAKs) while also having small TLPs in the queue, the transmitter can lock up.

CFGERRCPLRDYN Signal Inversion

In the devices listed in Table 1, the signal CFGERRCPLRDYN, which corresponds to cfg_err_cpl_rdy_n on the PCIe wrapper, is the wrong polarity. Designs that use this signal need to be modified for compatibility with non-ES devices.

Work-around

An inverter can be added in the wrapper to correct the polarity.

LCRC Errors on Received Power Management Message TLPs

For the devices listed in Table 1, the Endpoint block for PCI Express will not detect LCRC errors on downstream Power Management Message TLPs.

Packet Accepted DLLPs and Replay Timer Expiring

For the devices listed in Table 1, Packet Accepted DLLPs that are received at the same time the replay timer expires can cause the endpoint block for PCIe to indicate a fatal error.

Memory Controller Block (MCB)

MCB Performance

DS162, *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics* (v1.5) includes new data rate specifications for DDR2 and DDR3 interfaces implemented with the MCB. The new data rates are supported in the Standard MCB performance mode when operating within the standard V_{CCINT} recommended operating conditions. In addition, a new Extended MCB performance mode has been introduced with V_{CCINT} operating conditions that allow the MCB to operate at the originally specified performance.

Table 2: **MCB Performance Specification Comparison**

Performance Specification	V_{CCINT} Operating Range	DDR2 / DDR3 Performance	
		-2	-3
Original (No Longer Supported)	1.14V – 1.26V	667 Mb/s	800 Mb/s
New (Standard Performance)	1.14V – 1.26V	625 Mb/s	667 Mb/s
New (Extended Performance)	1.2V – 1.26V	667 Mb/s	800 Mb/s

This errata is being provided to highlight this change and ensure that all MCB users are aware of the new performance modes and specifications. The ISE 12.2 software (with MIG 3.5) will provide support for selection and timing validation of the new Standard and Extended MCB performance modes. Prior to the ISE 12.2 software release, these modes can be used by adhering to the correct V_{CCINT} range and ensuring that MIG tool selections are made in compliance with the new performance specifications.

Answer Record 35818 contains additional information.

MCB Calibration

In the devices listed in Table 1, for designs using Calibrated Input Termination, use the pin locations in Table 3 for the RZQ reference resistor.

Table 3: **Required RZQ Reference Resistor Pins**

Package	MCB Bank 1	MCB Bank 3	MCB Bank 4	MCB Bank 5
FGG484	Pin P19	Pin K7	N/A	N/A
FGG676	Pin U21	Pin M10	Pin M4	Pin M21

MCB and Suspend

In the devices listed in Table 1, the MCB does not support the self-refresh mode of the external memory during FPGA Suspend.

MCB Address Bus Hold Time

In the devices listed in Table 1, some bits of the MCB address bus (mcbx_dram_addr) can violate the input hold time (t_{IH}) specification of the memory device.

Work-around

See Answer Record 34089.

DCM Minimum Frequency

The Digital Clock Manager (DCM_SP or DCM_CLKGEN) minimum frequency does not meet the data sheet specifications in the devices listed in Table 1. The following specifications deviate from the data sheet:

- CLKIN_FREQ_DLL Min: 50 MHz
- CLKOUT_FREQ_CLK0 Min: 50 MHz
- CLKOUT_FREQ_CLK90 Min: 50 MHz
- CLKOUT_FREQ_2X Min: 100 MHz
- CLKOUT_FREQ_DV Min: 3.125 MHz
- CLKIN_FREQ_FX Min: 1.6 MHz
- CLKOUT_FREQ_FX Min: 50 MHz
- CLKOUT_FREQ_FXDV: 1.6 MHz

BUFPLL LOCK Output

In the devices listed in Table 1, the BUFPLL LOCK output might stay High when the PLL_BASE LOCKED signal is Low. As a result, the timing of the SERDESSTROBE signal might change after the PLL has been reset.

Work-around

Any application that performs a training, framing, or Bitslip function on the incoming data should be reinitialized following a PLL reset to ensure correct data reception.

Device DNA

Device DNA is not supported in the devices listed in Table 1. Do not use this feature.

Configuration Frequency for Block RAM Initialization

For the devices listed in Table 1, the configuration frequency must be limited to 10 MHz or less to guarantee that the block RAM will be initialized with the data in the configuration file.

Configuration Readback and Readback CRC

Readback is not supported in the devices listed in Table 1. Readback CRC for SEU detection (POST_CRC) is not supported in the devices listed in Table 1.

Encryption Security

In the devices listed in Table 1, encrypted FPGA designs using the eFUSE key as the decryption key will not be fully secure.

Work-around

Use battery-backed RAM for the decryption key.

Operational Guidelines

Design Software Requirements

The devices listed in Table 1, unless otherwise specified, requires the following Xilinx development software installation.

- Speed specification v1.01 (or later), Xilinx ISE® Design Suite 11.3 or later version of software.
- Upgrading to ISE 12.1 or later is recommended.

Operating Conditions Required when Using I/O Delay Variable Mode

In the devices listed in Table 1, when using I/O Delay Variable Mode, the operating conditions must be:

- V_{CCINT} = 1.20V to 1.26V
- Junction temperature (T_j) = 25°C to 85°C

The I/O delay variable mode (also known as I/O delay calibration and reset) is used when the IODELAY2 CAL or RST are used or when IODELAY2 IDELAY_TYPE attribute is set to VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX, or DIFF_PHASE_DETECTOR.

Notes and Recommendations

Charged Device Model ESD Protection

The Charged Device Model (CDM) ESD for the GTP transceiver pins MGTRREF and MGTAVTTRCAL deviates from the qualification acceptance criteria of 250V in the devices listed in Table 1. These pins meet a CDM ESD level of 100V.

Traceability

The XC6SLX150T is marked as shown in Figure 1. The other devices listed in Table 1 are similarly marked.

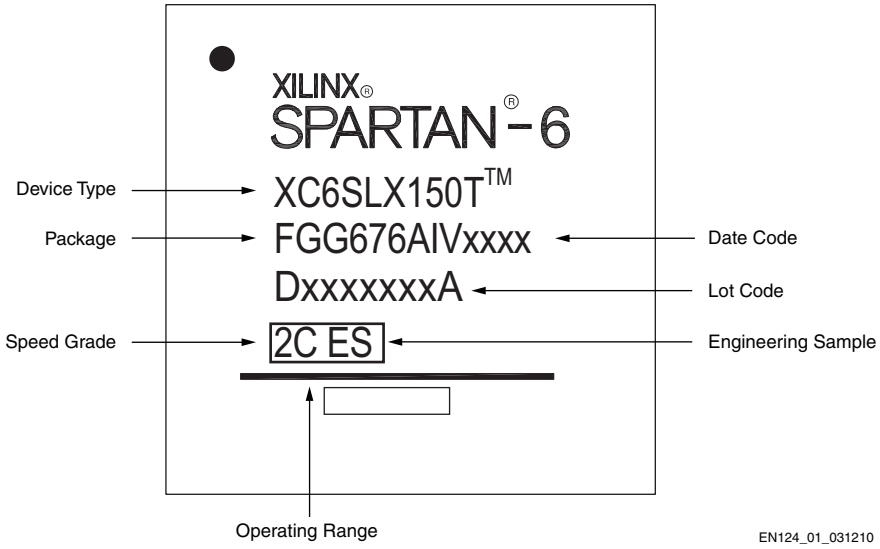

Figure 1: **XC6SLX150T-2FGG676CES Marking**

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
10/22/09	1.0	Initial Xilinx release.
03/22/10	1.1	Added MCB Address Bus Hold Time.
05/07/10	1.2	Added Dual Port Block RAM Address Overlap in READ_FIRST and Simple Dual Port Mode and 9K Simple Dual Port Block RAM Width Restriction sections.
06/28/10	1.3	Added MCB Performance. Updated Design Software Requirements.

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