

## Introduction

Thank you for designing with the XA Spartan®-6 FPGA Automotive family of devices. Although Xilinx has made every effort to ensure the highest possible quality, the devices in [Table 1](#) are subject to the limitations described in the following errata.

## Devices

These errata apply to the XA Spartan-6 devices shown in [Table 1](#).

*Table 1: Devices Affected by These Errata*

Devices	JTAG ID (Revision Code)
XA6SLX4	2 or higher
XA6SLX9	2 or higher
XA6SLX16	4 or higher
XA6SLX25	2 or higher
XA6SLX25T	2 or higher
XA6SLX45	4 or higher
XA6SLX45T	4 or higher
XA6SLX75	2 or higher
XA6SLX75T	2 or higher
XA6SLX100	2 or higher
Package	All
Speed Grades	All

## Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

## IODELAY2

In the devices listed in [Table 1](#), the IODELAY2 block can experience single data bit corruption. MCB interfaces are not affected by the IODELAY2 errata.

### Single Data Bit Corruption in IDELAY and ODELAY Modes

The IODELAY2 block can corrupt a single data bit for some IDELAY\_VALUE and ODELAY\_VALUE settings.

#### Work-arounds

**IDELAY\_TYPE=FIXED, VARIABLE\_FROM\_ZERO, VARIABLE\_FROM\_HALF\_MAX or DIFF\_PHASE\_DETECTOR, or when used in ODELAY mode**

Limit the data rate through the IODELAY2 to the maximum specifications in [Table 2](#).

Table 2: Maximum IODELAY2 Data Rate

V <sub>CCINT</sub> Range	Temperature	Maximum Data Rate (Mb/s) <sup>(1)</sup>	
		-3, -3Q	-2, -2Q
Standard Performance (Standard V <sub>CCINT</sub> )	Industrial, Q-Grade	740	625
Extended Performance (Requires Extended Performance V <sub>CCINT</sub> )		860	700

#### Notes:

- Higher data rates are achievable when certain system design restrictions or considerations are taken into account. See [Answer Record 41083](#) for additional information.

#### IDELAY\_TYPE=FIXED or VARIABLE\_FROM\_ZERO or when used in ODELAY mode, with tap limit

When using a fixed tap value and requiring higher performance than specified in [Table 2](#), restricting the maximum IDELAY\_VALUE or ODELAY\_VALUE can avoid data corruption at the higher indicated data rates. [Table 3](#) provides a summary of these higher data rates for fixed tap values.

Table 3: Maximum IDELAY\_VALUE or ODELAY\_VALUE

Maximum DELAY Value	Maximum Data Rate (Mb/s)	
	-3, -3Q	-2, -2Q
6	1,080	950
7	1,050	
8	1,000	
9	950	
14	800	800
18	See <a href="#">Table 2</a>	700
20	See <a href="#">Table 2</a>	667

## Operational Guidelines

### Design Software Requirements

The devices listed in [Table 1](#), unless otherwise specified, require the following Xilinx development software installation:

- Refer to the Spartan-6 Device Production Software and Speed Specification Release table in [DS162](#), *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics* for the Xilinx ISE® Design Suite version required for the selected part.
- See ISE 13 Software Known Issues with regards to Spartan-6 FPGAs in [Answer Record 40000](#).

### Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support:

<http://www.xilinx.com/support/clarexpress/websupport.htm> or your Xilinx Sales Representative:

<http://www.xilinx.com/company/contact.htm>.

## Revision History

Date	Version	Description
07/11/11	1.0	Initial Xilinx release.

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