Virtex-7 FPGA XC7VX690T CES, CES9925, and CES9910 Errata

EN227 (v1.2) April 26, 2013 **Errata Notification**

Introduction

Thank you for participating in the Virtex®-7 FPGAs Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in Table 1. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the devices shown in Table 1.

Table 1: **Devices Affected by These Errata**

Product Family	Device	JTAG ID (Revision Code)	Packages	Speed Grades	Junction Temperature
Virtex-7	XC7VX690T CES	2	All	-1, -2	0°C to 85°C
	XC7VX690T CES9925				0°C to 100°C
	XC7VX690T CES9910				–40°C to +100°C

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

GTH Transceivers

TX Interface Widths for 64B/66B or 64B/67B with GEARBOX_MODE[2] = 1'b1

When 64B/66B or 64B/67B Encoding with GEARBOX_MODE[2] = `1'b1` (CAUI Interface mode) is used, the 4-byte FPGA TX interface with 4-byte internal data width (TX_DATA_WIDTH = 32 and TX_INT_DATAWIDTH = 1) must be used.The 8-byte FPGA TX interface with 4-byte internal data width (TX_DATA_WIDTH = 64 and TX_INT_DATAWIDTH = 1) is not supported.

When 64B/66B or 64B/67B Encoding with GEARBOX_MODE[2] = `1'b1` (CAUI Interface mode) is used with 4-byte internal data width (RX_DATA_WIDTH = 64/32 and RX_INT_DATAWIDTH = 1), both the 8-byte and 4-byte FPGA RX interfaces are supported.

GTH Transceiver Power-On/Power-Off

While $V_{MGTAVCC}$ is powered within its recommended operating range and $V_{MGTAVTT}$ is below 0.7V, an additional 70 mA per transceiver is drawn from $V_{MGTAVCC}$.

Depending on the number of transceivers used, this extra current can be greater than the consumption reported in XPE.

Refer to Answer Record 47443 for more information.

GTH Transceiver Eye Scan

To use the GTH receiver eye scan, RX_DATA_WIDTH must be set to 16, 32, or 64.

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PCIe

Virtual Channel Capability

The Virtual Channel Capability is always enabled in Configuration Space when the Secondary PCI Express® Capability is enabled.

Virtual Channel TC/VC Map

The Virtual Channel Resource Control register TC/VC Map is incorrectly reset to `8'h01` instead of the PCIe Base Specification 3.0 value of `8'hFF`.

Loopback Exit

Reset of the LTSSM state machine is required to exit Loopback.Active state in loopback slave mode at Gen3 link speed.

Power Budgeting Capability

The Power Budgeting Capability is not supported.

Resizable BAR

The optional PCIe Resizable BAR (RBAR) capability is not supported through configuration. The RBAR feature can be initiated after the FPGA has been configured.

End-to-End CRC

When End-to-End CRC (ECRC) is used with multiple functions (PF0 and PF1 enabled), then ECRC must be enabled for either both functions or neither. It cannot be enabled independently on a per function basis. If only PF0 is used, then ECRC can be enabled or disabled as required.

TLP Processing Hints

The TLP Processing Hints (TPH) Completer is not supported.

D1 Power State

The D1 lower power device state is not supported.

Root Port

Root Port mode is not supported.

AER Header Log Overflow

For the Virtual Function Configuration Space, the optional AER Correctable Error Status register Header Log Overflow Status bit is not supported.

Function Level Reset

Function Level Reset (FLR) of SR-IOV Physical Functions is not supported. The ARI Capable Hierarchy bit in the Physical Function SR-IOV Control register is reset by a Function Level Reset of the Physical Function.

Requester reQuest (RQ) Sequence Number

The output ports pcie_rq_seq_num[3:0], pcie_rq_seq_num_vld in the Requester reQuest (RQ) interface and seq_num[3:0] inputs within the s_axis_rq_tuser bus are not supported. As a result, the optional method for transmit transaction ordering control is not supported.

Power

Static Power

All power supplies can exhibit up to 25% higher static current compared to the static current reported in XPE.

Design Tool Requirements

The devices listed in Table 1, unless otherwise specified, require the following Xilinx Design Tools:

- Speed specification v1.06 or v1.07 of Xilinx® ISE® Design Suite 14.3 or 14.4 or Vivado® Design Suite 2012.4, available at http://www.xilinx.com/support/download/.
- For GTH transceiver attribute updates, refer to Answer Record 51625.
- See Virtex-7 FPGA Answer Record 54906 for the most current known issues and work-arounds for Xilinx Design Tools.

Traceability

Figure 1 shows an example device top mark for the devices listed in Table 1.

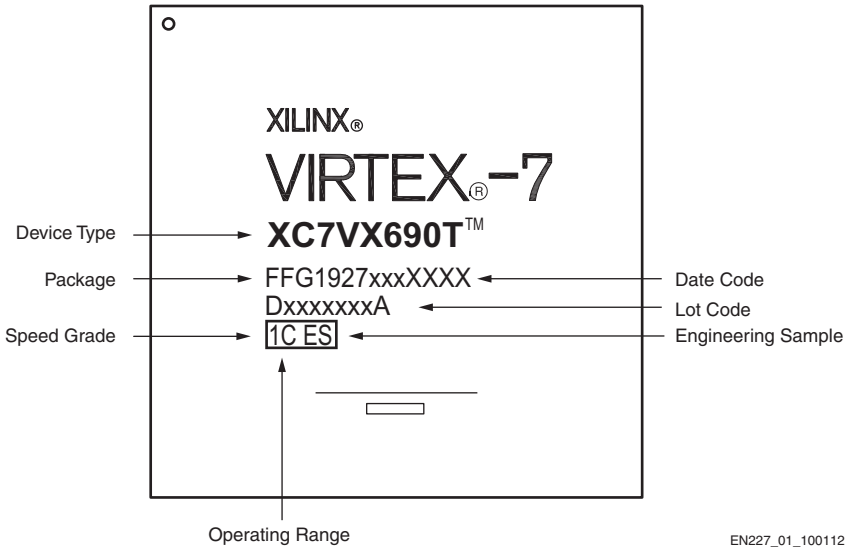

Figure 1: **Example Device Top Mark**

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact/index.htm.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
10/10/12	1.0	Initial Xilinx release.
10/16/12	1.1	Updated document to include XC7VX690T CES9925 and CES9910 Errata. Updated Table 1 and Design Tool Requirements. Added TX Interface Widths for 64B/66B or 64B/67B with GEARBOX_MODE[2] = 1'b1.
04/26/13	1.2	Updated Design Tool Requirements.

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