# ChipScope Pro ATC2 (v. 1.00a, 1.01a, 1.02a)

DS650 June 24, 2009 **Product Specification**

## Introduction

The Agilent Trace Core 2 (ATC2) is a customizable debug capture core that is specially designed to work with the latest generation logic analyzers from Agilent Technologies. The ATC2 core provides external Agilent logic analyzers access to internal FPGA design nets.

## Features

- Has up to 64 user-selectable banks
- Provides synchronous and asynchronous timing mode
- Has automatic pin mapping feature

For more information about the ATC2 core, refer to the *ChipScope Pro Software and Cores User Guide*.

| LogiCORE IP Facts | | | | |
|---|---|---|---|---|
| **Core Specifics** | | | | |
| Supported Device Family(1) | Spartan®-3, Spartan-3E, Spartan-3A, Spartan-3A DSP, Spartan-6, Virtex®-4, Virtex-5, Virtex-6 | | | |
| Resources Used(2) | I/O | LUTs | FFs | Block RAMs |
| | 8 | 122 | 185 | 0 |
| Special Features | N/A | | | |
| **Provided with Core** | | | | |
| Documentation | Product Specification | | | |
| Design File Formats | N/A | | | |
| Constraints File | N/A | | | |
| Verification | N/A | | | |
| Instantiation Template | Verilog and VHDL Wrapper | | | |
| Reference Designs /Application Notes | None | | | |
| Additional Items | Signal Description File (.cdc) | | | |
| **Design Tool Requirements** | | | | |
| Xilinx Implementation Tools | ISE® 11.2 | | | |
| Verification | ChipScope™ Pro 11.2 | | | |
| Simulation | Not supported in simulation | | | |
| Synthesis | Netlist is pre-synthesized by XST | | | |
| **Support** | | | | |
| Provided by Xilinx, Inc. | | | | |

1. Including the variants of these FPGA device families.
2. These estimates assume Virtex-4 device family with one 8-bit wide bank.

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## Applications

The ATC2 core is designed to be used in any application that requires verification or debugging using the ChipScope Pro software and an external Agilent Logic Analyzer.

## Functional Description

Communication with the ATC2 core is conducted using a connection to the JTAG port via the ICON core, as shown in the following figure.

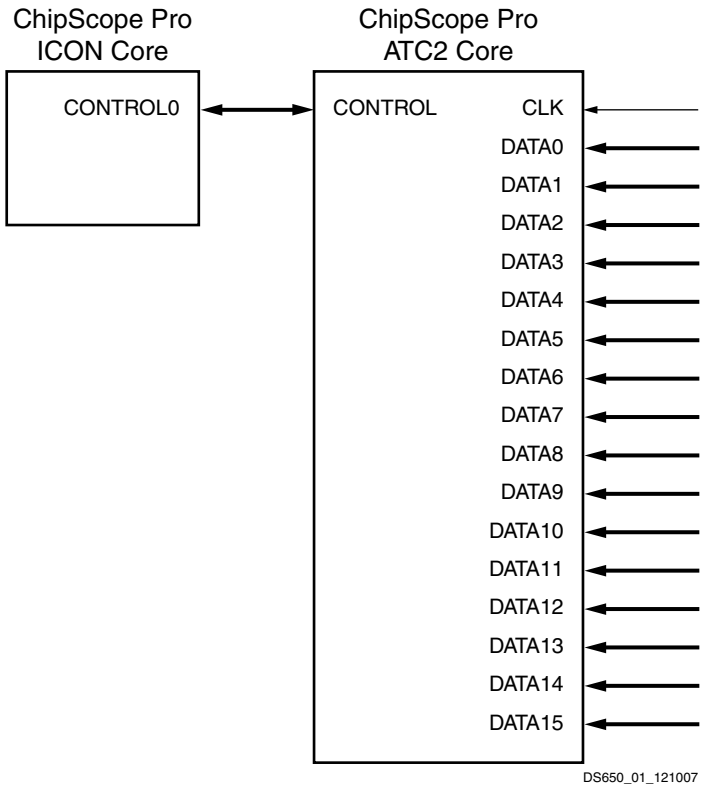


*Figure 1:* **ATC2 Core Connection to ICON Core**

The data path of the ATC2 core consists of:

- Up to 64 run-time selectable input signal banks that connect to the user's FPGA design.
- Up to 128 output data pins that connect to an Agilent logic analyzer's probe connectors.
- Optional 2x time-division multiplexing (TDM) available on each output data pin that can be used to double the width of each individual signal bank from 128 to 256 bits.
- Supports both asynchronous timing and synchronous state capture modes.
- Supports any valid I/O standard, drive strength, and output slew rate on each output data pin on an individual pin-by-pin basis.
- Supports any Agilent Technologies probe connection technology. For more information, refer to http://www.agilent.com/find/softtouch.

The maximum number of data probe points available at run time is calculated as:

(64 data ports) * (128 bits per data port) * (2x TDM) = 16,384 probe points.

### ATC2 Core Data Capture and Run-Time Control

The external Agilent logic analyzer is used to trigger on and capture the data that passes through the ATC2 core. This allows you to take full advantage of the complex triggering, deep trace memory, and system-level data correlation features of the Agilent logic analyzer. It provides increased visibility of internal design nodes provided by the ATC2 core. It is also used to control the run-time selection of the active data port by communicating with the ATC2 core via a JTAG port connection.

## ATC2 Interface Ports

The I/O signals of the ATC2 core consist of the control bus to ICON, a clock signal, and the signal banks, as displayed in the following table.

*Table 1:* **ATC2 Interface Ports**

| Port Name | Direction | Description |
|---|---|---|
| CLK | IN | Design clock needed to synchronize the data in state mode. Optional (depends on state_synchronous parameter). |
| CONTROL[35:0] | INOUT | Control bus to ICON core. Mandatory. |
| DATA<*n*>[<*m*>-1:0] | IN | Data signal input bank number <*n*> of width <*m*>. Optional, except for <*n*> = 0, which is mandatory (depends on parameter signal_bank_count = <*n*>+1, where <*n*> ranges from 0 through 63). |

## ATC2 XCO Parameters

The following table displays the ATC2 XCO parameters.

*Table 2:* **ATC2 XCO Parameters**

| Parameter Name | Allowable Values | Default Value | Description |
|---|---|---|---|
| atck_drive | N/A(1) | N/A(1) | Drive strength for ATCK pin. |
| atck_io_standard | N/A(1) | N/A(1) | IO standard for ATCK pin. |
| atck_pin_loc | any alphanumeric | none | Pin location for ATCK pin. |
| atck_slew_rate | fast, slow | fast | slew rate for ATCK pin. |
| atd_drivers | same_as_atck, different_than_atck | same_as_atck | Whether to use atck settings for all data pins (same_as_atck) or individual settings for data pins (different_than_atck) |
| atd_pin_count | 4-64 | 8 | Number of data pins to use. |
| atd<*n*>_drive | N/A(1) | N/A(1) | Drive strength for data pin <*n*>. |
| atd<*n*>_io_standard | N/A(1) | N/A(1) | IO standard for data pin <*n*>. |
| atd<*n*>_pin_loc | any alphanumberic | none | Pin location for data pin <*n*>. |
| atd<*n*>_slew_rate | fast, slow | fast | slew rate for data pin <*n*>. |
| component_name | String with A-z, 0-9, and _ (underscore) | vio | Name of component instance. |
| driver_endpoint_type | single-ended, differential | single-ended | Type of output driver to use. Applies to all pins. |
| enable_always_on_mode | true, false | false | Enables measurement immediately after FPGA configuration. |
| enable_auto_setup | true, false | true | Include ciruitry that will use a test pattern to properly aiign the data. |

*Table 2:* **ATC2 XCO Parameters *(Cont'd)***

| Parameter Name | Allowable Values | Default Value | Description |
|---|---|---|---|
| max_frequency_range | 0-100_mhz, 101-200_mhz, 201-300_mhz, 301-500_mhz | 0-100_mhz | Sets the core operating range. This is used in generating the core and during instrument setup. |
| signal_bank_count | 1, 2, 4, 8, 16, 32, 64 | 1 | Number of signal banks. |
| tdm_rate | 1x, 2x | 1x | Time Division Multiplexing rate, either 1x at design speed or 2x multiplexing. |

1. The I/O standards available will be different depending on the selected FPGA device family. Refer to the datasheet of the appropriate FPGA device family for details. Also, different drive strength selections are available based on the selected I/O standard.

## Restrictions

A maximum of 15 ATC2 cores can be used in a single design.

# Using ATC2 Core in EDK

The ATC2 core can be inserted into an embedded processor design using the Xilinx® Embedded Development Kit (EDK). In this case, the ATC2 core depends on ICON and OPB_MDM component instances already being in the design, as shown in the following figure.

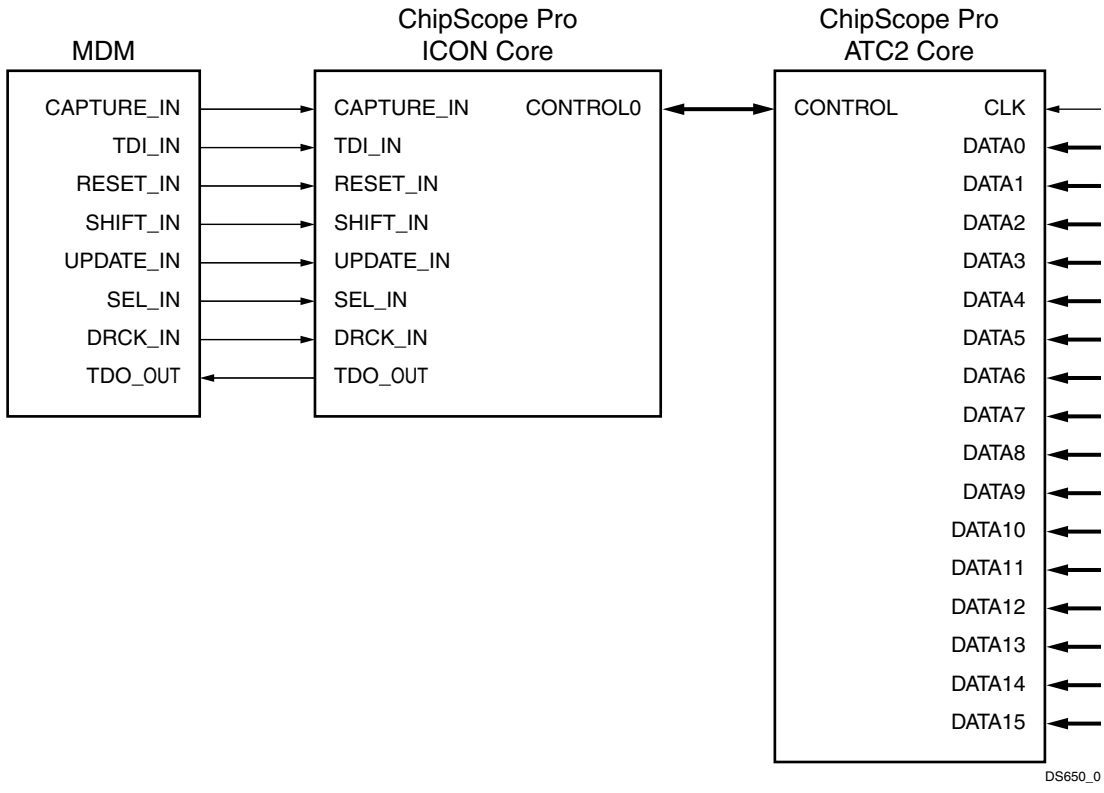


*Figure 2:* **ATC2 Core Component in EDK Design**

In EDK, the ATC2 core is integrated into the tool using a Tcl script. When the EDK Platgen tool is run, the Tcl script is called and the script internally calls CORE Generator in command line mode. The Tcl script provides CORE Generator an arguments file (.xco) to generate the ATC2 core netlist. The Tcl script also generates an HDL wrapper to match the ATC2 ports based on the core parameters.

The XST synthesis tool is used for synthesizing the wrapper HDL generated for the ATC2 core. The NGC netlist outputs from XST and ChipScope Pro Core Generator are subsequently incorporated into the Xilinx ISE tool suite for actual device implementation.

## Verification

Xilinx has verified the ATC2 core in a proprietary test environment, using an internally developed bus functional model.

## References

[1] More information on the ChipScope Pro software and cores is available in the *Software and Cores User Guide*, located at http://www.xilinx.com/literature/literature-chipscope.htm.

[2] Information about hardware debugging using ChipScope Pro in EDK is available in the Platform Studio 11.2 online help, located at
http://toolbox.xilinx.com/docsan/xilinx11/help/platform_studio/platform_studio.htm.

[3] Information about hardware debugging using ChipScope Pro in System Generator for DSP is available in the *Xilinx System Generator for DSP User Guide*, located at
http://www.xilinx.com/support/sw_manuals/sysgen_ug.pdf.

## Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

## Ordering Information

The ATC2 core is provided under the SignOnce IP Site License and can be generated using the Xilinx CORE Generator system 11.2 or higher. The CORE Generator system is shipped with Xilinx ISE Foundation Series Development software.

## Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|---|---|---|
| 03/24/2008 | 1.0 | Release 10.1 (Initial Xilinx release). |
| 04/25/2008 | 1.1 | Release 10.1, Service Pack 1 changes. |
| 09/19/2008 | 1.2 | Release 10.1, Service Pack 3 changes. |
| 04/07/2009 | 2.0 | Release 11.1 |
| 06/24/2009 | 2.1 | Release 11.2 |

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