LogiCORE IP AXI 10-Gigabit Ethernet v1.2

Product Guide

Vivado Design Suite

PG157 April 2, 2014

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Introduction

This document provides the design specification and other design information for the LogiCORE™ IP AXI 10-Gigabit Ethernet core. This core integrates a 10-Gigabit Ethernet MAC and a 10-Gigabit Ethernet PCS/PMA in 10GBASE-R mode to provide an IEEE1588-compatible 10-Gigabit Ethernet port.

The transmit and receive data interfaces use AXI4-Stream interfaces. This core proves a control interface to internal registers using an AXI4-Lite interface. This AXI4-Lite slave interface supports single beat read and write data transfers (no bursts).

Features

- Supports high accuracy IEEE1588 1-step and 2-step timestamping on a 10GBASE-R network interface.
- System timer resynchronization into timestamping clock domains.

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1) (2)	Zynq®-7000, Virtex®-7, Kintex®-7
Supported User Interfaces	AXI4-Lite, AXI4-Stream
Resources	See Table 2-2
Provided with Core	
Design Files	Encrypted RTL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	Not Provided
Supported S/W Driver	N/A
Tested Design Flows(3)	
Design Entry	Vivado® Design Suite IP Integrator
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. For the listed families, only a -2 speed grade or faster is supported.
3. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The AXI 10-Gigabit Ethernet core can be added only to a Vivado® IP Integrator block design in the Vivado Design Suite. The AXI 10-Gigabit Ethernet core is a hierarchical design block diagram that contains multiple LogiCORE™ IP instances (infrastructure cores). The cores are configured and connected during the system design session.

The helper cores for this IP are:

- Xilinx LogiCORE IP 10-Gigabit Ethernet MAC (XGMAC)
- Xilinx LogiCORE 10-Gigabit Ethernet PCS/PMA

The AXI 10-Gigabit Ethernet core integrates these two cores and adds a high accuracy timestamping capability compatible with IEEE1588-2008 (also known as IEEE1588v2). For detailed specifications, see Chapter 2, Product Specification. See the change log in the IP customization GUI for the core versions used in this design. All core documents can be downloaded from the Xilinx Support website; see References.

Feature Summary

The core supports the following features:

- IEEE1588-compatible hardware timestamping at full 10 Gb Ethernet line rate on both transmit and receive paths. Timestamp accuracy is better than ± 10 ns under all operating conditions.
- IEEE1588 hardware timestamping for a 1-step and 2-step operation on 10GBASE-R network interfaces using 7-Series GTXE2 and GTHE2 transceivers.
- The system timer provided to the core and the consequential timestamping taken from it are available in one of two formats which are selected during IP core generation.
    - Time-of-Day (ToD) format: IEEE1588-2008 format consisting of an unsigned 48-bit second field and a 32-bit nanosecond field.
    - Correction Field format: IEEE1588-2008 numerical format consisting of a 64-bit signed field representing nanoseconds multiplied by 2^{16} (see IEEE1588 clause 13.3.2.7). This timer should count from 0 through the full range up to 2^{64} -1 before wrapping around.

- In-band and out-of-band control of timestamp behavior.
- In-band and out-of-band reporting of receive-side timestamps.
- Supports all underlying 10-Gigabit Ethernet MAC features except those listed in Unsupported Features.
- Supports all underlying 10-Gigabit Ethernet PCS/PMA features except those listed in Unsupported Features.

Unsupported Features

The following features are not supported in this release of the core.

- Transceiver types other than 7 Series GTXE2 and GTHE2 transceivers.
- 10-Gigabit Ethernet PHY types other than 10GBASE-R.
- Unsupported 10-Gigabit Ethernet MAC features:
  - WAN mode.
  - Configuration/Status vector.
  - Transmit-side in-band FCS passing for 1-step timestamped frames.
- Unsupported 10-Gigabit Ethernet PCS/PMA feature:
  - 10GBASE-KR functionality, including training, autonegotation, and FEC.
  - Shared logic in example design
  - Transceiver debug signals

Licensing and Ordering Information

License Checkers

If the IP requires a license key, the key must be verified. The Vivado design tools have several license check points for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- `write_bitstream` (Tcl command)

IMPORTANT: *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

License Type

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx® Vivado Design Suite under the terms of the Xilinx End User License. However, to use the AXI 10-Gigabit Ethernet core, a 10-Gigabit Ethernet MAC license must be purchased.

IMPORTANT: *For full access to all core functionalities in simulation and in hardware, you must purchase a 10-Gigabit Ethernet MAC license.*

For more information, visit the AXI 10-Gigabit Ethernet core product page.

More details related to the licensing of the 10-Gigabit Ethernet MAC can be found in the *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072) [Ref 1].

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

A high-level block diagram of the AXI 10-Gigabit Ethernet core is shown in Figure 2-1.

The AXI4-Stream 64-bit buses are provided for moving transmit and receive Ethernet data to and from the AXI 10-Gigabit Ethernet core. The AXI 10-Gigabit Ethernet core also provides an AXI4-Lite bus interface for a straightforward connection to a processor core for register access.

Other AXI4-Stream interfaces are provided to report IEEE1588 timestamp information to the controlling logic.

The AXI 10-Gigabit Ethernet core builds on the existing functionality of the following cores:

- **10-Gigabit Ethernet MAC core**: This core is described in the *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072) [Ref 1].
- **10-Gigabit Ethernet PCS/PMA core**: This core is described in the *LogiCORE IP 10-Gigabit Ethernet PCS/PMA Product Guide* (PG068) [Ref 2].
- **Timer Synchronization core (Timer Sync)**: This core synchronizes the timer in the selected format from the system clock domain into the core clock domain.

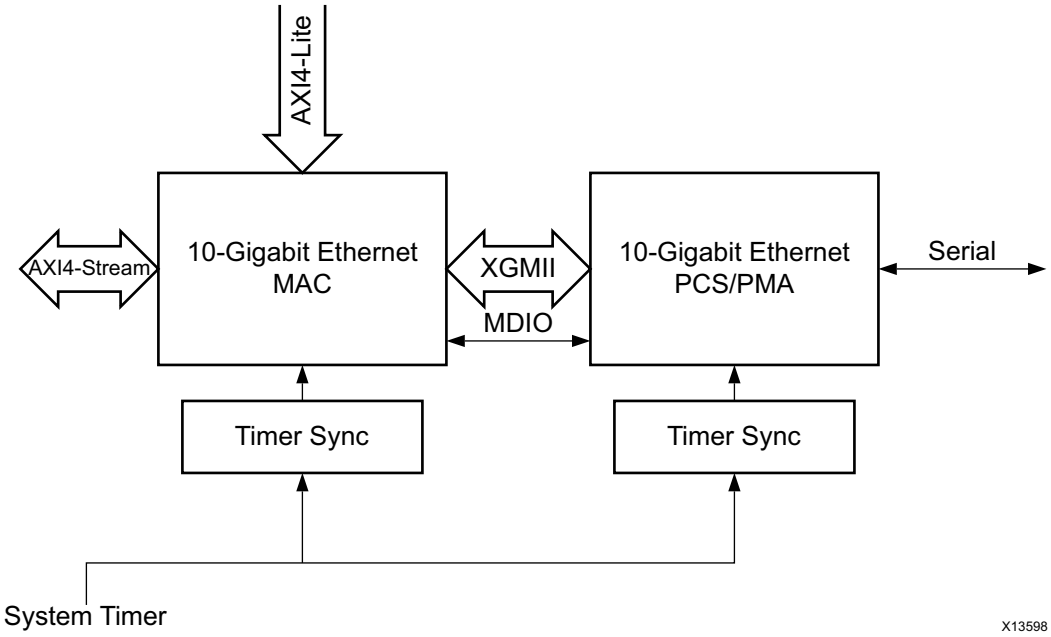

Figure 2-1: **AXI 10-Gigabit Ethernet High-Level Block Diagram**

See the *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072) [Ref 1] for instructions about using the AXI4-Stream interfaces for the datapath, and the AXI4-Lite interface for configuration and status of the 10-Gigabit Ethernet core. Only the additional ports and functionality specific to IEEE1588 timestamp operation are described in this guide.

Transmit

Figure 2-2 shows the transmit side of the AXI 10-Gigabit Ethernet core.

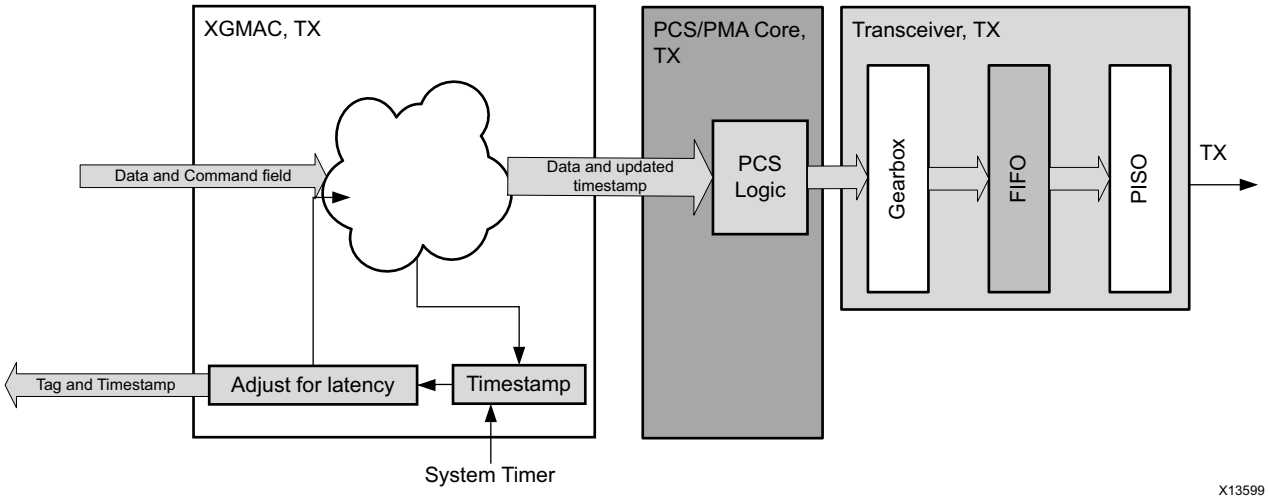

Figure 2-2: **Transmit-Side Architecture**

On transmit, a command field is provided by the client to the core, either in-line with the frame sent for transmission, or out-of-band in parallel with the frame sent for transmission. This indicates, on a frame-by-frame basis, the 1588 function to perform (either no-operation, 1-step, or 2-step) and also indicates, for 1-step frames, whether there is a UDP checksum field to update.

If using the ToD format, then for both 1-step and 2-step operation, the full captured 80-bit ToD timestamp is returned to the client logic using the additional ports defined in Table 2-5. If using the Correction Field format, then for both 1-step and 2-step operation, the full captured 64-bit timestamp is returned to the client logic using the additional ports defined in Table 2-5 (with the upper bits of data set to zero as defined in the table).

If using the ToD format, then for 1-step operation, the full captured 80-bit ToD timestamp is inserted into the frame. If using the Correction Field format, then for 1-step operation, the captured 64-bit timestamp is summed with the existing Correction Field contained within the frame and the summed result is overwritten into the original Correction Field of the frame. Supported frame types for 1-step timestamping are:

- Raw Ethernet
- UDP/IPv4
- UDP/IPv6

For 1-step UDP frame types, the UDP checksum is updated in accordance with IETF RFC 1624.

For all 1-step frames, the Ethernet Frame Check Sequence (FCS) field is calculated after all frame modifications have been completed.

For 2-step transmit operation, all Precision Time Protocol (PTP) frame types are supported.

Frame-by-Frame Timestamping Operation

The Ethernet frame sent to the MAC contains a command field. The format of the command field is defined in the following list. The information contained within the command field indicates one of the following on a frame-by-frame basis.

- No operation: the frame is not a PTP frame and no timestamp action should be taken.
- 2-step operation is required and a tag value (user-sequence ID) is provided as part of the command field; the frame should be timestamped, and the timestamp made available to the client logic, along with the provided tag value for the frame. The additional MAC transmitter ports (defined in Table 2-4) provide this function.
- 1-step operation is required
  - For the ToD timer and timestamp format a timestamp offset value is provided as part of the command field; the frame should be timestamped, and the timestamp should be inserted into the frame at the provided offset (number of bytes) into the frame.
  - For the Correction Field format, a Correction Field offset value is provided as part of the command field; the frame should be timestamped, and the captured 64-bit Timestamp is summed with the existing Correction Field contained within the frame and the summed result is overwritten into original Correction Field of the frame.

  For 1-step operation, following the frame modification, the CRC value of the frame should also be updated/recalculated. For UDP IPv4 and IPv6 PTP formatted frames, the checksum value in the header of the frame needs to updated/recalculated.
- For 1-step UDP frame types, the UDP checksum is updated in accordance with IETF RFC 1624.
  - If using the ToD format, in order for this update function to work correctly, the original checksum value for the frame sent for transmission should be calculated using a zero value for the timestamp data. This particular restriction does not apply when using the Correction Field format.
  - If using the Correction Field format then a different restriction does apply: the separation between the UDP Checksum field and the Correction Field within the 1588 PTP frame header is a fixed interval of bytes, supporting the 1588 PTP frame definition. This is a requirement to minimize the latency through the MAC since both the checksum and the correction field must both be fully contained in the MAC pipeline in order for the checksum to be correctly updated. This particular restriction does not apply to the ToD format since the original timestamp data is calculated as a zero value; consequently the checksum and timestamp position can be independently located within the frame.

Table 2-1 provides a definition of the command field.

Table 2-1: **Ethernet Frame Command Field Description**

Bits	Name	Description
[1:0]	1588 operation	2'b00 – No operation: no timestamp is taken and the frame is not modified. 2'b01 – 1-step: a timestamp should be taken and the frame will be modified accordingly. 2'b10 – 2-step: a timestamp should be taken and returned to the client using the additional ports of Table 2-5. The frame itself is not modified. 2'b11 – Reserved: acts as No operation.
[7:2]	Reserved	Reserved for future use. Values are ignored by the 10-Gigabit Ethernet MAC core.
[8]	Update Checksum	The usage of this field is dependent on the 1588 operation For No operation or 2-step, this bit is ignored. For 1-step: 1'b0: the PTP frame does not contain a UDP checksum. 1'b1: the PTP frame contains a UDP checksum which the core is required to recalculate.
[15:9]	Reserved	Reserved for future use. Values is ignored by the 10-Gigabit Ethernet MAC cores.
[31:16]	Tag Field	The usage of this field is dependent on the 1588 operation. For No operation or 1-step, this field is ignored. For 2-step, this field is a tag field. This tag value is returned to the client with the timestamp for the current frame using the additional ports of Table 2-5. This tag value can be used by the software to ensure that the timestamp can be matched with the 2-step frame that it sent for transmission.

Table 2-1: **Ethernet Frame Command Field Description *(Cont'd)***

Bits	Name	Description
[47:32]	Timestamp or Correction Field Offset	The usage of this field is dependent on the 1588 operation For No operation or 2-step this field is ignored. For 1-step ToD format, this field is a numeric value indicating the number of bytes into the frame to where the first byte of the timestamp field to be inserted is located (where a value of 0 represents the first byte of the Destination Address, etc). For 1-step Correction Field format, this field is a numeric value indicating the number of bytes into the frame to where the first byte of the Correction Field to be modified is located (where a value of 0 represents the first byte of the Destination Address, etc). Only even values of offset are currently supported. ***Note:*** The IPv6 header size is unbounded, so this field is able to cope with all frames sizes up to 16K jumbo frames.
[63:48]	Checksum Offset	The usage of this field is dependent on the 1588 operation and the Update Checksum bit. If using the Correction Field format, then this field is completely ignored because the Checksum location is a fixed number of bytes prior to the position of the Correction Field Offset (fully supporting the IEEE1588 PTP frame formats). If using the ToD format then: • For No operation, 2-step or 1-step when Update Checksum is set to 1'b0, this field is ignored. • For 1-step when Update Checksum is set to 1'b1, this field is a numeric value indicating the number of bytes into the frame to where the first byte of the checksum is located (where a value of 0 represents the first byte of the Destination Address, etc). Only even values of offset are currently supported. ***Note:*** The IPv6 header size is unbounded, so this field is able to cope with all frames sizes up to 16K jumbo frames.

Transmitter Latency and Timestamp Adjustment

Figure 2-2 illustrates the *1588 Sample and add known TX latency* block. The system timer is sampled when the Ethernet Start codegroup (/S/) is observed in the 10-Gigabit Ethernet MAC transmitter pipeline. This is required to update the UDP Checksum and FCS fields with the frame modification for a 1-step operation. For this timestamp to provide reliable system behavior, the following conditions apply.

- The 10-Gigabit Ethernet MAC core contains a fixed latency from the timestamp position onwards through its pipeline.
- The 10-Gigabit Ethernet PCS/PMA core provides a deterministic latency for the transmitter path.
- The 7 series GTX or GTH transceiver provides a deterministic latency through its transmitter path. This is achieved by using the GTX or GTH transceiver in TX buffer Bypass mode.

The logic is also then capable of adjusting the timestamp value taken by adding a configurable duration. (See the 1588 configuration registers described in Enhancements to 10-Gigabit Ethernet MAC Configuration/Status Registers.) This value is user adjustable and should be initialized with the entire transmitter path latency (through the 10-Gigabit Ethernet MAC, 10-Gigabit Ethernet PCS/PMA, and transceiver). This results in the returned timestamp default value representing the time at which the Start codegroup can be first observed on the transceiver serial transmit output. This latency adjust functionality can be applied to either of the ToD or Correction Field formats.

Receive

Figure 2-3 shows the receive side of the AXI 10-Gigabit Ethernet core.

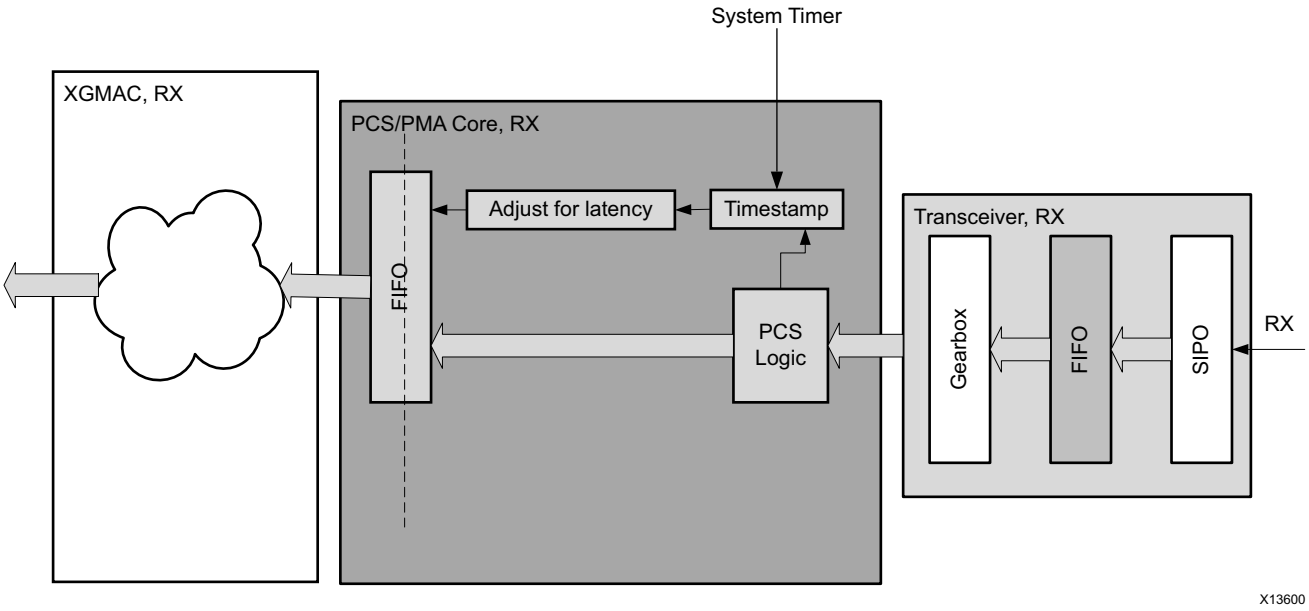

Figure 2-3: **Receive-Side Architecture**

On receive for the ToD format, all frames are timestamped with a captured 80-bit ToD timestamp. The full 80-bit timestamp is provided to the client logic out of band using additional ports defined in Table 2-6. In addition, a 64-bit timestamp can optionally be provided in line with the received frame. This 64-bit timestamp consists of the lower 32 bits from the 1588 timers seconds field, plus all 32 bits of the nanoseconds field. For the Correction Field format, the full 64-bit timestamp is provided to the client logic out of band using additional ports defined in Table 2-6. In addition, the 64-bit timestamp can optionally be provided in line with the received frame.

Receiver Latency and Timestamp Adjustment

Figure 2-3 illustrates a block called *Timestamp* and a block called *Adjust for latency*. This illustrates the timestamp point in the receiver pipeline when the Start codegroup is observed. This timestamp is performed in the 10-Gigabit Ethernet PCS/PMA, prior to any variable length latency logic.

- The 7 series GTX or GTH transceiver provides deterministic latency through its receiver path. This is achieved by using the GTX or GTH transceiver in RX buffer Bypass mode.
- The 10-Gigabit Ethernet PCS/PMA core provides fixed latency for the receiver path up until the timestamp point.

The logic is also then capable of adjusting the timestamp value taken by subtracting a configurable duration (See the 1588 configuration registers described in Enhancements to the 10-Gigabit Ethernet PCS/PMA MDIO Registers.) This value is adjustable and should be initialized with the receiver path latency (transceiver, and 10-Gigabit Ethernet PCS/PMA) prior to the timestamping position. This results in the returned timestamp value representing the time at which the Start codegroup appeared on the transceiver serial input. This latency adjust functionality can be applied to either of the ToD or Correction Field formats.

Standards

The AXI 10-Gigabit Ethernet core is compatible with the following IEEE standards:

- IEEE802.3-2012, the Ethernet standard.
- IEEE1588-2008, version 2 of the Precision Time Protocol (PTP) standard.

Performance

The AXI 10-Gigabit Ethernet core operates at full line-rate in a 10-Gigabit Ethernet system.

Resource Utilization

7 Series and Zynq-7000 Devices

Table 2-2 provides approximate resource counts for the various core options on 7 series and Zynq®-7000 devices.

Table 2-2: **Device Utilization: 7 Series and Zynq-7000 Devices**

Parameter Values			Device Resources	
Statistics Gathering	**1-Step/2-Step**	**Timer Format**	**LUTs**	**FFs**
No	2-Step only	ToD	7320	7960
Yes	2-Step only	ToD	9240	9320
No	1-Step and 2-Step	ToD	7910	8330
Yes	1-Step and 2-Step	ToD	9910	9680
No	2-Step only	Correction Field	6990	7720
Yes	2-Step only	Correction Field	7830	8880
No	1-Step and 2-Step	Correction Field	8090	8150
Yes	1-Step and 2-Step	Correction Field	8930	9320

The results are post-implementation, using tool default settings except for high effort. LUT counts include SRL16s or SRL32s.The resource counts might also be affected by other tool options, additional logic in the device, using a different version of Xilinx tools, and other factors.

Port Descriptions

Client-Side Data Interfaces

Due to the underlying IP Integrator technology used for the AXI 10-Gigabit Ethernet core, there is a remapping of certain signal names from the 10-Gigabit Ethernet MAC cores. This remapping is shown in Table 2-3.

Table 2-3: **Port Name Mappings**

AXI 10-Gigabit Ethernet Port	10-Gigabit Ethernet MAC Port
s_axi_tx_tdata	tx_axis_tdata
s_axi_tx_tkeep	tx_axis_tkeep
s_axi_tx_tlast	tx_axis_tlast
s_axi_tx_tuser	tx_axis_tuser

Table 2-3: **Port Name Mappings *(Cont'd)***

AXI 10-Gigabit Ethernet Port	10-Gigabit Ethernet MAC Port
s_axi_tx_tvalid	tx_axis_tvalid
s_axi_tx_tready	tx_axis_tready
s_axi_pause_tdata	pause_val
s_axi_pause_tvalid	pause_req
m_axi_rx_tdata	rx_axis_tdata
m_axi_rx_tkeep	rx_axis_tkeep
m_axi_rx_tlast	rx_axis_tlast
m_axi_rx_tuser	rx_axis_tuser
m_axis_axis_tvalid	rx_axis_tvalid

Note: All of these interfaces are synchronous to `clk156_out`.

Transmit – Providing the Command Field In-band

For timestamping in the transmit direction, the command field can optionally be provided in-band with the frame sent for transmission on the existing AXI4-Stream data interface – Transmit (see *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072) [Ref 1]). Enabling this mode of operation is through an AXI4-Lite addressable configuration bit – see Table 2-9, bit 22).

When enabled, the 64-bit command field is passed to the AXI 10-Gigabit Ethernet core immediately before the start of frame (Figure 2-4).

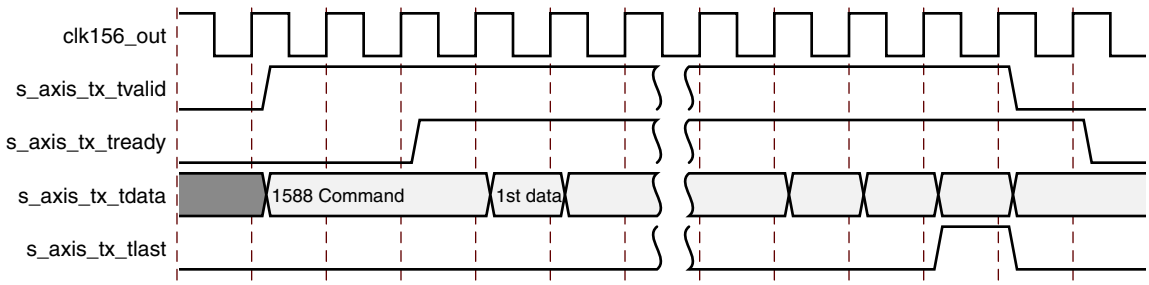

Figure 2-4: **In-band Command Field**

In-band command field passing and custom preamble passing cannot be enabled at the same time. If both are enabled, the Custom Preamble feature takes precedence.

Transmit - Providing the Command Field Out-of-Band

If in-band command field passing is not used (for example, bit 22 is set to 0), the command field can be provided out-of-band using a subfield of the `s_axis_tx_tuser` port on the core. The subfields within the `s_axis_tx_tuser` signal are shown in Table 2-4.

Table 2-4: **Port Definition**

Bits	Name	Description
s_axis_tx_tuser [0]	Underrun	AXI4-Stream User signal used to signal explicit underrun. This is as per the current definition in *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072) [Ref 1].
s_axis_tx_tuser[63:1]	Reserved	Reserved for future use (all bits are ignored).
s_axis_tx_tuser[127:64]	Command Field	A 64-bit field as per the Command Field definition of Table 2-1.

Figure 2-5 shows a timing diagram for the out-of-band command field. The command subfield in `s_axis_tx_tuser` must be valid on the same clock cycle when the first data word is sent for transmission.

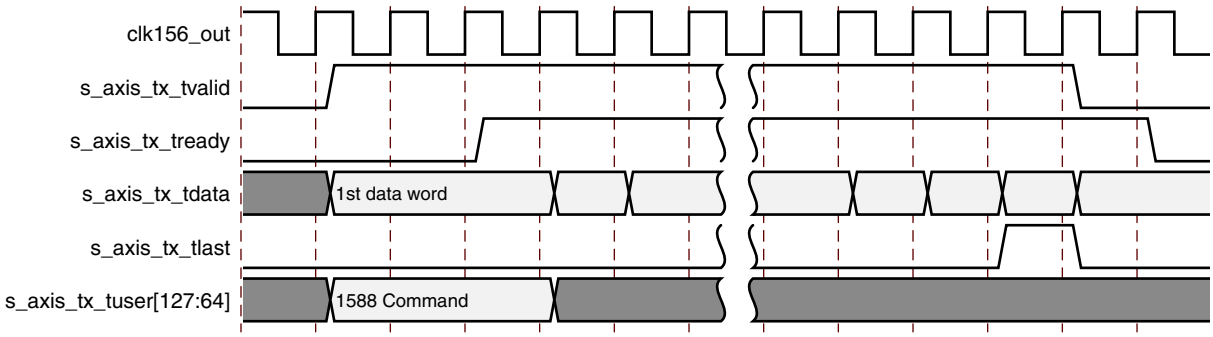

Figure 2-5: **Out-of-Band Command Field**

Transmitted Timestamp Ports

When the command field signals 1-step or 2-step timestamping on transmit, the captured timestamp and tag are presented on a dedicated AXI4-Stream interface. The signal definition and timing diagram are shown in Table 2-5 and Figure 2-6.

Table 2-5: **Port Definition**

Name	Direction	Description
m_axis_tx_ts_tdata[127:0]	Out	**ToD Timestamp Format** m_axis_tx_ts_tdata[31:0]: Transmit Timestamp from the 10-Gigabit Ethernet MAC, nanoseconds. m_axis_tx_ts_tdata[79:32]: Transmit Timestamp from the 10-Gigabit Ethernet MAC, seconds. m_axis_tx_ts_tdata[95:80]: Original 16-bit Tag Field for the frame (from the Tag Field of the Command Field for the frame sent for transmission). m_axis_tx_ts_tdata[127:96]: Reserved for future use (all bits should be ignored). **Correction Field Timestamp Format** m_axis_tx_ts_tdata[63:0]: Transmit Timestamp from the 10-Gigabit Ethernet MAC. m_axis_tx_ts_tdata[79:64]: Reserved for future use (all bits should be ignored). m_axis_tx_ts_tdata[95:80]: Original 16-bit Tag Field for the frame (from the Tag Field of the Command Field for the frame sent for transmission). m_axis_tx_ts_tdata[127:96]: Reserved for future use (all bits should be ignored).
m_axis_tx_ts_tvalid	Out	AXI4-Stream Transmit Timestamp Data Valid from the 10-Gigabit Ethernet MAC.

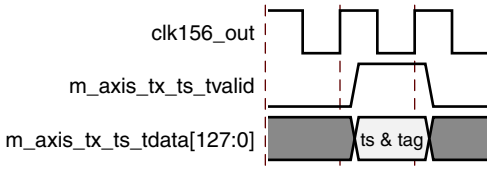

Figure 2-6: **Transmit Timestamp Out**

Receive – Timestamp In Line With Frame Reception

The captured timestamp can optionally be provided in line with the received frame using the AXI4-Stream Interface – Receive (see *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072) [Ref 1]).

You can enable this mode of operation through an AXI4-Lite addressable configuration bit (see Table 2-10, bit 22). When enabled, a 64-bit timestamp field is passed to the client immediately before the start of frame reception (in place of the Preamble field). This is illustrated in Figure 2-7.

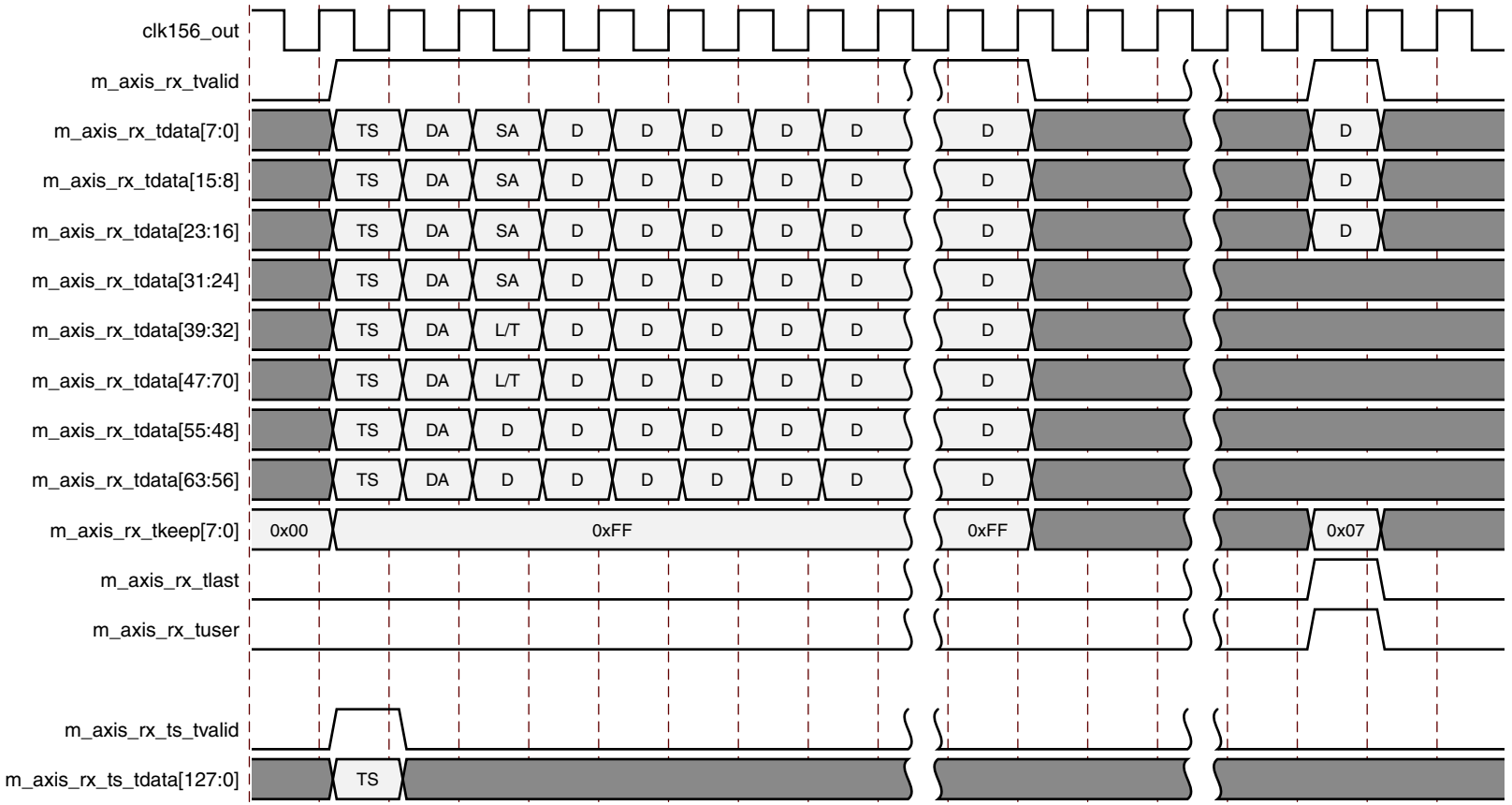

Figure 2-7: **Receive Timestamp Timing Diagram**

For the ToD format, the 64 bits are made up of the timestamp nanosecond field in bits [31:0] of `m_axis_rx_tdata`, and the lower 32 bits of the timestamp seconds field in bits [63:32] of `m_axis_rx_tdata`. For the Correction Field format, the timestamp is completely contained.

You cannot enable in-band command field passing and custom preamble passing at the same time. If both are enabled, the custom preamble feature takes precedence.

Received Timestamp Ports (Out-of-Band)

The captured timestamp is always presented out-of-band upon frame reception using a dedicated AXI4-Stream interface. The signal definition is found in Table 2-6.

Table 2-6: **Port Definition**

Name	Direction	Clock Domain	Description
m_axis_rx_ts_data[127:0]	Out	clk156_out	AXI4-Stream Receive Timestamp value. **ToD Timestamp Format** [127:80]: Reserved: all bits should be ignored. [79:32]: The timestamped value of the seconds field for the current frame. [31:0]: The timestamped value of the nanoseconds field for the current frame. **Correction Field Timestamp Format** m_axis_tx_ts_tdata[63:0]: Transmit Timestamp from the 10-Gigabit Ethernet MAC. m_axis_tx_ts_tdata[127:64]: Reserved for future use (all bits should be ignored).
m_axis_rx_ts_tvalid	Out	clk156_out	AXI4-Stream Receive Timestamp Data Valid

Figure 2-7 shows a timing diagram of the operation of this interface. To summarize, the timestamp is valid in the same clock cycle as the first data beat of frame data. Figure 2-7 illustrates this for the case where the in-line timestamp is enabled and so the timestamp is the first data beat of the frame. When the in-line timestamp is not enabled, the first data beat of the frame is the address fields.

IEEE1588 System Timer Ports

Time-of-Day (ToD) System Timer Format

The IEEE1588 system-wide Time-of-Day (ToD) timer is provided to the core using the ports defined in Table 2-7.

Table 2-7: **IEEE1588 System Timer Ports**

Name	Direction	Clock Domain	Description
systemtimer_clk	In	-	Clock for the system timer provided to the core.
systemtimer_s_field[47:0]	In	systemtimer_clk	The 48-bit seconds field of the 1588-2008 system timer. This increases by 1 every time the systemtimerin_ns_field[29:0] is reset back to zero.
systemtimer_ns_field[31:0]	In	systemtimer_clk	The 32-bit nanoseconds field of the 1588-2008 system timer. This counts from 0 up to $(1x10^9)$-1 [1 second], then resets back to zero.

Correction Field System Timer Format

The 64-bit Correction Field timer, using the numerical format defined in IEEE1588 clause 13.3.2.7, is provided to the core using the ports defined in Table 2-8.

Table 2-8: **Correction Field System Timer Ports**

Name	Direction	Clock Domain	Description
correctiontimer_clk	In	-	Clock for the system timer provided to the core.
Correction_timer[63:0]	In	correctiontimer_clk	Bits [63:16] represent a 48-bit signed ns field. Bits[15:0] represents a fractional ns field (bit 15 represents a half ns, bit 14 represents a quarter ns, bit 13 represents one eighth ns,... This timer should count from 0 through the full range up to 2^{64} -1 before wrapping around.

Register Space

10-Gigabit Ethernet MAC Registers

All existing registers of the integrated 10-Gigabit Ethernet MAC core are present in the AXI 10-Gigabit Ethernet core, and can be accessed through the AXI4-Lite slave interface. For more information related to these registers, see the *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072) [Ref 1].

10-Gigabit Ethernet PCS/PMA Registers

All existing registers of the integrated 10-Gigabit Ethernet PCS/PMA core are present in the AXI 10-Gigabit Ethernet core, and can be accessed through the AXI4-Lite slave interface over the integrated MDIO bus.

For more details on the 10-Gigabit Ethernet PCS/PMA MDIO register space, see the *LogiCORE IP 10-Gigabit Ethernet PCS/PMA Product Guide* (PG068) [Ref 2]. For information on accessing the MDIO registers over the AXI4-Lite slave interface of the AXI 10-Gigabit Ethernet core, see the "MDIO Interface" section in the *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072) [Ref 1].

Additional Registers to Support IEEE 1588

To support IEEE1588 timestamping, some registers have been added to both the 10-Gigabit Ethernet MAC and the 10-Gigabit Ethernet PCS/PMA cores.

Enhancements to 10-Gigabit Ethernet MAC Configuration/Status Registers

Transmitter Configuration Word (Address 0x408)

Bit 22 was previously reserved, and is now defined as follows:

Table 2-9: **Transmitter Configuration Word**

Bits	Default Value	Type	Description
21:0	N/A	RO	Reserved.
22	0	RW	In-band 1588 Command Field Enable. When 0, the Command Field is provided out-of-band. When 1, the Command Field is provided in line. If bit 23 (Preserve Preamble) is set, that bit takes precedence over this one.
23	0	R/W	Transmit Preserve Preamble Enable. **Important!** This bit takes precedence over bit 22, In-band Command Field Enable.
24	0	R/W	Deficit Idle Count Enable.
25	0	RW	Interframe Gap Adjust Enable.
26	0	RW	WAN Mode Enable.
27	0	RW	VLAN Enable.
28	1	RW	Transmit Enable.
29	0	RW	Inband FCS Enable.
30	0	RW	Jumbo Frame Enable.
31	0	RW	Reset.

Receiver Configuration Word (Address 0x404)

Bit 22 was previously reserved, and is now defined as follows:

Table 2-10: **Receiver Configuration Word**

Bits	Default Value	Type	Description
15:0	0	RW	Pause frame MAC Source Address[47:32].
21:16	N/A	RO	Reserved.
22	0	RW	In-band 1588 Timestamp Enable. When 0, the Timestamp is only provided out-of-band. When 1, the Timestamp is provided in line in addition to out-of-band. Bit 26 (Preamble Preserve) has precedence over this one.
23	0	RO	Reserved
24	0	RW	Control Frame Length Check Disable.
25	0	RW	Length/Type Error Check Disable.

Table 2-10: **Receiver Configuration Word *(Cont'd)***

Bits	Default Value	Type	Description
26	0	RW	Received Preamble Preserve. **Important!** This bit has precedence over bit 22, In-band Timestamp Enable.
27	0	RW	VLAN Enable.
28	1	RW	Receiver Enable.
29	0	RW	In band FCS Enable.
30	0	RW	Jumbo Frame Enable.
31	0	RW	Reset.

Transmitted Timestamp Adjustment Control Register (0x41c)

The fixed portion of the transmit latency adjustment to the timestamp is maintained in a programmable register. This allows field adjustment for external factors, such as additional pipelining or board delays. This new register is defined as follows:

Table 2-11: **Transmitted Timestamp Adjustment Control Register**

Bits	Default Value	Type	Description
15:0	0x0000	RW	Transmit latency adjust value. This value is in units of nanoseconds, and should be initialized to reflect the delay following the timestamp datum through the MAC and PHY components.
16	0	RW	Transmitted Timestamp correction enable. When 0, the transmit timestamp is not adjusted. When 1, the transmit timestamp is adjusted.
31:17	0	RO	Reserved.

Enhancements to the 10-Gigabit Ethernet PCS/PMA MDIO Registers

IEEE1588 Control (Address 3.65520)

Table 2-12: **IEEE1588 Control**

Bits	Default Value	Type	Description
0	1	RW	PMA Adjust Enable. When 1, a timestamp correction is made for the state of the RX PMA barrel shifter. When 0, no correction is made.
1	1	RW	Gearbox State Adjust Enable. When 1, a timestamp correction is made for the state of the RX gearbox in the transceiver. When 0, no correction is made.

Table 2-12: **IEEE1588 Control *(Cont'd)***

Bits	Default Value	Type	Description
2	1	RW	Fixed Latency Adjust Enable. When 1, the timestamp is adjusted by the amount in registers 3.65521 and 3.65522. When 0, no adjustment is made.
3	1	RW	Timestamp Correction Enable. When 1, the RX timestamp is adjusted to compensate for enabled PHY fixed and variable latencies. When 0, no adjustment is made to the timestamp.
15:4	N/A	RO	Reserved.

RX Fixed Latency, Integer ns (Address 3.65521)

Table 2-13: **RX Fixed Latency, Integer ns**

Bits	Default Value	Type	Description
15:0	0x0000	RW	Fixed latency in nanoseconds, integer part. When Fixed Latency Adjust bit is set to 1, this value is used to adjust for the fixed latency components of the offset between the timestamp point and the edge of the device.

RX Fixed Latency, Fractional ns (Address 4.65522)

Table 2-14: **RX Fixed Latency, Fractional ns**

Bits	Default Value	Type	Description
15:0	0x0000	RW	Fixed latency in nanoseconds, fractional part. When Fixed Latency Adjust bit is set to 1, this value is used to adjust for the fixed latency components of the offset between the timestamp point and the edge of the device.

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

Clocking

For the AXI 10-Gigabit Ethernet core, all data interfaces (including `s_axis_tx`, `s_axis_pause`, `m_axis_rx`, `m_axis_tx_ts`, `m_axis_rx_ts`) are synchronous to the `clk156_out` port of the core. This clock is generated within the support layer of the integrated 10-Gigabit Ethernet PCS/PMA core. For more information on the clock and the other logic included in the support layer of the core, see *LogiCORE™ IP 10-Gigabit Ethernet PCS/PMA Product Guide* (PG068) [Ref 2].

The management interface `s_axi` is associated with the `s_axi_aclk` input. For more information on the requirements for the `s_axi_aclk` input, see the *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072) [Ref 1].

Resets

The reset input provides an active-high global asynchronous reset input that resets everything in the design, including the transceiver and associated PLLs.

When the reset sequencing is complete, the `areset_clk156_out` signal asserts High. This signal is synchronous to `clk156_out`. For more information, see *LogiCORE IP 10-Gigabit Ethernet PCS/PMA Product Guide* (PG068) [Ref 2].

Each of the interface resets (`s_axi_aresetn`, `tx_axis_aresetn` and `rx_axis_aresetn`), apply local resets to sub-blocks of the overall design. These resets should not be required in normal operation or implementation.

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows in the IP Integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 3]
- *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 4]
- *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 5]
- *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 6]

Customizing and Generating the Core

This section includes information about using the Vivado® Design Suite to customize and generate the core.

If you are customizing and generating the core in the Vivado IP Integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 3] for detailed information. IP Integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value you can run the `validate_bd_design` command in the Tcl console.

Vivado Integrated Design Environment

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.
2. Double-click the selected IP, or select the **Customize IP** command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 4] and the *Vivado Design Suite User Guide: Getting Started* (UG910)[Ref 5].

Note: Figures in this chapter are illustrations of the Vivado IDE. This layout might vary from the current version.

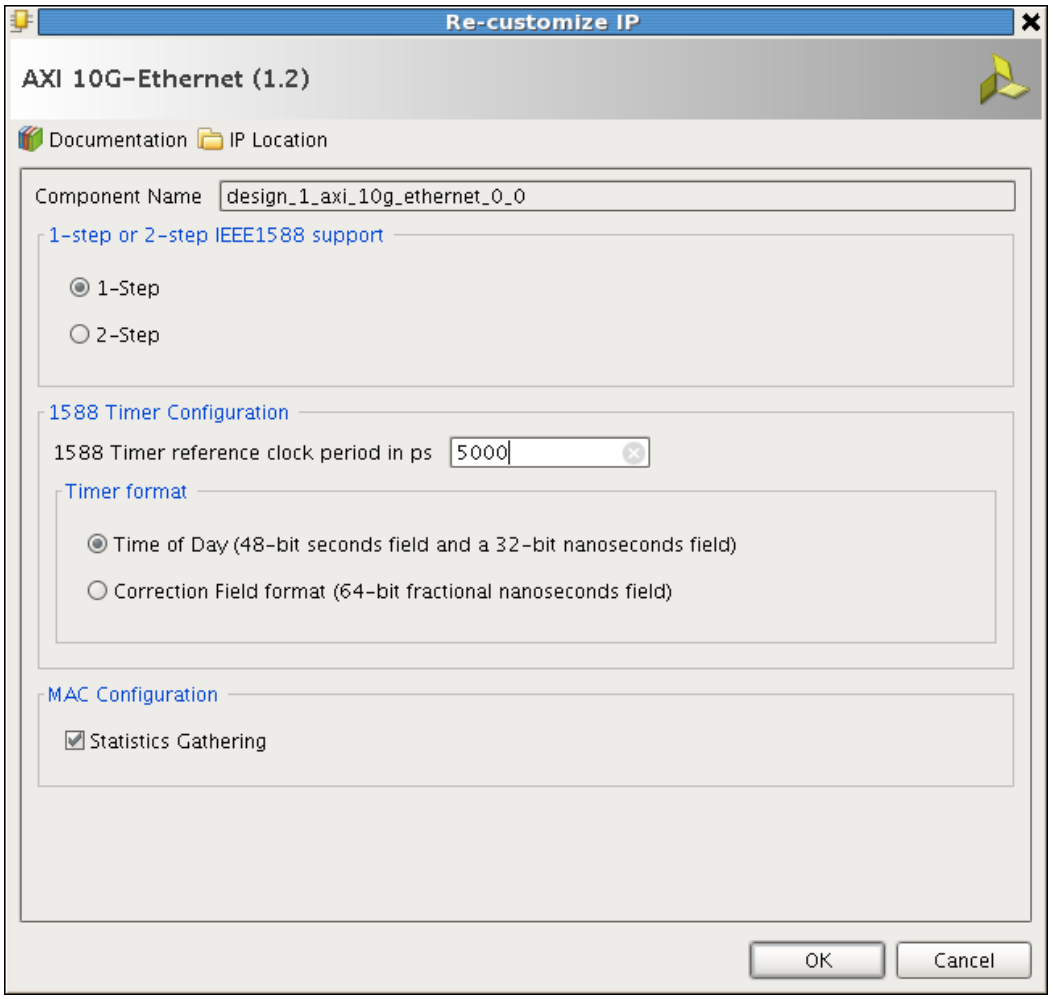

Figure 4-1: **AXI 10-Gigabit Ethernet Customization Options**

1-Step or 2-Step IEEE 1588 Support

This radio button selects whether to include logic that supports 1-step timestamping in the transmit side of the core, including timestamp insertion, UDP/IP checksum update, and Ethernet CRC update. 2-step support is always included.

1588 Timer Reference Clock Period (ps)

Enter the period of `systemtimer_clk` signal (in ps) in this text box. It is used to optimize the logic that hands off the system timer value across the clock domains of the core.

Timer Format

This radio button selects whether to include logic that supports either the Time-of-Day (ToD) timer and timestamp format, or alternatively to support the Correction Field timer and timestamp format.

Statistics Gathering

Check this box to include 10-Gigabit Ethernet MAC statistics counters. For more information, see the *LogiCORE™ IP 10-Gigabit Ethernet MAC Product Guide* (PG072) [Ref 1].

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 4].

Constraining the Core

This section contains information about constraining the core in the Vivado Design Suite environment.

Required Constraints

Because the AXI 10-Gigabit Ethernet core is a hierarchical core, it enables the use of timing constraints from the infrastructure cores. The core automatically acquires constraints from the subcores.

User-supplied clock period constraints are required on:

- The `refclk_p` and `refclk_n` pair (see the *LogiCORE™ IP 10-Gigabit Ethernet PCS/PMA Product Guide* (PG068) [Ref 2]
- The `s_axi_aclk` signal (see the *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072) [Ref 1]).

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

Reference clock placement must be compatible with the transceiver placement used. For more information, see the transceiver user guide for the transceiver in use.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

For comprehensive information about Vivado Design Suite simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 6].

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 4].

Migrating and Upgrading

This appendix contains information about migrating a design from the ISE® Design Suite to the Vivado® Design Suite, and for upgrading to a more recent version of the IP core. For customers upgrading in the Vivado Design Suite, important details (where applicable) about any port changes and other impact to user logic are included.

Migrating to the Vivado Design Suite

For information about migrating to the Vivado Design Suite, *see the ISE to Vivado Design Suite Migration Guide* (UG911) [Ref 7].

Upgrading in the Vivado Design Suite

This section provides information about any changes to the user logic or port designations that take place when you upgrade to a more current version of this IP core in the Vivado Design Suite.

The changes for v1.2 are backwards compatible.

Parameter Changes

None.

Port Changes

None.

Other Changes

None.

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

TIP: *If the IP generation halts with an error, there may be a license issue. See License Checkers in Chapter 1 for more details.*

Finding Help on Xilinx.com

To help in the design and debug process when using the AXI 10-Gigabit Ethernet, the Xilinx Support web page (www.xilinx.com/support) contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the AXI 10-Gigabit Ethernet core. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page (www.xilinx.com/support) or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the Design Tools tab on the Downloads page (www.xilinx.com/download). For more information about this tool and the features available, open the online help after installation.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

The Solution Center specific to the AXI 10-Gigabit Ethernet core is listed below.

- Xilinx Ethernet IP Solution Center

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use keywords such as

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the AXI 10-Gigabit Ethernet

AR: 57358

Contacting Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support:

1. Navigate to www.xilinx.com/support.
2. Open a WebCase by selecting the WebCase link located under Additional Resources.

When opening a WebCase, include:

- Target FPGA including package and speed grade.
- All applicable Xilinx Design Tools and simulator software versions.
- Additional files based on the specific issue might also be required. See the relevant sections in this debug guide for guidelines about which file(s) to include with the WebCase.

Note: Access to WebCase is not available in all cases. Log in to the WebCase tool to see your specific support options.

Debug Tools

There are many tools available to address AXI 10-Gigabit Ethernet design issues. It is important to know which tools are useful for debugging various situations.

Vivado Lab Tools

Vivado® lab tools insert logic analyzer and virtual I/O cores directly into your design. Vivado lab tools also allow you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx devices.

The Vivado logic analyzer is used with the logic debug IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 8].

Hardware Debug

Hardware issues can range from link bring-up to problems seen after hours of testing. This section provides debug steps for common issues. The Vivado lab tools are a valuable resource to use in hardware debug. The signal names mentioned in the following individual sections can be probed using the Vivado lab tools for debugging specific problems.

General Checks

Ensure that all the timing constraints for the core were properly incorporated from the example design and that all constraints were met during implementation.

- Does it work in post-place and route timing simulation? If problems are seen in hardware but not in timing simulation, this could indicate a PCB issue. Ensure that all clock sources are active and clean.
- If using MMCMs in the design, ensure that all MMCMs have obtained lock by monitoring the `LOCKED` port.
- If your outputs go to 0, check your licensing.

Interface Debug

Interface debug should be performed according to the information provided in the product guides of the underlying IP cores.

Additional Resources and Legal Notices

This appendix describes additional resources and references pertaining to the AXI 10-Gigabit Ethernet core.

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

For a glossary of technical terms used in Xilinx documentation, see the Xilinx Glossary.

References

These documents provide supplemental material useful with this product guide:

1. *LogiCORE IP 10-Gigabit Ethernet MAC Product Guide* (PG072)
2. *LogiCORE IP 10-Gigabit Ethernet PCS/PMA Product Guide* (PG068)
3. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
4. *Vivado Design Suite User Guide: Designing with IP* (UG896)
5. *Vivado Design Suite User Guide: Getting Started* (UG910)
6. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
7. *ISE to Vivado Design Suite Migration Guide* (UG911)
8. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
9. *AMBA® AXI4-Stream Protocol Specification* (ARM IHI 0051A)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/2014	1.2	Added support for IEEE1588 Correction Field modification using the alternative Correction Field formatted system timer.
12/18/2013	1.1	Added support for GTHE2 transceivers. Corrected default values for the IEEE1588 Control register.
10/02/2013	1.0	Initial Xilinx release.

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