

Introduction

The ChipScope™ Pro IBERT core for Kintex™-7 FPGA GTX transceivers is customizable and designed for evaluating and monitoring Kintex-7 FPGA GTX transceivers. This core includes pattern generators and checkers that are implemented in FPGA logic, and access to ports and the dynamic reconfiguration port attributes of the GTX transceivers. Communication logic is also included to allow the design to be run-time accessible through JTAG. This core can be used as a self-contained or an open design, based on customer configuration, and as described in this document.

Features

- Provides a communication path between the ChipScope Pro Analyzer software and the IBERT core.
- Has user-selectable number of Kintex-7 FPGA GTX transceivers.
- Each transceiver can be customized for the desired line rate, reference clock rate, reference clock source, and datapath width.
- Requires a system clock that can be sourced from a pin or one of the enabled GTX transceivers.

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family ⁽¹⁾	Kintex-7				
Supported User Interfaces	N/A				
Resources ⁽²⁾					Frequency
Configuration	LUTs	FFs	DSP Slices	Block RAMs	Max. Freq ⁽³⁾
Config1	2401	4120	0	0	306.551 MHz
Config2	8359	14533	0	0	295.859 MHz
Config3	23516	41022	0	0	246.233 MHz
Provided with Core					
Documentation	Product Specification User Guide				
Design Files	Netlist				
Example Design	Verilog/VHDL				
Test Bench	Not Provided				
Constraints File	Xilinx Constraints and Synthesis Constraints				
Simulation Model	Not Provided				
Tested Design Tools					
Design Entry Tools	Xilinx CORE Generator™ tool				
Simulation	Not Provided				
Synthesis Tools	Not Provided				
Support					
Provided by Xilinx @ www.xilinx.com/support					

1. Including the variants of this FPGA device.
2. Resources listed here are for Kintex-7 devices. For more complete device performance numbers, see [Table 2](#).
3. Performance numbers listed are for Kintex-7 FPGAs. For more complete performance data, see [Performance and Resource Utilization](#).

Applications

The IBERT core is designed to be used in any application that requires verification or evaluation of Kintex-7 FPGA GTX transceivers.

Functional Description

The IBERT core provides a broad-based Physical Medium Attachment (PMA) evaluation and demonstration platform for Kintex-7 FPGA GTX transceivers. Parameterizable to use different GTX transceivers and clocking topologies, the IBERT core can also be customized to use different line rates, reference clock rates, and logic widths. Data pattern generators and checkers are included for each GTX transceiver desired, giving a variety of different Pseudo-random binary sequence (PRBS) and clock patterns to be sent over the channels. The configuration and tuning of the GTX transceivers is accessible through logic that communicates to the DRP port of the GTX transceiver. This allows changing attribute settings and registers that control the values on the ports. At run time, the ChipScope Analyzer tool communicates to the IBERT core through JTAG, using the Xilinx cables and proprietary logic that is part of the IBERT core.

GTX Transceiver Features

IBERT is designed for Physical Medium Attachment (PMA) evaluation and demonstration. All the major PMA features of the GTX transceiver are supported and controllable in IBERT, including:

- TX pre-emphasis and post-emphasis
- TX differential swing
- RX equalization
- Decision Feedback Equalizer (DFE)
- Phase-Locked Loop (PLL) Divider settings

Some of the Physical Coding Sublayer (PCS) features offered by the transceiver are outside the scope of IBERT, including

- Clock Correction
- Channel Bonding
- 8B/10B, 64B/66B, or 64B/67B encoding
- TX or RX Buffer Bypass

PLL Configuration

For each Serial Transceiver Channel, there is a ring Phase-Locked Loop (PLL) called Channel PLL (CPLL). The GTX in the Kintex-7 FPGA has an additional shared PLL per quad, Quad PLL (QPLL). This QPLL is shared LC PLL to support high speed, high performance and low power multi-lane applications.

Figure 1 shows a Quad in a Kintex-7 device. The GTXE2_CHANNEL component has the serial transceiver and CPLL units and the GTXE2_COMMON has the QPLL unit.

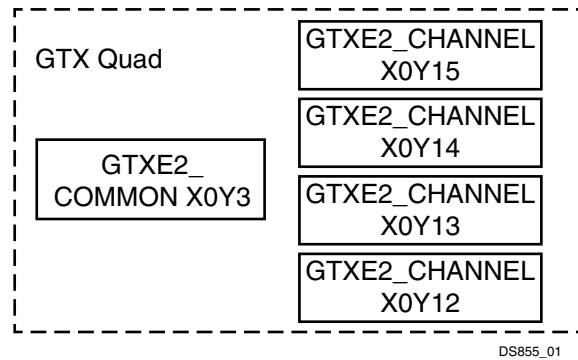


Figure 1: Quad in a Kintex-7 Device

The serial transceiver REFCLK can be sourced from either CPLL or QPLL based on multiplexers as shown in Figure 2. This can be selected from the Kintex-7 FPGA IBERT CORE Generator tool GUI.

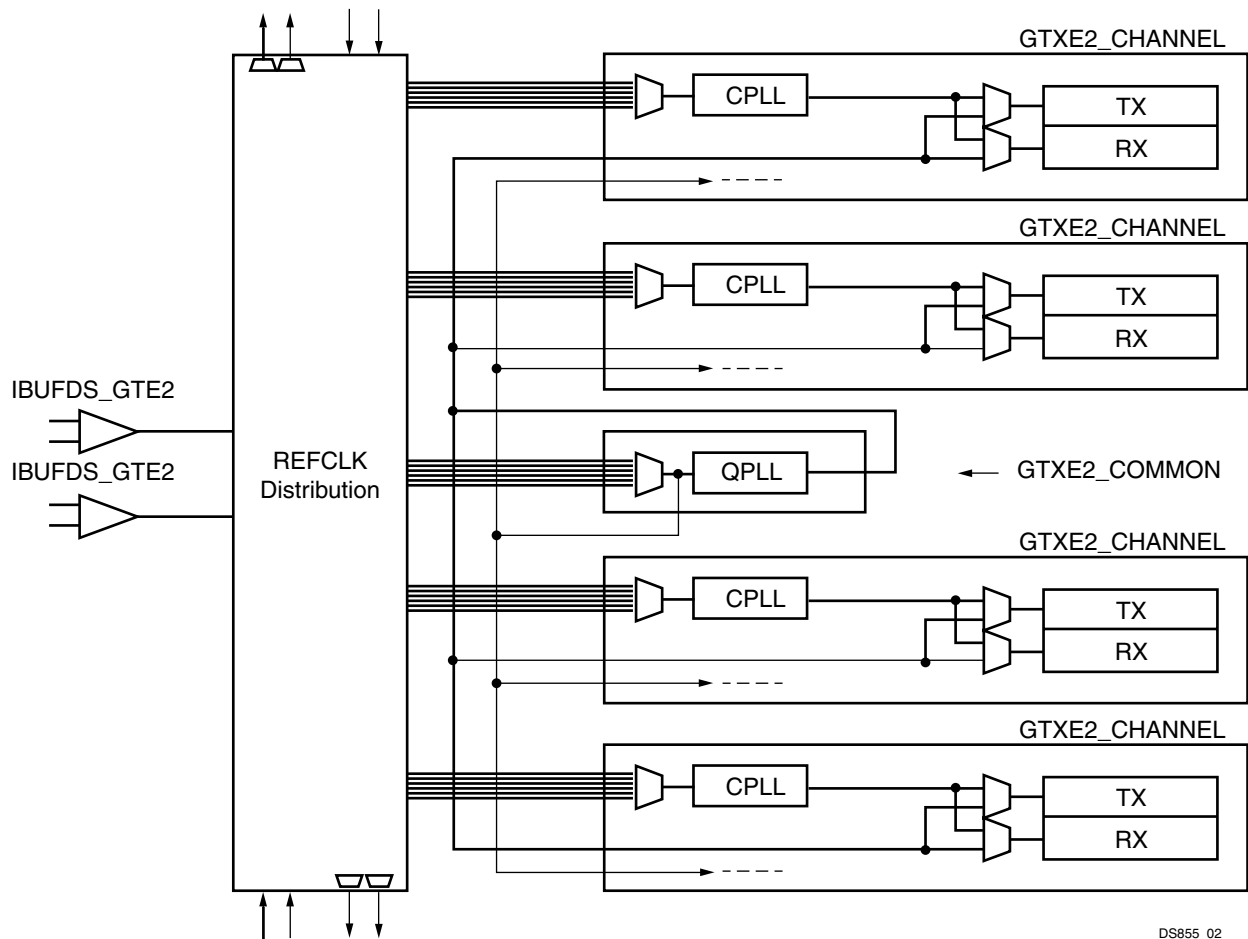


Figure 2: Serial Transceiver REFCLK Sourcing

Pattern Generation and Checking

Each GTX transceiver enabled in the IBERT design has both a pattern generator and a pattern checker. The pattern generator sends data out through the transmitter. The pattern checker takes the data coming in through the receiver and checks it against an internally generated pattern. IBERT offers PRBS 7-bit, PRBS 15-bit, PRBS 23-bit, PRBS31-bit, Clk 2x (101010...) and Clk 10x(11111111110000000000...) patterns.

These patterns are optimized for the logic width chosen, and are selectable at run time. The TX pattern and RX pattern are individually selectable.

The Analyzer software displays a 'link' signal until there are five consecutive cycles with errors. Using the pattern checker logic, the incoming data is compared against a pattern that is internally generated. When the checker receives five consecutive cycles of data with errors, the Analyzer software disables the link signal. Internal counters accumulate the number of words and error received.

DRP and Port Access

IBERT also provides flexibility for users to change GTX transceiver ports and attributes. DRP interface logic is included in the IBERT core to allow the run-time software to monitor and change any attribute in any of the GTX transceivers and the corresponding CPLL/QPLL. When applicable, readable and writable registers are also included that are connected to the various ports of the GTX transceiver. All are accessible at run time using the ChipScope Analyzer tool.

Xilinx CORE Generator Tool

The Xilinx CORE Generator tool allows you to define and generate a customized IBERT core to use to validate the transceivers of the device. You can customize the number of serial transceivers, line rate and reference clock, and PLL selection for each serial transceiver.

Entering the Component Name

The Component Name field, stored as `component_name` in the generated XCO parameter file, can consist of any combination of alpha-numeric characters in addition to the underscore symbol. However, the underscore symbol cannot be the first character in the component name.

Generating an Example Design

The IBERT CORE Generator tool normally generates example design along with standard Xilinx CORE Generator output files, such as a netlist and instantiation template files. Example design and Implement scripts are generated under the folder with the component name.

Generate Bitstream

The Generate Bitstream by default is enabled and when it is generated, it runs through the entire implementation flow, including bitstream generation. When Generate Bitstream is disabled and generated, the design will run through synthesis. You can edit the example design and embed the custom design along with the IBERT instance. The implement script provided with the generated files allows you to run the example design until bitstream generation.

Receiver Output Clock

The receiver clock probe enable is provided if you want to pull out a recovered clock from any serial transceiver. When enabled, a new panel appears just before the summary page where you can fill in the serial transceiver source and probe pin standards.

GTX Transceiver Naming Style

There are two conventions for the GTX transceiver name based on the location in the serial transceiver tile in the device. M and n in X_mY_n naming convention indicate the X and Y coordinates of the serial transceiver location. M and n in serial transceiver m_n naming convention indicating serial transceiver number and quad associated.

System Clock

The IBERT core requires a free-running system clock to clock the communication and other logic included in the core. This clock can be chosen at generation time to come from an FPGA pin, or be driven from the TXOUTCLK port of one of the GTX transceivers in the core. In order for the core to operate properly, this system clock source must remain operational and stable when the FPGA is configured with the IBERT core design. If the system clock is running faster than 150 MHz, it is divided down internally using an Mixed-Mode Clock Manager (MMCM) to satisfy timing constraints.

Line Rate Support

IBERT supports a maximum of three different line rates in a single design. For each of these line rates, select a custom value based on your requirements. You can also choose from pre-provided industry standard protocols such Common Packet Radio Interface (CPRI™), gigabit Ethernet, eXtended Attachment Unit Interface (XAUI). For each line rate, you should specify the number of serial transceivers that will be programmed with these settings. Because usage of QPLL is recommended for line rates above 6.5 Gb/s, you are given a choice to select QPLL/CPLL for each line rate falling in the range 0.6 Gb/s to 6.5 Gb/s.

Serial Transceiver Location

Based on the total number of serial transceivers selected in the previous panel, you should provide the specific location of each serial transceiver that you intend to use. The region shown in the panel indicates the location of serial transceivers in the tile. This demarcation of region is based on the physical placement of serial transceivers with respect to median of BUFGs available for each device.

Reference Clock

For all the serial transceivers selected, the reference clock source should be provided. The drop-down list provides you with possible sources based on local clocks in the same quad and shared clocks from north/south quads.

Generating the Core

After entering the IBERT core parameters, click Generate to create the IBERT core files. After the IBERT core has been generated, a list of files that are generated will appear in a separate window called "Readme <corename>".

IBERT Interface Ports

The I/O signals of the IBERT core consist only of the GTX transceiver reference clocks, the GTX transceiver transmit and receive pins, and a system clock (optional).

Table 1: Interface Ports

Port Name	Direction	Description
IBERT_SYSCLOCK_I	IN	Clock that clocks all communication logic. This port is present only when an external clock is selected in the generator.
CONTROL[35:0]	IN/OUT	Control bus connection to the ICON core.
XiYj_TX_P_OPAD-1:0] ⁽¹⁾ XiYj_TX_P_OPAD[n-1:0] ⁽¹⁾	OUT	Transmit differential pairs for each of the n GTX transceivers used.
XiYj_RX_N_IPAD[n-1:0] ⁽¹⁾ XiYj_RX_P_IPAD[n-1:0] ⁽¹⁾	IN	Receive differential pairs for each of the n GTX transceivers used.
MGTREFCLK_P[m-1:0] ⁽²⁾	IN	GTX transceiver reference clocks used. Note: The number of MGTREFCLK ports can be equal to or less than the number of transmit and receive ports because some GTX transceivers can share clock inputs.
XiYj_RXOUTCLK_O ⁽¹⁾	OUT	Quad based RX output clock.

1. The XiYj name refers to the GTX site location.
2. The Qk name refers to the GTX quad site location.

Performance and Resource Utilization

Table 2: Configuration Details

Configuration Name	Device	IBERT Setup
Config1	XC7K325T-2FFG900	1 serial transceiver with line rate set to 10.3125 Gb/s
Config2	XC7K325T-2FFG900	4 serial transceivers with line rate set to 10.3125 Gb/s
Config3	XC7K325T-2FFG900	12 serial transceivers with line rate set to 10.3125 Gb/s

Verification

Xilinx has verified the IBERT core in a proprietary test environment, using an internally developed bus functional model.

References

- More information on the ChipScope Pro software and cores is available in the *Software and Cores User Guide*, located at www.xilinx.com/documentation.
- For more information about the Kintex-7 FPGA GTX transceiver, see the *7 Series FPGAs GTX Transceivers User Guide*, located at www.xilinx.com/documentation.

Support

Xilinx provides technical support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The IBERT core is provided under the Integrated Software Environment (ISE®) Design Suite End-User License Agreement and can be generated using the Xilinx CORE Generator™ system 13.3 or higher. The CORE Generator system is shipped with Xilinx ISE Design Suite development software.

Contact your local Xilinx [sales representative](#) for pricing and availability of additional Xilinx LogiCORE IP modules and software. Information about additional Xilinx LogiCORE IP modules is available on the Xilinx [IP Center](#).

List of Acronyms

Acronym	Spelled Out
CPRI	Common Packet Radio Interface
DFE	Decision Feedback Equalizer
DRP	Dynamic Reconfiguration Port
FF	Flip-Flop
FPGA	Field Programmable Gate Array
IBERT	Integrated Bit Error Ratio Tester
I/O	Input/Output
ILA	Integrated Logic Analyzer
ISE	Integrated Software Environment
JTAG	Joint Test Action Group
LUT	Lookup Table
MMCM	Mixed-Mode Clock Manager
MHz	Mega Hertz
PCS	Physical Coding Sublayer
PLL	Phase-Locked Loop
PMA	Physical Medium Attachment
PRBS	Pseudorandom binary sequence
RAM	Random Access Memory
RX	Receive
TX	Transmit
XAUI	eXtended Attachment Unit Interface

Revision History

The table shows the revision history for this document:

Date	Version	Description of Revisions
06/22/2011	1.0	Initial Xilinx release
10/19/2011	2.0	Added configuration information, new signals to Table 1, devices to Table 2. Updated for the IDS 13.3. software.

Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties which can be viewed at <http://www.xilinx.com/warranty.htm>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in Critical Applications: <http://www.xilinx.com/warranty.htm#critapps>.