



## Features

- Supported FPGA families: Virtex®-5, Virtex-4, Virtex-II Pro, Virtex-II, Spartan®-3, and Spartan-3A
- MPEG-4 Part 2 Simple Profile standard
- Maximum frame size for standard TV resolutions
- IDCT-based transform
- Macro block processing
- 4:2:0 YUV processing
- Motion compensation
- Residual processing
- 8-bit input data
- 12-bit IDCT coefficients
- AC/DC prediction
- Variable length decoder
- Local YUV buffer
- Communication primitives
- Bit-accurate testing
- I and P Frame Processing

## Applications

Applications for the MPEG-4 Simple Profile Decoder core are:

- **Automotive** – Global Positioning Systems (GPS), collision avoidance systems, and video compression technology.
- **Industrial and Security** – Video sequencing from multiple locations to a central processing location.
- **Broadcasting** – Transmitting information in a highly compressed format to deliver high-quality video both inside and outside studios, as in HDTV.
- **Military** – Video surveillance from military aircraft over wireless communication channels.
- **Video Conferencing** – Transmitting high-quality video to multiple sites in real time.
- **Streaming Video** – Internet communications technology.
- **Video Messaging** – Cellular telephones, including video and small-screen applications.

## General Description

The Xilinx® LogiCORE™ MPEG-4 Part 2 Simple Profile Decoder core is a fully functional VHDL design implemented on a Xilinx FPGA. The MPEG-4 Decoder core accepts compressed video information and recreates a video image suitable for display, based on the “*Information Technology–Generic Coding of Audio Visual Objects–Part 2 Visual*” section of the ISO/IEC 14496-2 standard. For a list of unsupported features, see the *MPEG-4 Simple Profile Decoder Data Sheet (DS338)*.

The MPEG-4 Decoder core requires a memory controller to perform motion compensation algorithms, necessitated by the MPEG standard. The *MPEG-4 Simple*

*Profile Decoder Data Sheet* addresses varied requirements with two options: one with a memory controller and one without, designated as two discrete subcores under the same general heading of an MPEG-4 Simple Profile Decoder core.

Because of the variety of possible video image resolutions, Xilinx provides netlists for two video resolutions (CIF and 4CIF) for each of the supported FPGA families.

## Resources

Table 1: Virtex-4, Virtex-II Pro, Virtex-II, Spartan-3, and Spartan-3A FPGA Resource Usage

| Resources                                    | Slices | LUTs | FFs  | Block RAMs | Mults/<br>DSP48s |
|--|--------|------|------|------------|------------------|
| CIF 1-Stream Decoder                         | 4577   | 7929 | 2625 | 19         | 34               |
| CIF 1-Stream Decoder with Memory Controller  | 5033   | 8605 | 2974 | 22         | 34               |
| 4CIF 1-Stream Decoder                        | 4637   | 7923 | 2637 | 26         | 34               |
| 4CIF 1-Stream Decoder with Memory Controller | 5139   | 8738 | 3082 | 29         | 34               |

Table 2: Virtex-5 FPGA Resource Usage

| Resources Used                 | LUTs  | FFs   | Block RAMs | DSP48s |
|--------------------------------|-------|-------|------------|--------|
| CIF without Memory Controller  | 4,472 | 2,429 | 5          | 32     |
| 4CIF without Memory Controller | 5,174 | 2,651 | 15         | 34     |
| CIF with Memory Controller     | 6,170 | 3,221 | 18         | 34     |
| 4CIF with Memory Controller    | 6,230 | 3,228 | 22         | 34     |

## Ordering Information

The MPEG-4 Simple Profile Decoder product, sold as netlist, is provided under the [LogiCORE Core Site License Agreement](#). A free evaluation version is available from Xilinx DSP marketing or from your local Xilinx [sales representative](#). For part number information, go to the MPEG-4 Simple Profile product page on the Xilinx [IP Center](#). To purchase the core, contact your local Xilinx sales representative.

## Revision History

| Date     | Version | Revision                      |
|----------|---------|-------------------------------|
| 10/19/05 | 1.0     | Initial Xilinx release.       |
| 04/14/08 | 1.1     | Updated for core version 1.3. |

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