Data Side OCM Bus v1.0 (v2.00b)

DS480 January 23, 2007 **Product Specification**

Introduction

The DSOCM_V10 core is a data-side On-Chip Memory (OCM) bus interconnect core. The core connects the PowerPC™ 405 data-side OCM interface to OCM peripherals, such as the data-side OCM BRAM controller (DSBRAM_IF_CNTRL). For information about the PowerPC 405 OCM controller interface, see the *PowerPC 405 Processor Block Reference Guide*.

Features

- Single master - no bus arbitration logic
- Configurable multiple slave capability - contains read-data multiplexing when used with 2 or more slaves

LogiCore Facts		
Core Specifics		
Supported Device Family	Virtex™II Pro, Virtex4	
Version of Core	dsocm_v10	v2.00b
Resources Used		
	Min	Max
Slices	0	N/A
LUTs	0	64 [1]
FFs	0	0
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	N/A	
Design Tool Requirements		
Xilinx Implementation Tools	ISE 9.1i or higher	
Verification	N/A	
Simulation	ModelSim SE/PE 5.7f or higher	
Synthesis	XST	
Support		
Support provided by Xilinx, Inc.		

1. Example for 3 slaves. Size increases with number of slaves

Functional Description

The DSOCM_V10 core shown in Figure 1 is a data-side On-Chip Memory (OCM) bus interconnect core. The signals shown in the block diagram are listed and described in Table 1.

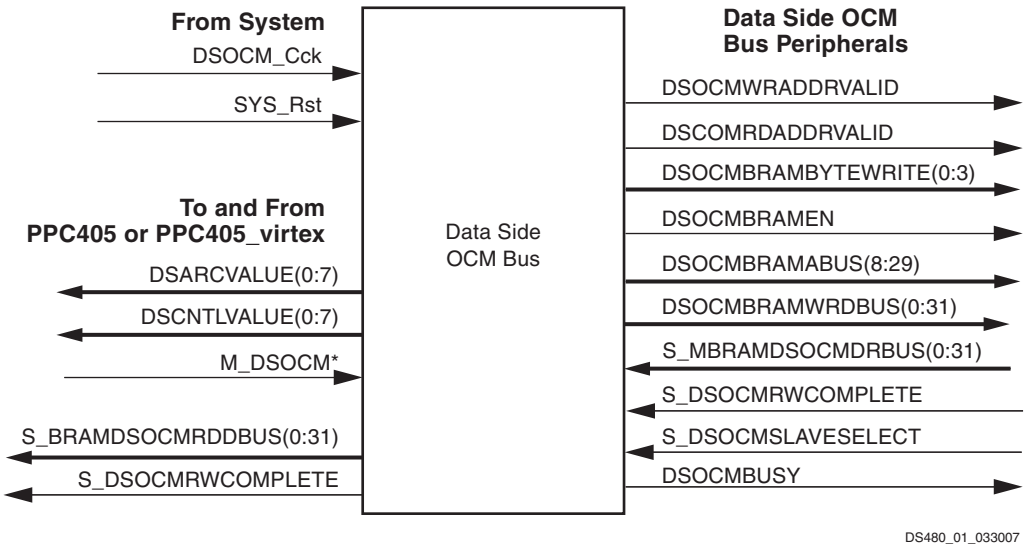

Figure 1: **Data-side OCM Bus Block Diagram**

Data Side OCM Bus I/O Signals

Table 1: **Data Side OCM Bus I/O**

Signal	I/O	Connects to	Description
DSOCM_Clk	I	system	Unused
SYS_Rst	I	system	Drives the output DSOCM_RST
DSOCM_RST	O	slaves	Reset signal for DSOCM slave peripherals
M_DSOCMBRAMABUS	I	ppc405	Drives the output DSOCMBRAMABUS
M_DSOCMBRAMEN	I	ppc405	Drives the output DSOCMBRAMEN
M_DSOCMRDADDRVALID	I	ppc405	Drives the output DSOCMRDADDRVALID
M_DSOCMWRADDRVALID	I	ppc405	Drives the output DSOCMWRADDRVALID
M_DSOCMBRAMWRDBUS	I	ppc405	Drives the output DSOCMBRAMWRDBUS.
M_DSOCMBRAMBYTE WRITE	I	ppc405	Drives the output DSOCMBRAMBYTEWRITE.
M_DSOCMBUSY	I	ppc405	Drives the output DSOCMBUSY.
S_DSOCMSLAVESELECT	I	slaves	Acknowledge signal from addressed slave. Controls read data multiplexing in multi-slave system.
S_DSOCMRWCOMPLETE	I	slaves	Virtex-4 only. Drives the output DSOCMRWCOMPLETE

Table 1: **Data Side OCM Bus I/O *(Contd)***

Signal	I/O	Connects to	Description
S_BRAMDSOCMRDDBUS	I	slaves	This signal connects directly to the output BRAMDSOCMRDDBUS.
DSOCMRDADDRVALID	O	slave	Virtex-4 only. Single cycle read request indicating that address is valid. Used with variable latency (non-BRAM) slaves
DSOCMWRADDRVALID	O	slave	Virtex-4 only. Single cycle write request indicating that address and write data are valid. Used with variable latency (non-BRAM) slaves
DSOCMRWCOMPLETE	O	ppc405	Virtex-4 only. Acknowledge that access has been completed by variable latency (non-BRAM) slave. Read data should be valid
BRAMDSOCMRDDBUS	O	ppc405	Read access read-data
DSARCVALUE	O	ppc405	DSOCM power-on16MB address window offset. The value of this signal is set by the parameter C_DSARCVALUE.
DSCNTLVALUE	O	ppc405	DSOCM power-on configuration. The value of this signal is set by the parameter C_DSCNTLVALUE.
DSOCMBRAMEN	O	slave	Memory enable signal for BRAM
DSOCMBRAMWRDBUS	O	slave	Write access write-data
DSOCMBRAMBYTEWRITE	O	slave	Write access byte enable
DSOCMBRAMABUS	O	slave	Read/Write access address bus
DSOCMBUSY	O	slave	DCR writable control signal. Reflects DSCNTL(2)

Data Side OCM Bus Parameters

Table 2: **Data SIde OCM Bus Parameters**

Parameter	Description	Default	Tool Calculated	Type
C_NUM_MASTERS	Number of DSOCM masters. The only allowed value is 1	1	Yes	integer
C_NUM_SLAVES	Number of DSOCM slaves	1	Yes	integer

Table 2: **Data SIde OCM Bus Parameters *(Contd)***

Parameter	Description	Default	Tool Calculated	Type
C_DSARCVALUE	Power-on offset of the 16 MB DSOCM address window relative to the PLB address range. For example, with C_DSARCVALUE=0x54, the DSOCM memory window will reside in the address range: 0x5400_0000-0x54FF_FFFF.	0x31	Yes	std_logic_vector
C_DSCNTLVALUE	Power-on configuration of the PowerPC DSOCM interface controller. For details, see the "*PowerPC 405 Block Reference Guide*"	0x81	Yes	std_logic_vector
C_FIXED_LATENCY	Virtex-4 only. Select between fixed return data latency (=1) or handshake (=0)	1	No	integer

Allowable Parameter Combinations

There are no restrictions on allowed parameter combinations in this core.

For information about the OCM controller interface feature, see the *PowerPC 405 Processor Block Reference Guide*.

Parameter - Port Dependencies

Table 3: **Port and parameter dependencies**

Name	Affects	Depends	Relationship Description
Design Parameters			
C_NUM_SLAVES	S_BRAMDSOCM RDDBUS	0 to C_NUM_ SLAVES*32-1	Scale width of OCM read data bus based on number of connected slaves
C_NUM_SLAVES	S_DSOCMRW COMPLETE	0 to C_NUM_ SLAVES	Scale width of OCM slave select based on number of connected slaves
C_NUM_SLAVES	S_DSOCMSLAVE SELECT	0 to C_NUM_ SLAVES	Scale width of OCM slave select based on number of connected slaves
Port Signals			
S_BRAMDSOCM RDDBUS		C_NUM_SLAVES	Scale width of OCM read data bus based on number of connected slaves
S_DSOCMRW COMPLETE		C_NUM_SLAVES	Scale width of OCM slave select based on number of connected slaves
S_DSOCMSLAVE SELECT		C_NUM_SLAVES	Scale width of OCM slave select based on number of connected slaves

Multi-Slave Configuration

This version of the bus can handle multiple slaves. Slave address ranges must be non-overlapping and each slave core is responsible for its own address range check. All readable slaves must follow one of two methods for returning data:

1. Provide an acknowledge signal (S_DSOCMSLAVESELECT) which they raise when addressed. When not addressed this signal must be held Low. The slave read-data is ignored when the acknowledge is Low. The DSOCM bus use the acknowledge signal as a valid signal to multiplex read-data.
1. Always provide a High acknowledge signal, but drive all 0's (zeros) on read-data when not addressed.

Data Side OCM Bus Register Descriptions

There are no registers in this core.

Data Side OCM Bus Interrupt Descriptions

There are no interrupts associated with this core.

Design Implementation

Design Tools

The Data Side OCM Bus design is handwritten.

Xilinx XST is the synthesis tool used for synthesizing the Data Side OCM Bus.

Target Technology

The intended target technology is a Virtex-II Pro™, or a Virtex-4™ FPGA.

Device Utilization and Performance Benchmarks

Table 4: **Data Side OCM Bus Resource Utilization**

Parameters	Resources	
	Flip-Flops	4-input LUTs
C_NUM_SLAVES = 1	0	0
C_NUM_SLAVES = 2	0	32
C_NUM_SLAVES = 3	0	64
C_NUM_SLAVES = 4	0	96

There are no performance benchmarks available.

Specification Exceptions

Not applicable.

Reference Documents

UG018 PowerPC 405 Processor Block Reference Guide

DS447 Data Side OCM BRAM Interface Controller Data Sheet

Revision History

Date	Version	Revision
1/23/2007	1.0	Initial Xilinx release.