LogiCORE IP Fixed Interval Timer v1.01c

Product Guide

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Table of Contents

SECTION I: SUMMARY

Introduction

The FIT core is a peripheral that generates a strobe (interrupt) signal at fixed intervals and is not attached to any bus. The Fixed Interval Timer (FIT) generates an interrupt every C_NO_CLOCKS. The interrupt signal is held High for one clock cycle. The core begins operation immediately after FPGA configuration unless the clock is held or a reset is connected to the FIT.

Features

- Configurable number of clock cycles between interrupts
- Configurable inaccuracy in clock intervals between interrupts
- Optional reset

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Zynq™-7000(2), Kintex™-7, Virtex®-7, Artix™-7, Virtex-6, Spartan®-6, Virtex-5, Virtex-4, Spartan-3, Spartan-3E, Spartan-3A/3AN/3A DSP
Supported User Interfaces	N/A
Resources	See Table 2-1
Provided with Core	
Design Files	ISE: VHDL Vivado: VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	N/A
Simulation Model	VHDL Behavioral
Supported S/W Driver	N/A
Tested Design Flows(3)	
Design Entry	Vivado™ Design Suite 2012.4(4) Xilinx Platform Studio (XPS)
Simulation	Mentor Graphics ModelSim Vivado Simulator
Synthesis	Xilinx Synthesis Technology (XST) Vivado Synthesis (4)
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete list of supported derivative devices, see Embedded Edition Derivative Device Support.
2. Supported in ISE Design Suite implementations only.
3. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.
4. Supports 7 series devices only.

Overview

FIT Interrupt Descriptions

The FIT generates an interrupt every C_NO_CLOCKS. The interrupt signal is held high for one clock cycle. The core begins operation immediately after FPGA configuration if the reset is not connected. If the reset is connected and asserted the FIT begins operation after the reset is released. To reset the SRL16 primitives the reset must be asserted for a minimum of 17 cycles. To reset the bit counter implementation the reset need only be asserted for one clock cycle.

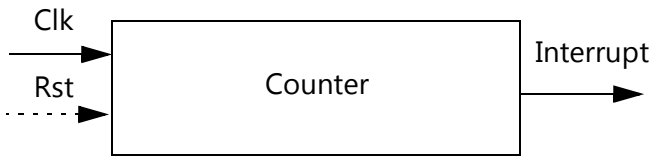

Figure 1-1: **FIT Block Diagram**

Design Tools

The FIT design is generated by the EDK or the Vivado™ Design Suite.

XST or Vivado synthesis is the synthesis tool used for synthesizing the FIT. The netlist output from the synthesis tool is then input to the Xilinx Project Naviagator or the Vivado Design Suite for actual device implementation.

Licensing and Ordering Information

This Xilinx LogiCORE™ IP module is provided at no additional cost with the Xilinx® Vivado Design Suite and ISE® Design Suite Embedded Edition tools under the terms of the Xilinx End User License.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

Performance

The frequency and latency of the FIT are optimized for use with MicroBlaze™. This means that the frequency targets are aligned to MicroBlaze targets.

Resource Utilization

The device utilization depends on the configured parameter values. For optimal device utilization the C_NO_CLOCKS should factor into numbers less than or equal to 16 and the reset should not be used.

The reset logic, when using the SRL16, doubles the resource usage, but in most cases this is still smaller than using a normal bit counter. When using the counter the reset logic adds 1 LUT.

Because the FIT core is used with other design modules in the FPGA, the utilization numbers reported in this section are estimates only. When the FIT core is combined with other designs in the system, the utilization of FPGA resources will vary from the results reported here.

The FIT core resource utilization for various parameter combinations measured with the Virtex®-6 FPGA as the target device are detailed in Table 2-1. This table shows the utilization without reset logic.

Table 2-1: **Resource Utilization Benchmarks on a Virtex-6 FPGA(1)**

Parameter Values		Device Resources		
C_NO_CLOCKS	C_INACCURACY	Slices	Slice Flip-Flops	LUTs
3	0	1	0	1
6216	0	4	14	14
6216	999	7	6	4
2147483647	0	8	32	32

1. Tested part is a xc6vlx240t-ff1156-3.

Port Descriptions

The I/O signals for the FIT are listed in Table 2-2.

Table 2-2: **FIT I/O Signals**

Signal Name	Interface	I/O	Initial State	Description
Clk	N/A	I	N/A	Clock
Rst	N/A	I	N/A	Optional reset
Interrupt	N/A	O	0	Interrupt signal

Designing with the Core

General Design Guidelines

This chapter includes guidelines and additional information to facilitate designing with the core.

Clocking

The input clock must be connected to the `Clk` port. The frequency of this clock, together with the C_NO_CLOCKS parameter, determines the time between strobes.

The inaccuracy between strobes is affected by the parameter C_INACCURACY. The parameter should normally be set to the default value 0, but resource usage can be reduced by allowing a certain inaccuracy.

Resets

The `Rst` port can be left unconnected or tied to ground to reduce resource usage. When resetting the SRL16 the reset signal must be asserted for at least 17 cycles. When resetting the bit counter the reset need only be asserted for one cycle.

SECTION II: VIVADO DESIGN SUITE

Customizing and Generating the Core

Constraining the Core

Customizing and Generating the Core

This chapter includes information about using Xilinx tools to customize and generate the core in the Vivado™ Design Suite environment.

GUI

The FIT configuration dialog is shown in Table 4-1.

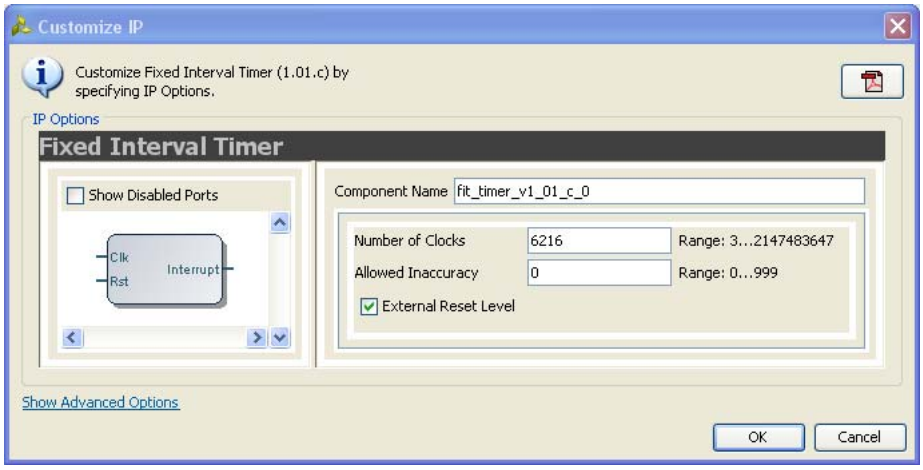

Figure 4-1: **Configuration Dialog**

- **Number of Clocks** - Sets the number of clock cycles between strobes.
- **Allowed Inaccuracy** - Defines the allowed inaccuracy between strobes. Normally this should not be changed from the default value of 0.
- **External Reset Level** - When checked indicates active-High level, and when unchecked indicates active-Low level.

Parameter Values

Table 4-1: **FIT Parameters**

Parameter Name	Feature /Description	Allowable Values	Default Value	Tool Assigned	VHDL Type
C_FAMILY	Device Family	Supported architectures	virtex7	Yes	string
C_NO_CLOCKS	The number of clock cycles between strobes	3 - 2147483647	6216	No	integer
C_INACCURACY	The allowed inaccuracy in the number of clock cycles between strobes. Expressed in per thousands.	0 - 999	0	No	integer
C_EXT_RESET_HIGH	Level of reset	0 = active-Low 1 = active-High	1	No	integer

Constraining the Core

This chapter contains information about constraining the core in the Vivado™ Design Suite environment.

Required Constraints

There are no required constraints for this core.

Device, Package, and Speed Grade Selections

There are no Device, Package or Speed Grade requirements for this core.

Clock Frequencies

There are no specific clock frequency requirements for this core.

Clock Management

There are no specific Clock management requirements for this core.

Clock Placement

There are no specific Clock placement requirements for this core.

Banking

There are no specific Banking rules for this core.

Transceiver Placement

There are no Transceiver Placement requirements for this core.

I/O Standard and Placement

There are no specific I/O standards and placement requirements for this core.

SECTION III: ISE DESIGN SUITE

Customizing and Generating the Core

Constraining the Core

Customizing and Generating the Core

This chapter includes information about using Xilinx tools to customize and generate the core in the ISE® Design Suite environment.

GUI

The FIT configuration dialog is shown in Figure 6-1.

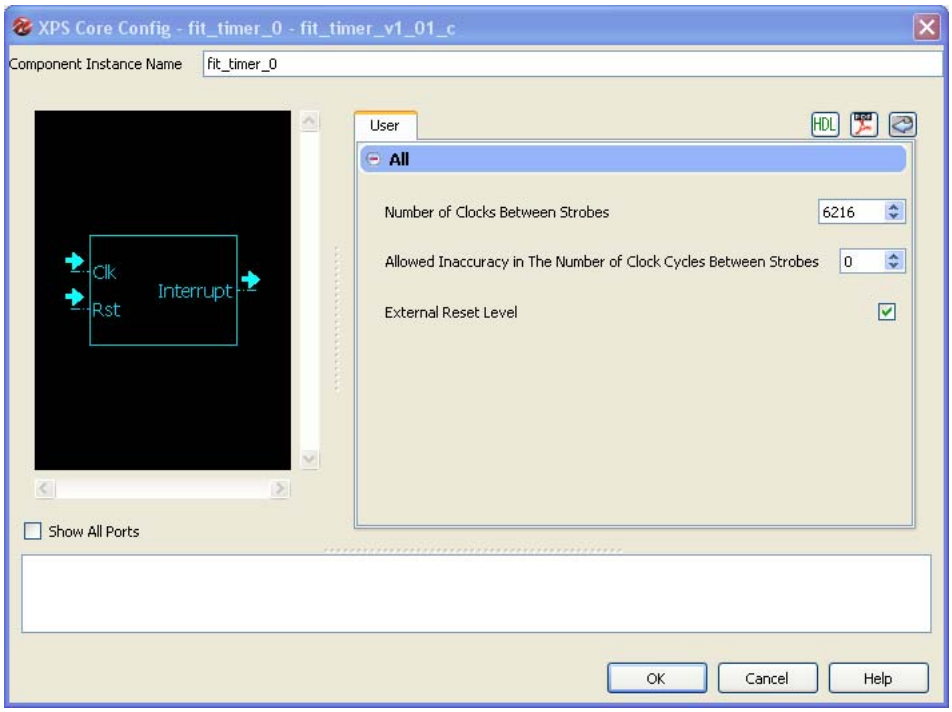

Figure 6-1: **Configuration Dialog**

- **Number of Clocks Between Strobes** - Sets the number of clock cycles between strobes.
- **Allowed Inaccuracy in The Number of Clock Cycles Between Strobes** - Defines the allowed inaccuracy between strobes. Normally this should not be changed from the default value of 0.
- **External Reset Level** - When checked indicates active-High level, and when unchecked indicates active-Low level.

Parameter Values

See Table 4-1 for a list of parameter values.

Constraining the Core

See SECTION II: VIVADO DESIGN SUITE, Chapter 5, Constraining the Core.

SECTION IV: APPENDICES

Debugging

Additional Resources

Appendix A

Debugging

This appendix provides information for using the resources available on the Xilinx Support website, debug tools, and other step-by-step processes for debugging designs that use the FIT.

Finding Help on Xilinx.com

To help in the design and debug process when using the FIT, the Xilinx Support web page (www.xilinx.com/support) contains key resources such as product documentation, release notes, answer records, information about known issues, and links for opening a Technical Support Web Case.

Documentation

This Product Guide is the main document associated with the FIT. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page (www.xilinx.com/support) or by using the Xilinx Documentation Navigator.

You can download the Xilinx Documentation Navigator from the Design Tools tab on the Downloads page (www.xilinx.com/download). For more information about this tool and the features available, open the online help after installation.

Release Notes

Known issues for all cores, including the FIT are described in the IP Release Notes Guide (XTP025.PDF).

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Contacting Technical Support

Xilinx provides premier technical support for customers encountering issues that require additional assistance.

To contact Xilinx Technical Support:

1. Navigate to www.xilinx.com/support.
2. Open a WebCase by selecting the WebCase link located under Support Quick Links.

When opening a WebCase, include:

- Target FPGA including package and speed grade.
- All applicable Xilinx Design Tools and simulator software versions.
- Additional files based on the specific issue might also be required. See the relevant sections in this debug guide for guidelines about which file(s) to include with the WebCase.

Appendix B

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

www.xilinx.com/support.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

References

These documents provide supplemental material useful with this product guide:

- Vivado™ Design Suite user documentation

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/18/12	1.0	Initial Xilinx release. This Product Guide is derived from DS451. There are no changes for release 14.4.

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