H.264 Deblocker Core v1.0

DS594 (v1.0) May 15, 2007 **Product Brief**

Features

- H.264/MPEG-4 Part 10 Baseline/Main/High Profiles at Level 4.2
- Compliant with International Standard ISO/IEC 14496-10:2005 (E) Rec. H.264 (E)
- Supports up to 300,000 Macroblocks/s operation
- Boundary Strength calculation internal to core
- Pass through mode
- FIFO reset facility for loss-of sync robustness
- Frame or Field processing
- 4:2:0 supported
- Two core types:
  - IF 0 (Economy)
  - IF 1 (Ease-of-Use)

Resource Summary

LogiCORE™ Facts			
Core Specifics			
Supported Device Families			Virtex™-5, Virtex-4, Spartan™-3E
Resources Used			
IF 0	Virtex-5	1080	1634 LUTs, 1565 flops 9 RAMB18x2, 3 RAMB36
		720P	1639 LUTs, 1563 flops 5 RAMB18x2, 3 RAMB36
		ITU-R-BT.601	1595 LUTs, 1550 flops 1 RAMB18x2, 7 RAMB36
		CIF	1575 LUTs, 1539 flops 1 RAMB18x2, 7 RAMB36
	Virtex-4	1080	21 block RAMs, 1438 slices
		720P	13 block RAMs, 1437 slices
		ITU-R-BT.601	9 block RAMs, 1382 slices
		CIF	9 block RAMs, 1358 slices
	Sparten-3E	1080	19 block RAMs, 1598 slices
		720P	11 block RAMs, 1577 slices
		ITU-R-BT.601	7 block RAMs, 1523 slices
		CIF	7 block RAMs, 1488 slices

LogiCORE™ Facts			
Core Specifics			
IF 1	Virtex-5	1080	1968 LUTs, 1948 flops 9 RAMB18x2, 6 RAMB36
		720P	1968 LUTs, 1946 flops 5 RAMB18x2, 6 RAMB36
		ITU-R-BT.601	1915 LUTs, 1918 flops 1 RAMB18x2, 10 RAMB36
		CIF	1933 LUTs, 1931 flops 1 RAMB18x2, 10 RAMB36
	Virtex-4	1080	23 block RAMs, 1764 slices
		720P	16 block RAMs, 1764 slices
		ITU-R-BT.601	12 block RAMs, 1715 slices
		CIF	12 block RAMs, 1685 slices
	Spartan-3E	1080	22 block RAMs, 1906 slices
		720P	14 block RAMs, 1914 slices
		ITU-R-BT.601	10 block RAMs, 1856 slices
		CIF	10 block RAMs, 1824 slices
Provided with Core			
Documentation			Data Sheet, User Guide
Design File Formats			VHDL, EDIF
Constraints File			
Verification			JM10 Reference C-Code vs. VHDL Testbench and HW-in-the-Loop
Instantiation Template			VHDL Wrapper
Design Tool Requirements			
Synthesis			Synplicity Synplify_Pro 8.6.2
Xilinx Implementation Tools			Xilinx ISE 8.2.03i (from ngd_build)
Verification			ModelSim 6.1c SE, MicroSoft Visual C++ V6.0, ActivePerl 5.8.3. Annapolis Micro Systems WildCard4 platform API 3.0, Driver 4.0, Firmware 1.0
Simulation			ModelSim 6.1c SE
Support			
Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing functionality, or support of product if implemented in devices not listed in the documentation, or if customized beyond that allowed in the product documentation, or if any changes are made in sections of the design marked DO NOT MODIFY.			

Introduction

The Xilinx H.264 Deblocking Version 1.0 core is a fully functional VHDL design implemented on a Xilinx FPGA. The Deblocker core accepts input parameters and macroblocks to deblock and generates output macroblocks as specified by the ITU-T Video Coding Experts Group (VCEG) together with the ISO/IEC Moving Picture Experts Group (MPEG) as the product of a collective partnership effort known as the Joint Video Team (JVT). The collaborative effort is also known as H.264/AVC/MPEG4 Part 10.

The aim of this core is to filter across the edges of the 4x4-pixel blocks inside and on the edge of a current input macroblock dependent upon a number of parameters and content-based criteria (see edges V1, V2, V3, H1, H2, and H3 in Figure 1. Also processed are the macroblock boundaries at the top and left edges (edges V0 and H0) of the current macroblock, requiring the availability of these adjacent macroblocks. It is important to note that this process also modifies the content of the adjacent macroblocks.

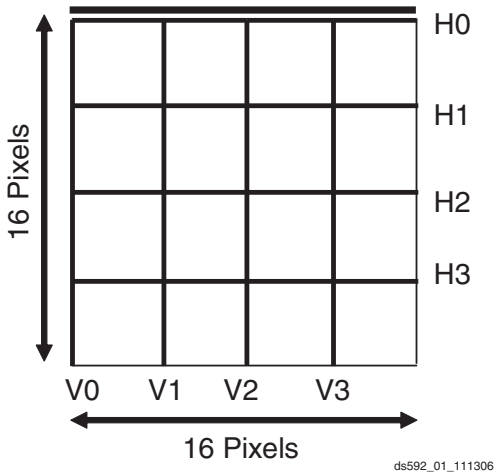

Figure 1: **Macroblock Edges**

Applications

The Deblocker core can be utilized in H.264 standard applications where hardware acceleration is needed to achieve real time operation. Typical video applications are video surveillance, video conferencing, and video broadcast. The Deblocker core can also be used as a post processing engine for previous standards, such as MPEG-2 decoder.

Performance

Target clock FMax and subsequent macroblocks throughput are summarized in Table 1. The throughput figures apply for IF 0 and IF 1 cores.

Table 1: **Performance Summary**

FPGA Family	Clock FMax	Approximate 4:2:0 Macroblock Throughput (Macroblocks/s)	Notes
Spartan-3E	150 MHz	200,000	Supports up to 601, 4CIF, 1080P/25, 720P/50
Virtex-4	225 MHz	300,000	Supports up to 1080P/30, 1080i/60, 720P/60
Virtex-5	225 MHz	300,000	Supports up to 1080P/30, 1080i/60, 720P/60

Revision History

Date	Version	Revision
05/15/07	1.0	Initial Xilinx release.