LogiCORE IP ChipScope Pro IBERT for 7 Series GTH Transceivers (v2.01a)

DS873 October 16, 2012 **Product Specification**

Introduction

The customizable LogiCORE™ IP ChipScope™ Pro Integrated Bit Error Ratio Test (IBERT) core for 7 series FPGA GTH transceivers is designed for evaluating and monitoring the GTH transceivers. This core includes pattern generators and checkers that are implemented in FPGA logic, and access to ports and the dynamic reconfiguration port attributes of the GTH transceivers. Communication logic is also included to allow the design to be run-time accessible through JTAG. This core can be used as a self-contained or open design, based on customer configuration, and as described in this document.

Features

- Provides a communication path between the ChipScope Pro Analyzer software and the IBERT core
- Provides a user-selectable number of 7 series FPGA GTH transceivers
- Transceivers can be customized for the desired line rate, reference clock rate, reference clock source, and datapath width
- Requires a system clock that can be sourced from a pin or one of the enabled GTH transceivers

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Virtex®-7
Supported User Interfaces	N/A
Resources	See Table 2 and Table 3.
Provided with Core	
Documentation	Product Specification User Guide
Design Files	Vivado™: RTL
Example Design	Verilog /VHDL
Test Bench	Not Provided
Constraints File	Xilinx Constraints and Synthesis Constraints
Simulation Model	Not Provided
Tested Design Flows(2)	
Design Entry	ISE Design Suite v14.3 Vivado Design Suite v2012.3(3)
Simulation	Not Provided
Synthesis	Xilinx Synthesis Technology (XST)
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete list of supported derivative devices, see the Embedded Edition Derivative Device Support.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.
3. Supports only 7 series devices.

© Copyright 2011-2012 Xilinx, Inc. Xilinx, the Xilinx logo, Artix, ISE, Kintex, Spartan, Virtex, Vivado, Zynq, 7 Series, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.

Applications

The IBERT core is designed to be used in any application that requires verification or evaluation of 7 Series FPGA GTH transceivers.

Functional Description

The IBERT core provides a broad-based Physical Medium Attachment (PMA) evaluation and demonstration platform for 7 series FPGA GTH transceivers. Parameterizable to use different GTH transceivers and clocking topologies, the IBERT core can also be customized to use different line rates, reference clock rates, and logic widths. Data pattern generators and checkers are included for each GTH transceiver desired, giving a variety of different Pseudo-random binary sequence (PRBS) and clock patterns to be sent over the channels. In addition, the configuration and tuning of the GTH transceivers is accessible though logic that communicates to the DRP port of the GTH transceiver, in order to change attribute settings, as well as registers that control the values on the ports. At run time, the ChipScope Analyzer tool communicates to the IBERT core through JTAG, using the Xilinx cables and proprietary logic that is part of the IBERT core.

GTH Transceiver Features

The IBERT core is designed for Physical Medium Attachment (PMA) evaluation and demonstration. All the major PMA features of the GTH transceiver are supported and controllable, including:

- TX pre-emphasis and post-emphasis
- TX differential swing
- RX equalization
- Decision Feedback Equalizer (DFE)
- Phase-Locked Loop (PLL) Divider settings

Some of the Physical Coding Sublayer (PCS) features offered by the transceiver are outside the scope of IBERT, including

- Clock Correction
- Channel Bonding
- 8B/10B, 64B/66B, or 64B/67B encoding
- TX or RX Buffer Bypass

PLL Configuration

For each serial transceiver channel, there is a ring Phase-Locked Loop (PLL) called Channel PLL (CPLL). The GTH in the 7 series FPGA has an additional shared PLL per quad, Quad PLL (QPLL). This QPLL is shared LC PLL to support high speed, high performance and low power multi-lane applications.

Figure 1 shows a Quad in a 7 series device. The GTHE2_CHANNEL component has the serial transceiver and CPLL units and the GTHE2_COMMON has the QPLL unit.

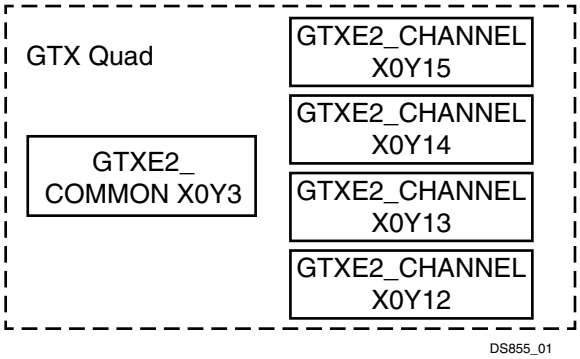

Figure 1: **Quad in a 7 Series Device**

The serial transceiver REFCLK can be sourced from either CPLL or QPLL based on multiplexers as shown in Figure 2. This can be selected from the 7 series FPGA IBERT Vivado IP Catalog tools GUI.

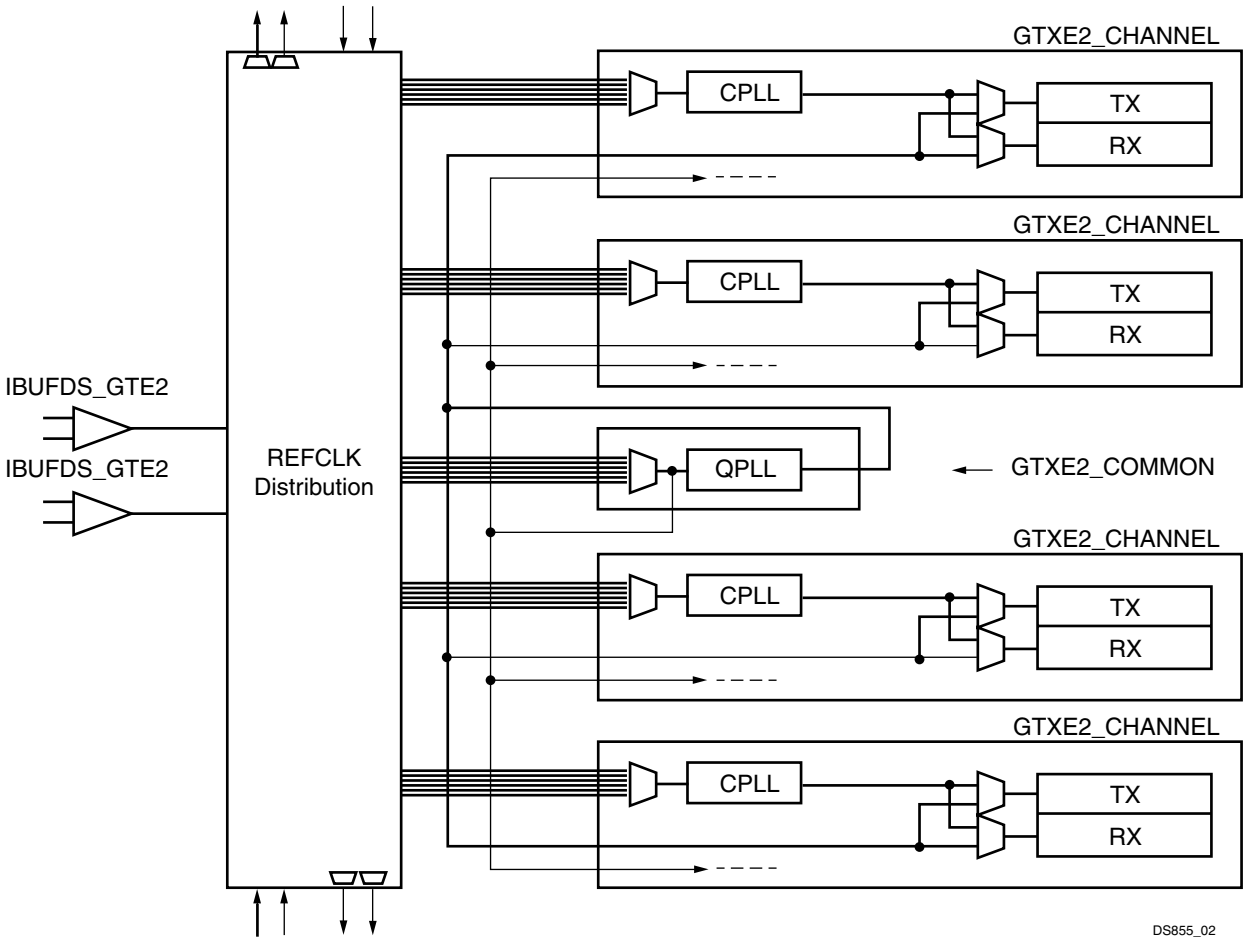

Figure 2: **Serial Transceiver REFCLK Sourcing**

Pattern Generation and Checking

Each GTH transceiver enabled in the IBERT design has a pattern generator and a pattern checker. The pattern generator sends data out through the transmitter. The pattern checker accepts data through the receiver and checks it against an internally generated pattern. IBERT offers PRBS 7-bit, PRBS 15-bit, PRBS 23-bit, PRBS31-bit, Clk 2x (101010...) and Clk 10x(11111111110000000000...) patterns.

These patterns are optimized for the logic width that was selected at run time. The TX pattern and RX pattern are individually selected.

The Analyzer software displays a 'link' signal until there are five consecutive cycles with errors. Using the pattern checker logic, the incoming data is compared against a pattern that is internally generated. When the checker receives five consecutive cycles of data with errors, the ChipScope Pro Analyzer software disables the link signal. Internal counters accumulate the number of words and errors received.

DRP and Port Access

You can change GTH transceiver ports and attributes. The DRP interface logic allows the run-time software to monitor and change any attribute of the GTH transceivers and the corresponding CPLL/QPLL. When applicable, readable and writable registers are also included that are connected to the various ports of the GTH transceiver. All are accessible at run time using the ChipScope Analyzer tool.

Vivado IP Catalog

The Vivado IP catalog allows you to define and generate a customized IBERT core to use to validate the transceivers of the device. You can customize the number of serial transceivers, line rate and reference clock, and PLL selection for each serial transceiver.

Entering the Component Name

The Component Name field, stored as `component_name` in the generated XCO parameter file, can consist of any combination of alpha-numeric characters including the underscore symbol. However, the underscore symbol cannot be the first character in the component name.

Generating an Example Design

The IBERT Vivado IP catalog normally generates example design along with standard Xilinx Vivado IP catalog output files, such as a netlist and instantiation template files. Example design and Implement scripts are generated under the folder with the component name.

Generate Bitstream

The Generate Bitstream is enabled by default. When generated, it runs through the entire implementation flow, including bitstream generation. When Generate Bitstream is disabled and generated, the design runs through synthesis. You can edit the example design and embed the custom design along with the IBERT instance. The implement script provided with the generated files allows you to run the example design until bitstream generation.

Receiver Output Clock

The receiver clock probe enable is provided to pull out a recovered clock from any serial transceiver, if desired. When enabled, a new panel appears just before the summary page where you can fill in the serial transceiver source and probe pin standards.

GTH Transceiver Naming Style

There are two conventions for naming the GTH transceiver, based on the location in the serial transceiver tile in the device. M and n in XmYn naming convention indicate the X and Y coordinates of the serial transceiver location. M and n in serial transceiver m_n naming convention indicating serial transceiver number and quad associated.

System Clock

The IBERT core requires a free-running system clock for communication and other logic that is included in the core. This clock can be chosen at generation time to originate from an FPGA pin, or to be driven from the TXOUTCLK port of one of the GTH transceivers. In order for the core to operate properly, this system clock source must remain operational and stable when the FPGA is configured with the IBERT core design. If the system clock is running faster than 150 MHz, it is divided down internally using an Mixed-Mode Clock Manager (MMCM) to satisfy timing constraints. Note that the clock source selected must be stable and free running after the FPGA is configured with the IBERT design. The system clock is used for core communication and as a reference for system measurements. Therefore, the clock source selected must remain operational and stable when using the IBERT core.

Line Rate Support

IBERT supports a maximum of three different line rates in a single design. For each of these line rates, you can select a custom value based on your requirements, or you can choose from pre-provided industry standard protocols (for example, CPRI™, Gigabit Ethernet, or XAUI). Specify the number of serial transceivers for each line rate that will be programmed with these settings. Because usage of QPLL is recommended for line rates above 6.5 Gb/s, you can select QPLL/CPLL for each line rate falling in the range 0.6 Gb/s to 6.5 Gb/s.

Serial Transceiver Location

Based on the total number of serial transceivers selected, provide the specific location of each serial transceiver that you intend to use. The region shown in the panel indicates the location of serial transceivers in the tile. This demarcation of region is based on the physical placement of serial transceivers with respect to median of BUFGs available for each device.

Reference Clock

The reference clock source should be provided for all the serial transceivers selected. The drop-down list provides you with possible sources based on local clocks in the same quad and shared clocks from north/south quads.

Generating the Core

After entering the IBERT core parameters, click Generate to create the IBERT core files. After the IBERT core has been generated, a list of files that are generated will appear in a separate window called "Readme <corename>".

IBERT Interface Ports

The I/O signals of the IBERT core consist only of the GTH transceiver reference clocks, the GTH transceiver transmit and receive pins, and a system clock (optional).

Table 1: **Interface Ports**

Port Name	Direction	Description
IBERT_SYSCLOCK_I	IN	Clock that clocks all communication logic. This port is present only when an external clock is selected in the generator.
CONTROL[35:0]	IN/OUT	Control bus connection to the ICON core.
XiYj_TX_N_OPAD[n-1:0](1) XiYj_TX_P_OPAD[n-1:0](1)	OUT	Transmit differential pairs for each of the n GTH transceivers used.
XiYj_RX_N_IPAD[n-1:0](1) XiYj_RX_P_IPAD[n-1:0](1)	IN	Receive differential pairs for each of the n GTH transceivers used.
Qk_CLK0_MGTREFCLK_I[m-1:0](2) Qk_CLK1_MGTREFCLK_I[m-1:0]	IN	GTH transceiver reference clocks used. ***Note:*** The number of MGTREFCLK ports can be equal to or less than the number of transmit and receive ports because some GTH transceivers can share clock inputs.
XiYj_RXOUTCLK_O(1)	OUT	Quad based RX output clock.

1. The XiYj name refers to the GTH site location.
2. The Qk name refers to the GTH quad site location.

Performance and Resource Utilization

Table 2: **Configuration Details**

Configuration	Device	IBERT Setup
Config1	XC7VX690T-FFG-1927-3	1 QUAD, 1 protocol set to 40b data width at 8.5 Gb/s with QPLL enabled.
Config2	XC7VX690T-FFG-1927-3	1 QUAD, 1 protocol set to 40b data width at 13.125 Gb/s with QPLL enabled
Config3	XC7VX690T-FFG-1927-3	2 QUADs, 1 protocol set to 40b data width at 10.3125 Gb/s with QPLL enabled

Table 3: **Performance and Resource Utilization for 7 Series FPGAs**

Configuration	Resources				Performance
	LUTs	Flip-Flops	DSP Slices	Block RAMs	F_{Max} (MHz)
Config1	9,208	11,569	0	0	327.5
Config2	7,950	11,569	0	0	327.5
Config3	15,864	22,600	0	0	327.5

Verification

Xilinx has verified the IBERT core in a proprietary test environment, using an internally developed bus functional model.

References

More information about the ChipScope Pro software and cores is available in the *Chipscope Pro Software and Cores User Guide*, located at www.xilinx.com/documentation.

For more information about the 7 series FPGA GTH transceiver, see the *7 Series FPGAs GTH Transceivers User Guide*, located at www.xilinx.com/documentation.

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

See the IDS Embedded Edition Derivative Device Support web page (www.xilinx.com/ise/embedded/ddsupport.htm) for a complete list of supported derivative devices for this core.

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx Vivado Design Suite and ISE Design Suite Embedded Edition tools under the terms of the Xilinx End User License.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

List of Acronyms

Acronym	Spelled Out
CPRI	Common Packet Radio Interface
DFE	Decision Feedback Equalizer
DRP	Dynamic Reconfiguration Port
FF	Flip-Flop
FPGA	Field Programmable Gate Array
IBERT	Integrated Bit Error Ratio Tester
I/O	Input/Output
ILA	Integrated Logic Analyzer
ISE	Integrated Software Environment
JTAG	Joint Test Action Group
LUT	Lookup Table
MMCM	Mixed-Mode Clock Manager
MHz	Mega Hertz
PCS	Physical Coding Sublayer
PLL	Phase-Locked Loop
PMA	Physical Medium Attachment
PRBS	Pseudorandom binary sequence
RAM	Random Access Memory
RX	Receive

Acronym	Spelled Out
TX	Transmit
XAUI	eXtended Attachment Unit Interface

Revision History

The following table shows a summary of changes to this document:

Date	Version	Revision
04/24/12	1.0	Initial Xilinx release.
10/16/12	2.0	Updated core to v2.01a for ISE Design Suite 14.3 and Vivado Design Suite v2012.3 release. Vivado updated in the IP Facts table and Vivado IP Catalog section.

Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties which can be viewed at http://www.xilinx.com/warranty.htm; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in Critical Applications: http://www.xilinx.com/warranty.htm#critapps.