

Introduction

The Xilinx® LogiCORE™ IP 3GPP LTE Channel Estimator v2.0 implements AXI4-Stream compliant, channel estimation functionality suitable to support decoding of the Physical Uplink Shared Channel (PUSCH) in LTE eNodeB applications as defined in 3GPP TS 36.211 specification. It represents one IP component in the Xilinx broader LTE Baseband Targeted Design Platform (TDP).

Additional Documentation

A product guide is available for this core. Access to this material may be requested by clicking on this registration link:
www.xilinx.com/member/chest_lte_eval/index.htm

Features

- Drop-in module for UltraScale architecture-based, Zynq-7000, Virtex-7, and Kintex-7 devices
- Support of channel estimation for 3GPP LTE Physical Uplink Shared Channel (PUSCH) with Single-Input, Single-Output (SISO) and Single-Input, Multiple-Output (SIMO) communication modes, Multi-User Multiple Input Multiple Output (MU-MIMO) communication modes
- Compliance with 3GPP-LTE TS 36.211 v9.0 (Release 9) standard specifications
- Parameterizable input/output data precision
- Bit accurate C-Language simulation model for system-level modeling

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family ⁽¹⁾	UltraScale™ Architecture, Zynq®-7000, Virtex®-7, Kintex®-7
Supported User Interfaces	AXI4-Stream
Provided with Core	
Design Files	RTL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	Bit Accurate C Model
Supported S/W Driver	Not Provided
Tested Design Flows⁽²⁾	
Design Entry	Vivado® Design Suite IP Integrator
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide .
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the [Xilinx Design Tools: Release Notes Guide](#).

Applications

Base station applications implementing eNodeB following the LTE specifications (3GPP TS 36.211). The 3GPP LTE Channel Estimator core performs the channel estimation function required for decoding of the PUSCH uplink data transmission in SISO and MU-MIMO modes of communication.

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

For the 3GPP LTE Channel Estimator core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
 - Resolved Issues
 - Known Issues
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Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the [Xilinx Core License Agreement](#). The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your [local Xilinx sales representative](#) for information about pricing and availability.

For more information, visit the 3GPP LTE Channel Estimator [product web page](#).

Information about other Xilinx LogiCORE IP modules is available at the [Xilinx Intellectual Property](#) page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your [local Xilinx sales representative](#).

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/2014	2.0	Characterization data link added to PG077.
12/18/2013	2.0	<ul style="list-style-type: none"> • Revision number reverted to 2.0 to align with core version number. • Added IP Integrator. • Added UltraScale support.
03/20/2013	2.1	<ul style="list-style-type: none"> • Updated core to v2.0 for Vivado Design Suite only. • Updated to Questa SIM.
10/16/2012	2.0	Minor document updates for 2012.3/14.3
10/19/2011	1.2	Updated for Release 13.3. Version 1.1 of Channel Estimator. Updated to include Virtex-7, Kintex-7 and Zynq-7000 support
08/15/2011	1.1	Updated to include web registration information
09/21/2010	1.0	Initial Xilinx release

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