LogiCORE IP 3GPP LTE MIMO Decoder v2.1

XMP040 September 30, 2012 **Product Brief**

Introduction

The Xilinx LogiCORE™ IP LTE MIMO Decoder v2.1 implements the uplink MIMO decoding functions for applications following the "3rd Generation Partnership Projects (3GPP); Evolved Universal Radio Access (E-UTRA); Physical Channels and Modulation (Release 9), 3GPP TS 36.211 V9.0.0 (2009-12) specification [Ref 1].

Features

- MMSE MIMO Decoder for spatial multiplexing MIMO systems
- Parameterizable drop-in module for Virtex®-5, Virtex-6, Virtex-6L, Virtex-7, Kintex™-7, and Zynq™-7000 devices
- Compliance with 3GPP-LTE specification, AXI4-Stream interface
- Key component of Xilinx LTE Baseband Targeted Design Platform
- High resource efficiency
- Supports four receive and four transmit antennas (4x4 spatial multiplexing MIMO system)
- Supports up to four antennas at the base station
- Supports up to four mobiles with one transmit antenna each, in MU-MIMO mode
- Supports one mobile with four transmit antennas in SU-MIMO mode
- Support for receive diversity only mode
- Bit accurate C model available
- Synchronous clear input
- Clock enable input

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family(1)	Zynq™-7000, Virtex®-7, Kintex™-7, Virtex-6, Virtex-6L,Virtex-5,				
Supported User Interfaces	AXI4-Stream				
	Resources(2)				**Frequency**
MIMO Configuration	**Slices**	**LUT/FF pairs**	**DSP Slices**	**Block RAMs(3)**	**Max. Freq.**
1x1	532	1427/ 1827	10	8	334.336
2x2	1304	3689/ 4614	48	9	337.154
3x3	2451	6875/ 8499	97	14	333.778
4x4	3586	10920/ 13363	162	15	313.087
Provided with Core					
Documentation	Product Brief Product Specification C Model User Guide				
Design Files	Netlist				
Example Design	Not Provided				
Test Bench	Contact Xilinx Support				
Constraints File	Not Provided				
Simulation Model	VHDL or Verilog Simulation Model Bit Accurate C Model				
Tested Design Tools					
Design Entry Tools	ISE 13.2(4)				
Simulation	Mentor Graphics ModelSim 6.6d				
Synthesis Tools	XST 13.2				
Support					
Provided by Xilinx @ www.xilinx.com/support					

1. For a complete list of supported derivative devices, see the IDS Embedded Edition Derivative Device Support.
2. Resources listed here are for Virtex-6 FPGAs.
3. Based on 18K block RAMs
4. For the supported versions of the tools, see the ISE Design Suite 13.2 Release Notes Guide.

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Applications

- Base station applications implementing eNodeB following the LTE specification [Ref 1]. The LTE MIMO Decoder v2.1 can perform the MMSE MIMO decoding function for uplink reception.
- Applications that can use a spatial multiplexing MMSE MIMO decoder that meet the timing and latency constraints of the LTE specification [Ref 1].

The LTE MIMO Decoder v2.1 is designed to fulfill the demanding processing requirements of MIMO decode in evolved 3GPP-LTE compliant base stations. A high level block diagram of the MIMO decoder and its location in the uplink system is shown in Figure 1. It is an MMSE MIMO decoder for spatial multiplexing MU-MIMO or SU-MIMO systems and is also optimized for receive diversity only systems. The core has been designed to meet the 3GPP-LTE timing and latency constraints.

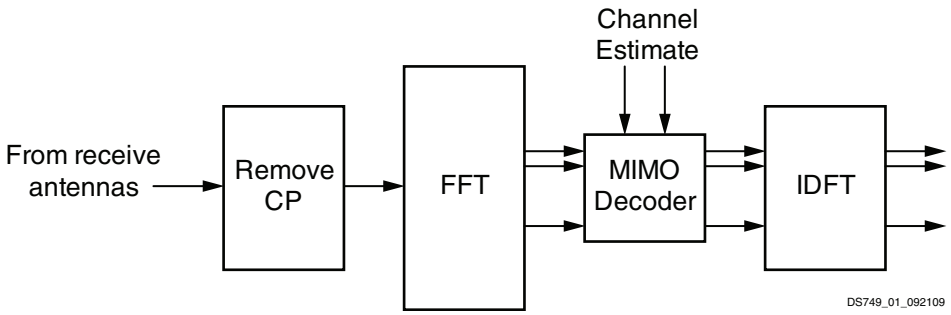

Figure 1: **Block Diagram of a 3GPP-LTE Uplink Receiver**

Additional Documentation and Supporting Materials

A full data sheet and additional supporting materials (C models and accompanying user guide documentation) are available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/3gpp_lte_mimo_decoder_eval/index.htm.

References

1. 3rd Generation Partnership Projects (3GPP); Evolved Universal Radio Access (E-UTRA); Physical Channels and Modulation (Release 9), 3GPP TS 36.211 V9.0.0 (2009-12)
2. XAPP1072: Target Platform Design for 3GPP LTE Uplink Receiver Application Note
3. UG726 - 3GPP LTE MIMO Decoder Bit Accurate C Model User Guide
4. UG761 - AXI Reference Guide

Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Refer to the IP Release Notes Guide (XTP025) for more information on this core. There will be a link to all DSP IP and then to the relevant core. For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Bug Fixes
- Known Issues

Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core Site License and the core is generated using the Xilinx ISE® CORE Generator™ software. The CORE Generator software is shipped with the Xilinx ISE Design Suite software.

For full access to all core functionality in simulation and in hardware, you must purchase a license for the core. Please contact your local Xilinx sales representative for information on pricing and availability of Xilinx LogiCORE IP modules. Information about additional modules is also available at the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/02/09	1.0	Initial Xilinx release.
12/14/10	2.0	Updated for ISE release 12.4 and version 2.0 of decoder
06/22/11	3.0	Updated for Release 13.2 - version 2.1 of decoder; updated to include Virtex-7, Kintex-7, and Zynq-7000 support.
08/15/11	3.1	Updated to include web registration information.
09/30/12	3.2	Updated reference to C Model User Guide.

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