LogiCORE IP 3GPP LTE MIMO Decoder v3.0

XMP040 April 2, 2014 **Product Brief**

Introduction

The Xilinx® LogiCORE™ IP LTE MIMO Decoder v3.0 implements the uplink MIMO decoding functions for applications following the 3rd Generation Partnership Projects (3GPP); Evolved Universal Radio Access (E-UTRA); Physical Channels and Modulation (Release 11), 3GPP TS 36.211 V11.0.0 (2012-09) specification [Ref 1].

Additional Documentation

A product guide is available for this core. Access to this material can be requested by clicking on this registration link: www.xilinx.com/member/3gpp_lte_mimo_decoder_eval/index.htm.

Features

- MMSE MIMO Decoder for spatial multiplexing MIMO systems
- Compliance with 3GPP-LTE specification, AXI4-Stream interface
- Key component of Xilinx LTE Baseband Targeted Design Platform
- High resource efficiency
- Supports four receive and four transmit antennas (4x4 spatial multiplexing MIMO system)
- Supports up to four antennas at the base station
- Supports up to four mobiles with one transmit antenna each, in MU-MIMO mode
- Supports one mobile with up to four transmit antennas in SU-MIMO mode
- Support for receive diversity only mode
- Synchronous clear input; clock enable input

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale™ Architecture, Zynq®-7030, Zynq-7045, Virtex®-7, Kintex®-7
Supported User Interfaces	AXI4-Stream
Provided with Core	
Design Files	Encrypted RTL
Example Design	Not Provided
Test Bench	Contact Xilinx Support
Constraints File	Not Provided
Simulation Model	VHDL Behavioral VHDL or Verilog Simulation Model Bit Accurate C Model
Tested Design Tools(2)	
Design Entry Tools	Vivado® Design Suite IP Integrator
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis Tools	Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

1. For a complete list of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Applications

- Base station applications implementing eNodeB following the LTE specification [Ref 1]. The LTE MIMO Decoder v3.0 can perform the MMSE MIMO decoding function for uplink reception.
- Applications that can use a spatial multiplexing MMSE MIMO decoder that meet the timing and latency constraints of the LTE specification [Ref 1].

The LTE MIMO Decoder v3.0 is designed to fulfill the demanding processing requirements of MIMO decode in evolved 3GPP-LTE compliant base stations. A high level block diagram of the MIMO decoder and its location in the uplink system is shown in Figure 1. It is an MMSE MIMO decoder for spatial multiplexing MU-MIMO or SU-MIMO systems and is also optimized for receive diversity only systems. The core has been designed to meet the 3GPP-LTE timing and latency constraints.

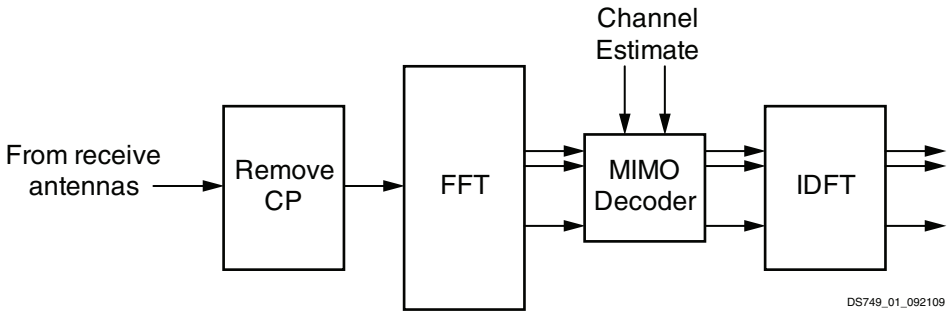

Figure 1: **Block Diagram of a 3GPP-LTE Uplink Receiver**

References

1. 3rd Generation Partnership Projects (3GPP); Evolved Universal Radio Access (E-UTRA); Physical Channels and Modulation (Release 11), 3GPP TS 36.211 V11.0.0 (2012-09)
2. *LogiCORE IP 3GPP LTE MIMO Decoder v3.0 Product Guide* (PG123), registration required.
3. *Vivado AXI Reference Guide* (UG1037)

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

For the master Answer Record related to the 3GPP LTE MIMO Decoder core, see AR: 54468.

Licensing and Ordering Information

This Xilinx LogiCORE™ IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information on pricing and availability.

To evaluate this core in hardware, generate an evaluation license, which can be accessed from the Xilinx IP Evaluation page. After purchasing the core, you will receive instructions for registering and generating a full license. The full license can be requested and installed from the Xilinx IP Center for use with the Vivado Design Suite.

For more information, visit the 3GPP LTE MIMO Decoder product page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
04/02/2014	4.0	Characterization data link added to PG123.
12/18/2013	4.0	Added UltraScale architecture support.
3/20/2013	4.0	Updated for core v3.0 and Vivado Design Suite-only support. Updated the technical support, and licensing and ordering information.
09/30/2012	3.2	Updated reference to C Model User Guide.
08/15/2011	3.1	Updated to include web registration information.
06/22/2011	3.0	Updated for Release 13.2 - version 2.1 of decoder; updated to include Virtex-7, Kintex-7, and Zynq-7000 support.
12/14/2010	2.0	Updated for ISE release 12.4 and version 2.0 of decoder
12/02/2009	1.0	Initial Xilinx release.

Please Read: Important Legal Notices